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COVER NOTE

From:	Secretary-General of the European Commission, signed by Mr Jordi AYET PUIGARNAU, Director
date of receipt:	26 September 2017
To:	Mr Jeppe TRANHOLM-MIKKELSEN, Secretary-General of the Council of the European Union
No. Cion doc.:	C(2017) 6321 final - Annex 1 Part 6/11
Subject:	ANNEX 1 Part 6/11 to the Commission Delegated Regulation amending Council Regulation (EC) No 428/2009 setting up a Community regime for the control of exports, transfer, brokering and transit of dual-use items

Delegations will find attached document C(2017) 6321 final - Annex 1 Part 6/11.

Encl.: C(2017) 6321 final - Annex 1 Part 6/11

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ANNEX 1 – PART 6/11

ANNEX

to the

Commission Delegated Regulation

amending Council Regulation (EC) No 428/2009 setting up a Community regime for the control of exports, transfer, brokering and transit of dual-use items

ANNEX I (PART VI – Category 4)

CATEGORY 4 - COMPUTERS

Note 1: *Computers, related equipment and "software" performing telecommunications or "local area network" functions must also be evaluated against the performance characteristics of Category 5, Part 1 (Telecommunications).*

Note 2: *Control units which directly interconnect the buses or channels of central processing units, "main storage" or disk controllers are not regarded as telecommunications equipment described in Category 5, Part 1 (Telecommunications).*

N.B. *For the control status of "software" specially designed for packet switching, see 5D001.*

4A Systems, Equipment and Components

4A001 Electronic computers and related equipment, having any of the following and "electronic assemblies" and specially designed components therefor:

N.B. *SEE ALSO 4A101.*

a. Specially designed to have any of the following:

1. Rated for operation at an ambient temperature below 228 K (-45°C) or above 358 K (85°C); or

Note: *4A001.a.1. does not control computers specially designed for civil automobile, railway train or "civil aircraft" applications.*

2. Radiation hardened to exceed any of the following specifications:

a.	Total Dose	5×10^3 Gy (silicon);
b.	Dose Rate Upset	5×10^6 Gy (silicon)/s; or
c.	Single Event Upset	1×10^{-8} Error/bit/day;

Note: *4A001.a.2. does not control computers specially designed for "civil aircraft" applications.*

b. Not used.

4A003 "Digital computers", "electronic assemblies", and related equipment therefor, as follows and specially designed components therefor:

Note 1: *4A003 includes the following:*
- *'Vector processors';*
- *Array processors;*
- *Digital signal processors;*
- *Logic processors;*
- *Equipment designed for "image enhancement".*

Note 2: *The control status of the "digital computers" and related equipment described in 4A003 is determined by the control status of other equipment or systems provided:*

a. *The "digital computers" or related equipment are essential for the operation of the other equipment or systems;*

b. *The "digital computers" or related equipment are not a "principal element" of the other equipment or systems; and*

N.B. 1: *The control status of "signal processing" or "image enhancement" equipment specially designed for other equipment with functions limited to those required for the other equipment is determined by the control status of the other equipment even if it exceeds the "principal element" criterion.*

N.B. 2: *For the control status of "digital computers" or related equipment for telecommunications equipment, see Category 5, Part 1 (Telecommunications).*

c. *The "technology" for the "digital computers" and related equipment is determined by 4E.*

4A003 continued

a. Not used;

b. "Digital computers" having an "Adjusted Peak Performance" ("APP") exceeding 16 Weighted TeraFLOPS (WT);

c. "Electronic assemblies" specially designed or modified for enhancing performance by aggregation of processors so that the "APP" of the aggregation exceeds the limit specified in 4A003.b.;

Note 1: *4A003.c. controls only "electronic assemblies" and programmable interconnections not exceeding the limit specified in 4A003.b. when shipped as unintegrated "electronic assemblies".*

Note 2: *4A003.c. does not control "electronic assemblies" specially designed for a product or family of products whose maximum configuration does not exceed the limit specified in 4A003.b.*

d. Not used;

e. Not used;

f. Not used;

g. Equipment specially designed for aggregating the performance of "digital computers" by providing external interconnections which allows communications at unidirectional data rates exceeding 2,0 Gbyte/s per link.

Note: *4A003.g. does not control internal interconnection equipment (e.g. backplanes, buses), passive interconnection equipment, "network access controllers" or "communications channel controllers".*

4A004 Computers as follows and specially designed related equipment, "electronic assemblies" and components therefor:

a. "Systolic array computers";

b. "Neural computers";

c. "Optical computers".

4A005 Systems, equipment, and components therefor, specially designed or modified for the generation, command and control, or delivery of "intrusion software".

4A101 Analogue computers, "digital computers" or digital differential analysers, other than those specified in 4A001.a.1., which are ruggedized and designed or modified for use in space launch vehicles specified in 9A004 or sounding rockets specified in 9A104.

4A102 "Hybrid computers" specially designed for modelling, simulation or design integration of space launch vehicles specified in 9A004 or sounding rockets specified in 9A104.

Note: This control only applies when the equipment is supplied with "software" specified in 7D103 or 9D103.

4B Test, Inspection and Production Equipment

None.

4C Materials

None.

4D Software

Note: The control status of "software" for equipment described in other Categories is dealt with in the appropriate Category.

4D001 "Software" as follows:

a. "Software" specially designed or modified for the "development" or "production" of equipment or "software" specified in 4A001 to 4A004, or 4D.

b. "Software", other than that specified in 4D001.a., specially designed or modified for the "development" or "production" of equipment as follows:

1. "Digital computers" having an "Adjusted Peak Performance" ("APP") exceeding 8,0 Weighted TeraFLOPS (WT);

2. "Electronic assemblies" specially designed or modified for enhancing performance by aggregation of processors so that the "APP" of the aggregation exceeds the limit in 4D001.b.1.

4D002 Not used

4D003 Not used.

4D004 "Software" specially designed or modified for the generation, command and control, or delivery of "intrusion software".

4E Technology

4E001 a. "Technology" according to the General Technology Note, for the "development", "production" or "use" of equipment or "software" specified in 4A or 4D.

b. "Technology", according to the General Technology Note, other than that specified in 4E001.a., for the "development" or "production" of equipment as follows:

1. "Digital computers" having an "Adjusted Peak Performance" ("APP") exceeding 8,0 Weighted TeraFLOPS (WT);

2. "Electronic assemblies" specially designed or modified for enhancing performance by aggregation of processors so that the "APP" of the aggregation exceeds the limit in 4E001.b.1.

c. "Technology" for the "development" of "intrusion software".

TECHNICAL NOTE ON "ADJUSTED PEAK PERFORMANCE" ("APP")

"APP" is an adjusted peak rate at which "digital computers" perform 64-bit or larger floating point additions and multiplications.

"APP" is expressed in Weighted TeraFLOPS (WT), in units of 10^{12} adjusted floating point operations per second

Abbreviations used in this Technical Note

n	number of processors in the "digital computer"
i	processor number (i,...n)
t_i	processor cycle time ($t_i = 1/F_i$)
F_i	processor frequency
R_i	peak floating point calculating rate
W_i	architecture adjustment factor

Outline of "APP" calculation method

1. For each processor i, determine the peak number of 64-bit or larger floating point operations, FPO_i, performed per cycle for each processor in the "digital computer".

   Note In determining FPO, include only 64-bit or larger floating point additions and/or multiplications. All floating point operations must be expressed in operations per processor cycle; operations requiring multiple cycles may be expressed in fractional results per cycle. For processors not capable of performing calculations on floating point operands of 64-bit or more, the effective calculating rate R is zero.

2. Calculate the floating point rate R for each processor $R_i = FPO_i/t_i$.

3. Calculate "APP" as "APP" = $W_1 \times R_1 + W_2 \times R_2 + \ldots + W_n \times R_n$.

4. For 'vector processors', $W_i = 0{,}9$. For non-'vector processors', $W_i = 0{,}3$.

Note 1 *For processors that perform compound operations in a cycle, such as addition and multiplication, each operation is counted.*

Note 2 *For a* pipelined *processor the effective calculating rate R is the faster of the pipelined rate, once the pipeline is full, or the non-pipelined rate.*

Note 3 *The calculating rate R of each contributing processor is to be calculated at its maximum value theoretically possible before the "APP" of the combination is derived. Simultaneous operations are assumed to exist when the computer manufacturer claims concurrent, parallel, or simultaneous operation or execution in a manual or brochure for the computer.*

Note 4 *Do not* include *processors that are limited to input/output and peripheral functions (e.g., disk drive, communication and video display) when calculating "APP".*

Note 5 *"APP"* values *are not to be calculated for processor combinations (inter)connected by "Local Area Networks", Wide Area Networks, I/O shared connections/devices, I/O controllers and any communication interconnection implemented by "software".*

Note 6 *"APP" values must be calculated for processor combinations containing processors specially designed to enhance performance by aggregation, operating simultaneously and sharing memory;*

Technical Note:

1. *Aggregate all processors and accelerators operating simultaneously and located on the same die.*
2. *Processor combinations share memory when any processor is capable of accessing any memory location in the system through the hardware transmission of cache lines or memory words, without the involvement of any software mechanism, which may be achieved using "electronic assemblies" specified in 4A003.c.*

Note 7 *A 'vector processor' is defined as a processor with built-in instructions that perform multiple calculations on floating-point vectors (one-dimensional arrays of 64-bit or larger numbers) simultaneously, having at least 2 vector functional units and at least 8 vector registers of at least 64 elements each.*