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IMPACT ASSESSMENT REPORT

Accompanying the document

**Proposal for a Regulation of the European Parliament and of the Council
on a framework of measures for strengthening Europe's semiconductor ecosystem
repealing Regulation (EU) 2023/1782 (Chips Act 2.0)**

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Glossary

Term or acronym	Meaning or definition
Advanced nodes	Semiconductor manufacturing processes at the leading edge of miniaturisation, conventionally referring to nodes at or below 7nm. They deliver higher performance and energy efficiency and are primarily used for high-performance computing, AI accelerators and flagship mobile processors. Note that modern node designations no longer correspond to a specific physical transistor dimension.
AI chips	Logic chips optimised for the matrix and tensor operations that underpin machine-learning training and inference. The category includes GPUs, dedicated AI accelerators (e.g. TPUs, NPU), FPGAs and purpose-built ASICs.
Back-end	The stages of semiconductor manufacturing that follow wafer fabrication, comprising dicing, assembly, packaging and test of the finished device.
Chiplet	A small, independent die designed to perform one or more specific functions and intended to be combined with other chiplets within a single advanced package, allowing modular design and mixing of process nodes.
Chips for Europe Initiative	The framework established under Pillar I of the Chips Act to build large-scale technological capacity and support research and innovation across the Union's semiconductor value chain. It covers design capacities, pilot lines, quantum chips, competence centres and access to finance.
Competence centre	Facilities forming a Union-wide network, at least one per Member State, that provide access to design services, pilot lines, expertise and training to support stakeholders in the semiconductor ecosystem, in particular SMEs. They facilitate technology transfer, skills development, and links between students and semiconductor companies across the Union.
Compound semiconductors	Semiconductors made from two or more chemical elements, in contrast to elemental semiconductors such as silicon. Key examples include silicon carbide (SiC) and gallium nitride (GaN), used in power electronics and RF applications, and gallium arsenide (GaAs) and indium phosphide (InP), used in optoelectronics and high-frequency communications. They offer performance characteristics such as high voltage, high frequency, high temperature tolerance, that silicon cannot match, and are strategically important for automotive electrification, renewable energy and telecommunications.

Deep Ultraviolet lithography (DUV)	A lithography technology using ultraviolet light at 248nm or 193nm wavelengths (the latter typically in an immersion configuration) to pattern wafers. DUV remains the workhorse of semiconductor manufacturing for mature nodes and, with multi-patterning techniques, can produce features down to around the 7nm node.
Design Centre of Excellence	A label that may be awarded by the Commission to design centres established in the Union that significantly enhance the Union's capabilities in innovative chip design, either through their service offerings or through the development, promotion and strengthening of design skills. Such centres are recognised as serving the public interest and contributing to the resilience of the Union's semiconductor ecosystem.
Electronic Design Automation (EDA)	The category of software tools used to design, simulate, verify and prepare for manufacturing the integrated circuits and printed circuit boards that make up electronic systems. EDA tools are indispensable to modern chip design, particularly at advanced nodes, and the market is highly concentrated among a small number of global suppliers.
European Semiconductor Board (ESB)	The governance body composed of high-level representatives of all Member States and chaired by the Commission, responsible for facilitating implementation of, cooperation under and information exchange relating to the Chips Act, including advising on international cooperation, crisis response, and the assessment of integrated production facilities and open EU foundries.
Extreme Ultraviolet lithography (EUV)	A lithography technology using 13.5nm wavelength light to pattern the finest features on advanced-node wafers. EUV is essential for manufacturing at and below the 7nm node and is supplied globally by a single company (ASML, headquartered in the Netherlands), making it a strategic chokepoint in the semiconductor value chain.
Fabless	A semiconductor company that designs and sells integrated circuits but does not own or operate a wafer fabrication plant, instead outsourcing manufacturing to a foundry. The fabless model separates design from production and is the counterpart to the foundry model.
First-of-a-kind facility (FOAK)	A new or substantially upgraded semiconductor manufacturing facility, or a facility for the production of equipment or key components for such equipment predominantly used in semiconductor manufacturing, which provides innovation with regard to the manufacturing process or final product that is not yet substantively present or committed to be built within the Union. The innovation may concern improvements in computing power, security, safety or reliability, energy and environmental performance, the

	technology node or substrate materials, production-process efficiency, recyclability, or the reduction of production inputs.
Foundry	A semiconductor manufacturing company that fabricates wafers on behalf of other firms, typically fabless companies, IDMs or system companies, according to their designs, without selling chips under its own brand. A pure-play foundry undertakes no design of its own.
Front-end	The stages of semiconductor manufacturing from a blank wafer through to a completed, patterned wafer, comprising lithography, etching, deposition, doping and related process steps.
Heterogeneous integration	The assembly and interconnection within a single advanced package of multiple components, such as chiplets, memory stacks, photonic devices or sensors, that may be produced on different process technologies or from different materials. It is a leading alternative to traditional monolithic scaling and underpins the chiplet ecosystem.
Important Projects of Common European Interest (IPCEI)	Large-scale projects bringing together companies and research centres from several Member States to deliver significant benefits to strategic EU goals such as competitiveness, sustainable growth, addressing societal challenges and creating value across the Union.
Integrated Device Manufacturers (IDMs)	Semiconductor companies that design, manufacture (in their own fabs) and sell integrated-circuit products, in contrast to the fabless–foundry model.
IP block	A reusable, pre-designed and pre-verified unit of logic, cell or chip layout that can be licensed and integrated into a larger integrated-circuit design. Also referred to as a semiconductor IP core or design IP, IP blocks (e.g. CPU cores, memory controllers, interface PHYs) shorten design cycles and are a key input to modern system-on-chip development.
Lithography	The patterning step in semiconductor manufacturing in which the circuit design is transferred onto the wafer using light projected through a mask onto a light-sensitive coating (photoresist). Lithography is the principal driver of feature-size scaling and one of the most capital-intensive and technologically demanding steps in chip production.
Mature technology nodes	Established semiconductor manufacturing processes, conventionally referring to nodes at or above 28nm. They offer lower cost, high production stability and long product lifecycles, and remain dominant in high-volume applications such as automotive electronics, power management, industrial controls and consumer products. Also referred to as legacy nodes.

Memory chips	Semiconductor devices designed to store data, distinct from logic chips, which process it. The main families are DRAM (dynamic random-access memory, used as main system memory), NAND flash (non-volatile storage for SSDs and mobile devices) and NOR flash (typically used for code storage).
Microcontroller (MCU)	A small, self-contained integrated circuit combining a processor core, memory and input/output peripherals on a single chip, designed for embedded control applications. MCUs are produced predominantly at mature nodes and are central to automotive, industrial and consumer electronics. Shortages of automotive MCUs were a defining feature of the 2021–2023 semiconductor crisis.
Moore's Law	The empirical observation, formulated by Gordon Moore in 1965 and revised in 1975, that the number of transistors on an integrated circuit doubles roughly every two years. Although it is not a physical law, it has served for decades as a guiding target for the industry and as a proxy for progress in cost, performance and energy efficiency. The pace of scaling has slowed at advanced nodes, prompting greater emphasis on architectural innovation, advanced packaging and heterogeneous integration.
Original Equipment Manufacturers (OEMs)	Companies that produce systems or components which are integrated into another company's end product. In the semiconductor context, OEMs typically incorporate chips and modules supplied by others into the products they design, brand and sell.
Photonic chips	Integrated circuits that process or transmit information using light (photons) rather than, or in addition to, electrical signals. Silicon photonics i.e. photonic devices fabricated using CMOS-compatible silicon processes, is a particularly active area, with applications in high-bandwidth data-centre interconnects, telecommunications, sensing and emerging quantum technologies.
Pilot line	An experimental project or experimental production addressing higher technology readiness levels (TRL 3 to 8), used to further develop the enabling infrastructure required to test, demonstrate, validate and calibrate a product or system against its model assumptions.
Quantum chips	Integrated devices that exploit quantum-mechanical phenomena such as superposition and entanglement to perform computation, sensing or communication tasks. Several physical implementations are under active development, including superconducting circuits, trapped ions, photonic platforms and silicon-spin qubits. Quantum chips are explicitly supported under Pillar I of the Chips Act.

Substrate	The underlying material on which semiconductor devices are fabricated. The dominant substrate is monocrystalline silicon, supplied as wafers; other substrates include silicon carbide and gallium nitride (for power and RF devices), gallium arsenide and indium phosphide (for optoelectronics), and silicon-on-insulator (SOI) variants for specialised applications. The choice of substrate determines key device characteristics and constrains the available process technology.
System-on-Chip (SoC)	An integrated circuit that combines on a single die all the major functional components of a complete electronic system — typically including one or more processor cores, memory, input/output interfaces and specialised accelerators. SoCs are common in smartphones, embedded systems and increasingly in automotive and AI applications, and are usually assembled from a mix of in-house and licensed IP blocks.
Technology node	A designation referring to a specific semiconductor manufacturing process generation and its associated design rules. Historically tied to a physical transistor dimension (notably gate length), the term is today primarily a marketing and benchmarking label that signals a generation of performance and density rather than a measurable feature size.
Transistor	The fundamental building block of modern integrated circuits: a semiconductor device that acts as an electronic switch or amplifier by controlling current flow between two terminals through a voltage or current applied to a third. Billions of transistors, typically of the MOSFET family (including FinFET and gate-all-around variants at advanced nodes), are integrated on a single chip.
Yield	The proportion of functional dies produced on a wafer relative to the maximum theoretical number. Yield is a critical determinant of the unit cost and economic viability of a semiconductor process, particularly at advanced nodes where defect sensitivity is high and a single fab can represent investments of well over EUR 10 billion.

1 INTRODUCTION: POLITICAL AND LEGAL CONTEXT

1.1 Political context

Semiconductors underpin all digital technologies from household appliances to defence equipment to the data centres at the core of the artificial intelligence (AI) revolution. Since 2020, a series of shortages of supply stemming from crises, such as the COVID-19 pandemic, disruptions, such as the recent Nexperia case, and the ongoing supply-demand mismatch in the memory market expose how excessive external dependencies can render entire markets vulnerable. Increased geopolitical rivalry, including Sino-American tensions, and the emergence of AI have further amplified the crucial role of semiconductors, which have become a strategic asset in geopolitics. Without question, chips occupy an essential place in the global technological race.

Semiconductors are the third most traded commodity globally (after oil and vehicles), reaching revenues of USD 700.9 billion in 2025⁽¹⁾. It is widely expected that the market size of the semiconductor industry will reach USD 1 trillion by 2026⁽²⁾. The industry's role as a critical supplier to most modern industries and to the infrastructure that supports the rest, has elevated it to an important strategic resource which, in a more transactional world, can be a source of geopolitical leverage. Regions without significant capabilities in this domain find themselves dependent on components that others can restrict or condition in an increasingly coercive global environment.

The European Chips Act, which has been in force since September 2023, has served as a catalyst for renewed momentum and investment in the European semiconductor industry. It is a prime example of a new wave of European industrial policies and was conceived to reinforce the semiconductor ecosystem in the EU, ensure the security of supply chains and reduce external dependencies. It focuses on **five strategic objectives**:

1. Strengthening research and technological leadership
2. Building and reinforcing the EU's capacity to innovate in the design, manufacturing and packaging of advanced chips
3. Putting in place an adequate framework to increase production by 2030
4. Addressing the skills shortage and attracting new talent
5. Developing an in-depth understanding of global semiconductor supply chains

Under Pillar I of the Chips Act, the *Chips for Europe Initiative*⁽³⁾, over 85% of the Union's budget has been committed to the deployment of five pilot lines, a network of competence centres in all Member States, a Design Platform, six quantum chip pilot lines, skills development activities and scale-up investment in start-ups via the Chips Fund⁽⁴⁾.

⁽¹⁾ [WSTS Semiconductor Market Forecast Spring 2025](#)

⁽²⁾ [Global chip sales expected to hit \\$1 trillion this year, industry group says | Reuters](#)

⁽³⁾ [European Chips Act: The Chips for Europe Initiative | Shaping Europe's digital future](#)

⁽⁴⁾ A detailed analysis of these initiatives and the state of play of the implementation can be found in the annexed Evaluation of the Chips Act.

Through Pillar II⁽⁵⁾, the Chips Act has triggered around EUR 80 billion in announced or planned manufacturing investments in the Union. Key projects include the **European Semiconductor Manufacturing Company's (ESMC)** fab in Dresden (Germany) - bringing FinFET technology ⁽⁶⁾ to the EU; the **SiliconBox** facility in Novara (Italy) - a first advanced packaging facility in the EU; and the **STMicroelectronics Silicon Carbide (SiC) campus in Catania** (Italy) - now the world's largest SiC facility.

By the end of 2025, the Commission had approved eleven First-of-a-Kind projects, worth over EUR 31.6 billion of public and private investment. These projects include investments in mainstream semiconductor technologies to meet the needs of key European user industries, such as automotive⁽⁷⁾. Once these investments materialise, it is expected that the manufacturing capacity of the Union will increase by 30%, from 1.07 million wafers per month in 2023 to over 1.39 million wafers per month in 2030.⁽⁸⁾

As part of the activities under Pillar III of the Chips Act⁽⁹⁾, through the European Semiconductor Board (ESB), the Commission and Member States are coordinating more closely their activities and jointly building a crisis response mechanism, as set out in the Regulation.

Nevertheless, despite this considerable progress and the Union's strengths in key segments of the semiconductor value chain such as mainstream semiconductor production (including power electronics, embedded systems components, photonics, sensors), manufacturing equipment and materials, clear gaps in capabilities still need to be addressed. To this end, the EU must double down on its efforts to create an investment environment that is conducive for advanced front-end manufacturing, advanced packaging and heterogeneous integration fabs, as well as the ramp-up of leading-edge design activities, while maintaining a strong and competitive industry for more mature technologies. The vulnerabilities generated by these capability gaps become more consequential as productivity gains from the deployment of AI become more pronounced⁽¹⁰⁾.

Since the adoption of the Chips Act, the dynamics of the semiconductor market have shifted drastically, with AI becoming the key driver of revenues. Over the past two years, market growth has been largely driven by chips for AI datacentres (processors, memory), whilst most other segments have remained stagnant. This trend is expected to continue. According to McKinsey ⁽¹¹⁾, between 2023 and 2030, the AI logic chip segment is projected to grow at a compound annual growth rate (CAGR) of 18-29%, while AI memory chips are expected to grow at a CAGR of 17-23%, in contrast to most other semiconductor segments (excluding the China market) that are likely to show a more subdued performance, with average growth of

⁽⁵⁾ [European Chips Act: Security of supply and resilience | Shaping Europe's digital future](#)

⁽⁶⁾ The FinFET (Fin Field Effect Transistor) process is a 3D process adopted to overcome the limitations of conventional planar (2D) transistor structures and is used mostly for technology nodes between 16nm and 5nm.

⁽⁷⁾ [JRC, EU's strengths and weaknesses in the global semiconductor sector, 2025](#)

⁽⁸⁾ IDC, Semiconductors market data by feature size, sector and region, CNECT/2022/MVP/0084 – Second Interim Report. Risks here include economic downturns or market turbulations.

⁽⁹⁾ [European Chips Act: Monitoring and crisis response | Shaping Europe's digital future](#)

⁽¹⁰⁾ [The AI productivity take-off is finally visible](#)

⁽¹¹⁾ [AI's uneven impact on semiconductor industry market share | McKinsey](#)

around 3%. For the foreseeable future, AI-related components are expected to drive growth, and as seen in Figure 1, they should represent over 70% of the total semiconductor market by 2030⁽¹²⁾.

This shift in market dynamics is coupled with the stark reality that the EU finds itself without the sovereign means to compete effectively in a world where access to advanced AI technologies is becoming a key determinant of competitiveness. Unlike its main global competitors, the EU lacks the capacity necessary to capture a meaningful share of the rapidly expanding AI-driven market. As a result, the Union's dependence on third country suppliers for cutting-edge semiconductor manufacturing is near-total, exposing critical downstream industries to significant supply chain vulnerabilities and risks.

This needs to be addressed alongside continued consolidation of current European strengths that are crucial for important industrial verticals in the EU, such as automotive, industrial automation, aerospace and defence, and telecommunications. These however require relatively small volumes of semiconductors that are unable to sustainably maintain a viable semiconductor manufacturing ecosystem on their own, especially at more leading-edge technologies. Therefore, to safeguard the security of supply of these critical sectors, more needs to be done to stimulate demand in other sectors, which then create the conditions for a sustainable ramp-up of supply.

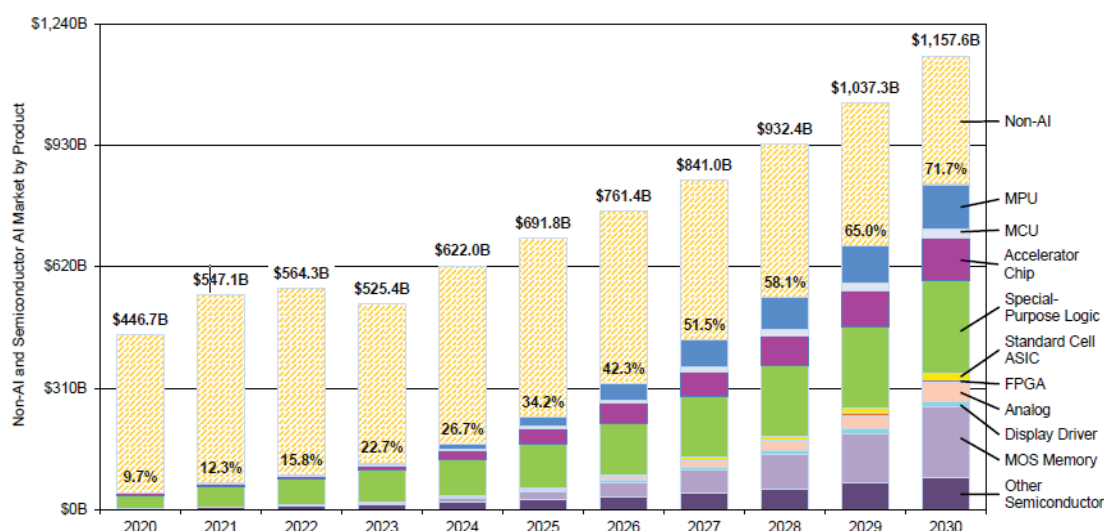


Figure 1 - Total Semiconductor Market and AI-related Share by Product (Source: IBS)¹³

To this end, humanoid robots and wearables are emerging application areas that are expected to generate significant future demand for semiconductors ⁽¹⁴⁾. Although both markets remain relatively small today, their projected growth is a sign of potential over the medium to long term until 2035-2040 and the EU could benefit from it. While industrial robots are already crucial factors in deploying automation in factories, humanoid robots are expected to expand

⁽¹²⁾ IBS, Global Semiconductor Industry Service, Semiconductor Market by Application Part 1, February 2025.

⁽¹³⁾ IBS, Global Semiconductor Industry Service, Semiconductor Market by Application Part 1, February 2025.

⁽¹⁴⁾ [McKinsey | The next big arenas of competition](#)

rapidly due to their potential in services, care, and human–machine interaction. The global semiconductor market for humanoid robots is estimated at EUR 360 million in 2024, and, under an optimistic uptake scenario, it is projected to grow at 26.2% annually to reach EUR 4.7 billion by 2035 ⁽¹⁵⁾. In the EU27, direct semiconductor consumption is estimated at EUR 70 million in 2024, increasing to EUR 770 million by 2035 (23.8% annual growth). Wearables constitute a second future-oriented market, combining consumer and healthcare applications. The global semiconductor market for wearables amounts to EUR 17 billion in 2024 and is expected to grow at 6.3% annually, reaching EUR 33.2 billion by 2035 ⁽¹⁶⁾.

Both applications present an opportunity for Europe since they require compute capacity at the edge, an area where the Union has considerable expertise and know-how. This will however require significant private investment, stimulated by public support, to ensure that incumbent and upcoming semiconductor suppliers in the EU are in a position to capture significant shares of these future markets. A robust semiconductor industry in the Union requires a three-pronged approach that carves out a space for European semiconductor solutions in the AI ecosystem, consolidates current strengths, and ventures into new markets

Against this backdrop, both Member States and the European Parliament have called for a renewed impetus to the EU’s efforts in the field of semiconductors. Through the ‘*Semicon Coalition*’ ⁽¹⁷⁾, all 27 EU Member States have called for a coordinated approach to ensure prosperity, indispensability and resilience:

- **Prosperity:** enabling a competitive European semiconductor ecosystem that enhances Europe’s economic welfare and value creation across end-markets.
- **Indispensability:** maintain and develop Europe’s technological and innovation leadership to secure critical control points in the global semiconductor value chain.
- **Resilience:** secure a stable and reliable supply of trustworthy semiconductors for Europe’s most critical sectors, particularly in times of global disruption or geopolitical uncertainty.

In March 2025, 54 Members of the European Parliament signed a letter ⁽¹⁸⁾ to the Commission calling for a revised Chips Act, with a core focus on “*AI chips and other semiconductor technologies that were not adequately covered under the initial proposal*”. Similarly, the European Parliament adopted an own-initiative report on European Technological Sovereignty and Digital Infrastructure ⁽¹⁹⁾ calling for urgent action to boost EU domestic semiconductor manufacturing, to put advanced AI chips at the core of the revision of the Chips Act, and to adapt the Chips Act to the architecture of the proposed Multiannual

⁽¹⁵⁾ Decision Etudes & Conseil and YOLE Group, Competitiveness of the EU semiconductor manufacturing industry, Nov.2025.

⁽¹⁶⁾ Decision Etudes & Conseil and YOLE Group, Competitiveness of the EU semiconductor manufacturing industry, Nov.2025.

⁽¹⁷⁾ [Semicon Coalition calls for reinforced Chips Act | Shaping Europe’s digital future](#)

⁽¹⁸⁾ [MEPs urge the Commission to propose a Chips Act 2.0 | Euractiv](#)

⁽¹⁹⁾ [REPORT on European technological sovereignty and digital infrastructure | A10-0107/2025 | European Parliament](#)

Financial Framework (MFF), particularly to the European Competitiveness Fund proposal ⁽²⁰⁾.

1.2 Relevant existing EU legislation and related initiatives

Semiconductors are critical enablers of the green and digital transitions, and their strategic importance for the EU is further amplified by geopolitical tensions, the Union's current over-dependence on advanced manufacturing and design, and the increasing weaponisation of these dependencies by third countries. In this context, Chips Act 2.0 is indispensable to the achievement of the Commission's political priorities, notably "*A new plan for Europe's sustainable prosperity and competitiveness*" and "*A new era for European defence and security*".

In the aftermath of the **Draghi report** ⁽²¹⁾, competitiveness became a central component of the Commission's political priorities for 2024-2029 ⁽²²⁾, triggering a series of initiatives. The report singled out semiconductors as a key sector in which Europe needs to close the innovation gap, contribute to a joint decarbonisation and competitiveness plan, increase security, and reduce dependencies. In his report, Prof. Draghi called for a new, better articulated and concerted approach to boost the EU's future competitiveness in this sector by "*developing a comprehensive EU Semiconductor Strategy, supported by a dedicated EU-level budget for semiconductors; enhanced funding for innovation, including grants or R&D tax incentives for fabless chip design companies and for foundries operating in strategically relevant segments*". Prof. Draghi's report also called for coordinated EU action in **back-end 3D advanced packaging, advanced materials, and finishing processes**²³, as well as the establishment of an **EU-wide**, streamlined, and investment-friendly **permitting regime** for semiconductor manufacturing. Furthermore, the report called for Europe to draw lessons from other regions and focus resources on a single large-scale leader in advanced chips, supported by a clear strategic focus and strong public-private alignment. ⁽²⁴⁾

The Competitiveness Compass ⁽²⁵⁾, a roadmap to restore Europe's economic dynamism and boost growth, was the Union's first response to Prof. Draghi's call to address the key challenges identified in his analysis: closing the innovation gap with the US and China, harmonising decarbonisation with competitiveness, and enhancing economic security by reducing dependencies.

⁽²⁰⁾ The related policy measures are subject to the ongoing interinstitutional negotiations related to the Multiannual Financial Framework.

⁽²¹⁾ [Mario Draghi. \(2024\). The future of European competitiveness: In-depth analysis and recommendations \(Part B\).](#)

⁽²²⁾ [Priorities 2024-2029 - European Commission](#)

⁽²³⁾ **Finishing processes** refer to the back-end stages of semiconductor manufacturing, encompassing assembly, packaging, and testing operations that transform processed wafers into functional, market-ready devices. Advanced finishing techniques such as 2.5D/3D packaging and chiplet integration are increasingly critical to semiconductor performance and represent a growing source of competitive differentiation in the global value chain.

⁽²⁴⁾ [The Draghi report: one year on](#)

⁽²⁵⁾ [Competitiveness compass - European Commission](#)

Several initiatives and measures in the Competitiveness Compass are of direct relevance to the strategic development of the EU's semiconductor industry. For example, the upcoming Cloud and AI Development Act will include **actions in relation to cutting-edge AI chips** through the stimulation of new data centres in the EU and can be a source of demand generation that will support the aims and objectives of the revised Chips Act. The **AI Continent Action Plan Communication** ⁽²⁶⁾ outlined how, as part of the broader effort to develop **AI Gigafactories**, the Union aims to realise “**strategic autonomy in the design and production of AI semiconductors, reduce dependencies on critical technologies, and strengthen sovereignty in cutting edge semiconductors**”. It consequently called for the acceleration of preparatory work towards a revised Chips Act in 2026.

The **Industrial Action Plan for the European automotive sector** ⁽²⁷⁾ underscored the importance of the semiconductor industry for an innovative and digitalised automotive sector. The transition to Software-Defined Vehicles, in which semiconductors will serve as a central and differentiating element, further highlights the need for a robust and competitive semiconductor ecosystem in the EU.

This initiative is also linked to the **Joint Communication on Strengthening Economic Security** ⁽²⁸⁾, which underlines that access to high-quality information and its thorough analysis are the foundation of effective, well-informed EU economic security policymaking and decision-making. In this context, this initiative contributes to strengthening supply chain resilience and reducing strategic dependencies, while developing and maintaining EU leadership in critical technologies. Similarly, the initiative is coherent with the adopted **EU Action Plan on Drone and Counter Drone Security**, in particular with the aim to the development of a competitive European drone market.

Chips Act 2.0 is also designed in complementarity with other initiatives such as the Important Projects of Common European Interest (IPCEI). Here, the preparation of the upcoming IPCEI on Advanced Semiconductor Technologies (AST) ⁽²⁹⁾ is a welcome initiative and fully in line with the spirit of the **Chips Act** by addressing the crucial bridging of the lab-to-fab gap.

Chips Act 2.0 is designed to be compatible with the current MFF (2021-2027) and the next MFF (2028-2034), including the European Competitiveness Fund and Framework Programme 10 (FP10). Its architecture will allow for immediate action and impact under the current MFF while ensuring continuity and scalability under the next MFF. The proposal does not alter or circumvent the design and architecture set out in the Commission's proposal on the MFF 2028–2034, nor does it pre-empt its implementation.

⁽²⁶⁾ [The AI Continent Action Plan | Shaping Europe's digital future](#)

⁽²⁷⁾ [Action plan on the future of the automotive sector - Mobility and Transport](#)

⁽²⁸⁾ [Commission announces strategic approach to strengthen Europe's economic security](#)

⁽²⁹⁾ The IPCEI AST is designed to build on existing EU initiatives, in particular pilot lines and the EU Chips Design Platform, ensuring continuity and acceleration rather than duplication. Driven by megatrends such as AI, automation, security and sustainability, IPCEI AST should provide a collective European response to disruptive technological change. It focuses on key technology areas including AI chips and accelerators, photonic integrated circuits, heterogeneous integration and advanced packaging, sensors, power electronics, energy-efficient solutions and secure communication, while covering the full semiconductor value chain, including enabling technologies such as EDA, equipment, testing, materials and wafers.

Furthermore, the revised options under Chips Act 2.0 are designed to remain coherent with existing State aid and competition frameworks, in particular the R&D&I Framework and the IPCEI Communication, while preserving their distinct objectives. As under the current framework, the IPCEIs and the R&D&I Framework will continue playing a central role in supporting research, development, innovation and first industrial deployment, notably for highly innovative and cross-border projects with strong spillover effects.

Measures under Chips Act 2.0 will build on this architecture by further clarifying and refining the scope of the First-of-a-Kind (FOAK) framework under Pillar II, which addresses a complementary and previously insufficiently covered investment gap at the manufacturing stage.

Chips Act 2.0 will also be coherent with the Chips Joint Undertaking (JU), established under Council Regulation (EU) 2021/2085 ('Single Basic Act') and funded by the **Digital Europe** and the **Horizon Europe** programmes, given that it is the main body responsible for implementing four of the five Pillar I objectives of the current and the revised Chips Act, i.e., pilot lines, the design platform, competence centres, and quantum chips.

Finally, Chips Act 2.0 is consistent with European cybersecurity legislation. Certain categories of chips are in scope of the **Cyber Resilience Act** and investments under the Chips Act will aim to complement its objectives by building on the strength of the European industry in the secure chips market segment.

Cybersecurity risks, including risks related to dependency on high-risk suppliers, may be observed in several critical Information and Communication Technologies (ICT) supply chains in the Union, including semiconductors. The recently adopted proposal for the revision of the **Cybersecurity Act** puts in place supply chain security requirements for certain sectors based on both "technical" and "non-technical" criteria. This would allow to exclude high-risk suppliers from third countries posing cybersecurity concerns from tendering for certain critical infrastructures in the EU, thus potentially increasing the demand for chips from domestic undertakings or undertakings from third countries providing equivalent assurances. In turn, **Chips Act 2.0** will support EU semiconductor manufacturers to invest in order to increase their production and maintain their leading position in secure products to be able to fulfil this demand, and add a security of supply dimension for the semiconductors publicly procured by critical entities. In concert with this approach, the Communication on Technological Sovereignty accompanying the Chips Act 2.0 proposal will announce that a cybersecurity risk assessment will evaluate both technical vulnerabilities and non-technical factors in anticipation of the revision of the Cybersecurity Act.

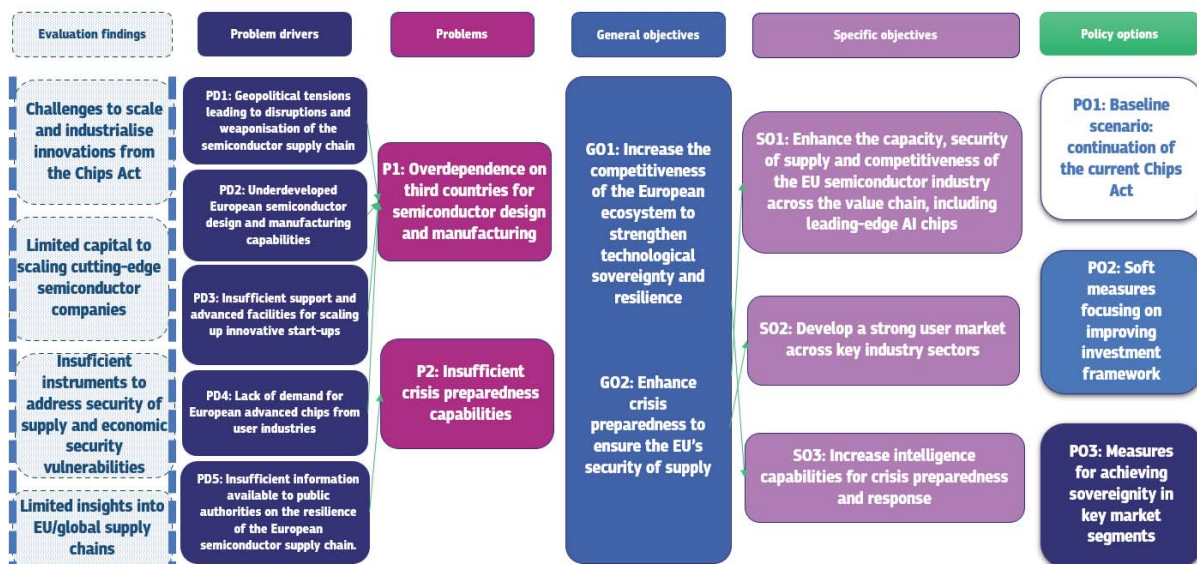


Figure 2- Intervention logic

2 PROBLEM DEFINITION

2.1 What is/are the problems?

The semiconductor value chain is critical to a wide range of industrial sectors. Its complexity makes it inherently fragile, and the Union's industry has experienced significant supply disruptions in recent years, which prompted the adoption of the first Chips Act on the 13 of September 2023. Despite those efforts, the EU continues to face major challenges in ensuring the secure, resilient and reliable supply of critical semiconductors. In this context, the two key problems that the revision of the Chips Act aims to resolve are the following: (1) overdependence on third countries for semiconductor design and manufacturing and (2) insufficient crisis preparedness capabilities.

2.1.1 P1: Overdependence on third countries for semiconductor design and manufacturing

The EU's semiconductor ecosystem **lacks sufficient design and manufacturing capacity to support its industrial base and wider digitalisation efforts. It is too reliant on a small number of countries and external actors.** Given the pervasiveness of semiconductors, this problem has a Union-wide dimension and carries important implications for all Member States.

Semiconductor shortages are a lived experience for industry in the EU. Supply shortages resulting from the COVID-19 pandemic cost the European automotive sector over EUR 100 billion from 2021 to 2022⁽³⁰⁾, and the recent Nexperia disruptions ⁽³¹⁾ resulted in an estimated

⁽³⁰⁾ [Missing chips cost EUR100bn to the European auto sector | Allianz](#)

⁽³¹⁾ [Europe's carmakers face 'devastating' chip crisis as Nexperia supply crunch continues | Minister of Economic Affairs invokes Goods Availability Act | News item | Government.nl](#)

EUR 5 billion in lost output ⁽³²⁾. Around 40% of the end-user participants in the open public consultation (OPC) reported chip shortages over the previous 12-24 months and a majority expect supply disruptions in the next 2-3 years, underlining how supply disruptions are becoming a lived experience for European industry ⁽³³⁾. Workshop participants as well as interview partners also observed overdependence on Asian suppliers, in particular when it comes to high-performance chips. Examples provided by stakeholders in the medical, industrial and telecoms sectors illustrated the resulting vulnerability of Europe's supply chains ⁽³⁴⁾.

Disruptions at Nexperia

On 30 September 2025, the Dutch Minister of Economic Affairs issued an order ⁽³⁵⁾ under its national Goods Availability Act regarding the semiconductor manufacturer Nexperia. ⁽³⁶⁾ Separately, on 1 October 2025, the Amsterdam Enterprise Chamber of Appeal took interim measures related to the company. ⁽³⁷⁾ Shortly afterwards, the Chinese authorities imposed company-specific export control measures on all Nexperia locations in China. This prevented packaged chips manufactured by Nexperia in China, following front-end production in Europe, from being re-imported into the EU. Economic operators in the EU and elsewhere faced shipment delays and stoppages, with knock-on effects for downstream industries and resulting production disruptions. Automotive manufacturers warned of potential production halts. ⁽³⁸⁾ The Chinese government eased export restrictions in early November and shipments of available chips have resumed, but uncertainties remain, and dwindling stocks may lead to further production disruptions in a multitude of end-user industries, including the automotive sector. ⁽³⁹⁾

2.1.1.1 Market concentration and clustering in the semiconductor industry

The semiconductor supply chain is prone to disruption due to the strong concentration of semiconductor manufacturing at both regional and company level. According to the Organisation for Economic Co-operation and Development (OECD)⁴⁰, in 2025, China, Taiwan, South Korea, Japan, and the United States accounted for 87% of global in-production wafer capacity, while the ten largest manufacturers held about half of the total global capacity. This concentration has structurally increased but is a result of cumulative processes that ran over decades⁴¹. Several factors have contributed to this situation.

First, a big part of the technological knowledge in the semiconductor domain is process knowledge, which has been accumulated by companies over years and cannot easily be acquired by another firm, since it is bound to human capital and subject to strict intellectual

⁽³²⁾ [Europe's Carmakers Brace for Severe Chip Supply Crisis](#)

⁽³³⁾ Annex 2 Sections 4, 5 and 6.

⁽³⁴⁾ Annex 2 Sections 4, 5 and 6.

⁽³⁵⁾ Pursuant to the order, the Dutch Minister of Economic Affairs may block or reverse company decisions where they are, or could be, harmful to the company's interests, its future as a Dutch and European enterprise, and/or the preservation of this critical value chain for Europe.

⁽³⁶⁾ [Minister of Economic Affairs invokes Goods Availability Act | News item | Government.nl](#)

⁽³⁷⁾ [ECLI:NL:GHAMS:2025:2752, Gerechtshof Amsterdam, 200.359.769/01 OK 2](#)

⁽³⁸⁾ [Automotive alarm: "Without Nexperia chips imminent stop in production." EU mediates betwe...](#)

⁽³⁹⁾ [Honda to halt production at plants in Japan and China due to chip shortage - The Japan Times](#)

⁽⁴⁰⁾ [The chip landscape. Geographical distribution of wafer fabrication capacity](#)

⁽⁴¹⁾ [The chip landscape. Geographical distribution of wafer fabrication capacity; Semiconductors and Modern Industrial Policy](#)

property protection and trade secrets. This cumulativeness of the knowledge base gives incumbent firms a significant head start.

Second, manufacturing is characterised by very high upfront CAPEX costs, which can go up to USD 20 to 30 billion for a leading-edge fab. This makes it very difficult for new companies to enter the market and is a powerful force for market consolidation. High fixed costs require consistently high utilisation rates in order to ensure economically viable production, creating strong economies of scale which further contribute to market concentration. In addition, customer relationships in the sector are highly entrenched, making it difficult to enter new market segments or attract customers as illustrated by the challenges faced by Intel in entering the foundry market ⁽⁴²⁾.

Finally, semiconductor firms crucially depend on a dense local ecosystem of specialised suppliers and service firms. Key manufacturers are surrounded by a web of specialised suppliers, chemical providers, equipment servicers, and a deep pool of trained engineers.

2.1.1.2 Semiconductor dependencies in the EU

In 2024, total chip consumption in the EU reached EUR 55 billion, of which EUR 43.6 billion was imported from third countries ⁽⁴³⁾. **EU-based production therefore accounts for only 22% of the Union's overall chip consumption** ⁽⁴⁴⁾. Out of EUR 43.6 billion in semiconductor imports in 2024, 35% originated from China and Taiwan as seen in **Figure 3**.

It is important to note that these figures largely reflect the final stages of the value chain and may underestimate upstream stages (including some in the EU), given that many dies are only packaged in these countries at the final stage of chip production. Moreover, the data does not capture chips imported as part of finished systems.

⁽⁴²⁾ See Evaluation of the Chips Act

⁽⁴³⁾ Decision Etudes & Conseil and YOLE Group, Competitiveness of the EU semiconductor manufacturing industry, Nov.2025.

⁽⁴⁴⁾ Excluding chips imported as part of broader systems; Decision Etudes & Conseil and YOLE Group, Addressing dependencies under Chips Act 2.0, Nov.2025.

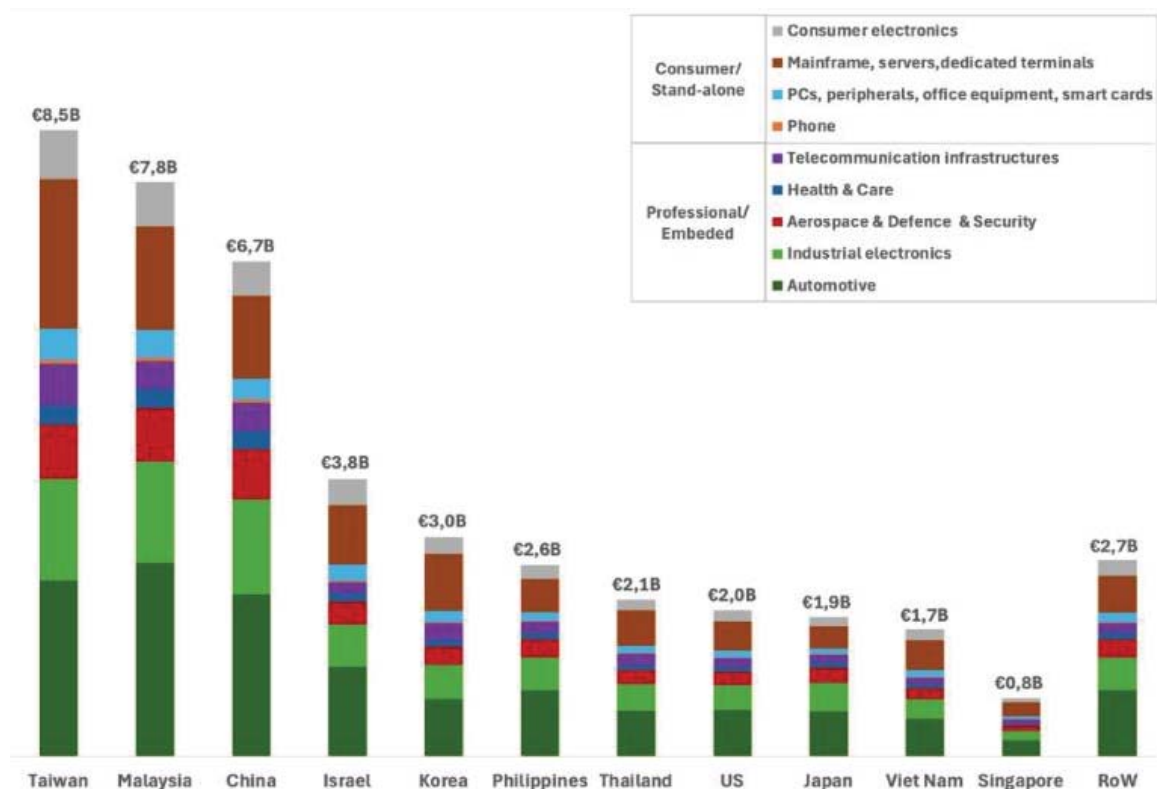


Figure 3 - EU chips consumption by origin of supply, 2024 (EUR Billion) (Source: Yole/Decision)⁴⁵

For the purposes of this Impact Assessment, four key areas of overdependence will be analysed: first, in the design and manufacturing of leading-edge chips, which are critical to a competitive and resilient AI value chain in the EU; second, in mature-technology chips, which remain essential to industries such as automotive and industrial automation; third, in memory chips; and finally, across upstream stages of the semiconductor value chain from a broader perspective.

⁴⁵ Decision Etudes & Conseil and YOLE Group, Competitiveness of the EU semiconductor manufacturing industry, Nov.2025.

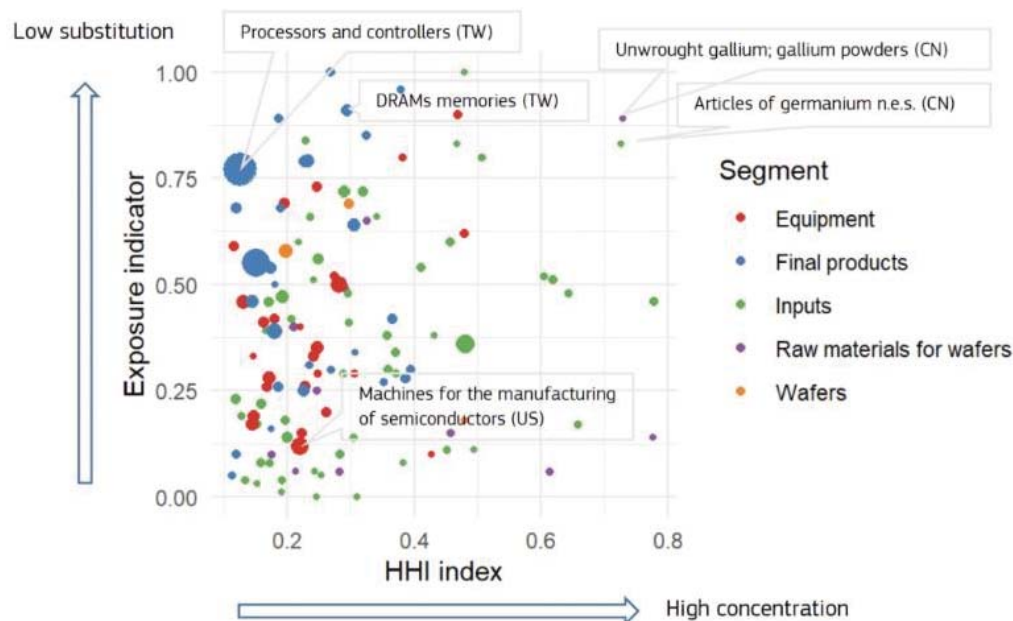


Figure 4 - Concentration of imports and potential substitution with EU production, by product, 2023 (size of bubble denotes import volumes) (JRC, 2025).

As seen in **Figure 4**, which provides a general overview of Europe's exposure along the semiconductor value chain, certain strategic inputs for the industry are acute EU supply vulnerabilities. Products such as unprocessed gallium and germanium have minimal EU domestic production and depend heavily on imports from China, creating concentrated single-source exposure even where total import values are modest. Similar dependency risks appear in several semiconductor categories: DRAM memories and specific processor/controller subsegments show limited scope for domestic substitution, while large import volumes are sourced primarily from Asian suppliers, notably Taiwan. This combination of high import concentration and low substitutability heightens the EU's vulnerability to geopolitical shocks, export controls, and supply chain disruptions. **These dependencies are further analysed in this sub-section, subsequent problem drivers and in Annex 4.**

2.1.1.3 Leading-edge chips

The Union's overdependence is most striking when it comes to leading-edge and advanced chips used for AI, high-performance computing, defence, or telecom applications ⁽⁴⁶⁾. As of today, **the EU has no foundry capacity for leading-edge semiconductor manufacturing** and is fully dependent on chip designs originating in the US and on fabrication capacities located in Taiwan and South Korea ⁽⁴⁷⁾. In Leixlip, Ireland, one can find leading-edge

⁽⁴⁶⁾ Leading-edge and advanced chips are produced at very small node sizes (currently at 7nm to 3nm, with 2nm being ramped up).

⁽⁴⁷⁾ IDC, Semiconductors market data by feature size, sector and region, CNECT/2022/MVP/0084 – Second Interim Report.

capacity (Intel 3 i.e. 3nm, one generation behind the current state-of-the-art) estimated at around 35,000 300mm wspm (wafer starts per month) that is used for Intel's own internal manufacturing, as part of its Integrated Device Manufacturer (IDM) model. ⁽⁴⁸⁾

Furthermore, capacities for the **design of leading-edge chips** leading to mass manufacturing are virtually non-existent in the EU ⁽⁴⁹⁾. Design is an important part of the problem, since production facilities need demand for the economic viability of manufacturing leading-edge chips. Europe faces a chicken-and-egg problem, as one weakness contributes to another vulnerability. Despite over EUR 80 billion in announced investments stemming from the Chips Act, the EU still lacks a full-fledged open foundry with capacities to produce chips below 10nm ⁽⁵⁰⁾.

In the absence of AI chips designed and manufactured in the Union, Europe's dependence on this rapidly expanding market segment is increasing at an alarming pace. As cutting-edge chips underpin virtually all future strategic growth markets, ranging from defence and security to drones, humanoids and service robotics, autonomous vehicles, and 5G/6G networks, there is a significant risk that Europe will be excluded from the future growth markets that will define economic competitiveness and technological sovereignty ⁽⁵¹⁾.

2.1.1.4 Mature node chips

Mature node chips are chips fabricated with older generation, well-established manufacturing processes, larger in node size. Their reliability and cost-effectiveness make them widely used in various applications where cutting-edge performance is not necessary.

European semiconductor companies have long-standing strengths in microcontrollers (MCU), analogue, sensors and power devices. In these segments, EU consumption is high, and front-end capacity is well aligned with the needs of EU industries: MCUs and analogue chips which benefit from a robust 40–90 nm production in the EU; Micro-Electro-Mechanical Systems (MEMS) that build on established EU competencies; and power electronics, where the EU benefits from a strong base of device manufacturers, particularly in the rapidly growing Silicon Carbide (SiC) segment.

However, as node sizes go smaller than 40nm, supply chain vulnerabilities start to emerge. Investments stemming from the Chips Act, particularly the ESMC project in Dresden,

In 2023, foundry manufacturing capacity at technology nodes of 7 nm and below was highly concentrated, with Taiwan accounting for 77% and South Korea for the remaining 23%. Intel's manufacturing capacity in Leixlip, Ireland is intended for internal use as discussed above. In 2024, 96% of AI chips sold in the EU were from US vendors (source: Decision Etudes & Conseil and YOLE Group, Competitiveness of the EU semiconductor manufacturing industry, Nov.2025.).

⁽⁴⁸⁾ IDC, Semiconductors market data by feature size, sector and region, CNECT/2022/MVP/0084 – Second Interim Report; The Intel Leixlip fab also has foundry capacity at 16nm.

⁽⁴⁹⁾ IDC, Semiconductors market data by feature size, sector and region, CNECT/2022/MVP/0084 – Second Interim Report.

⁽⁵⁰⁾ [Intel exit in Magdeburg: "This is not a good day for Europe" | heise online](#)

⁽⁵¹⁾ [McKinsey technology trends outlook 2025 | McKinsey](#)

Germany, should improve the situation, with upcoming capacity in 28/22nm technology and eventually 16/12nm.⁵²

The European industry in the mature node segment is also threatened from the ramping up of capacity in Asia, leading to possible overcapacity risks in certain sectors. For instance, China's massive capital expenditure has outpaced all other regions, rising from 6.8% of global CAPEX in 2012 to 42.3% in 2024, 36.5% in 2025 and 31.5% in 2026 (until April '26).

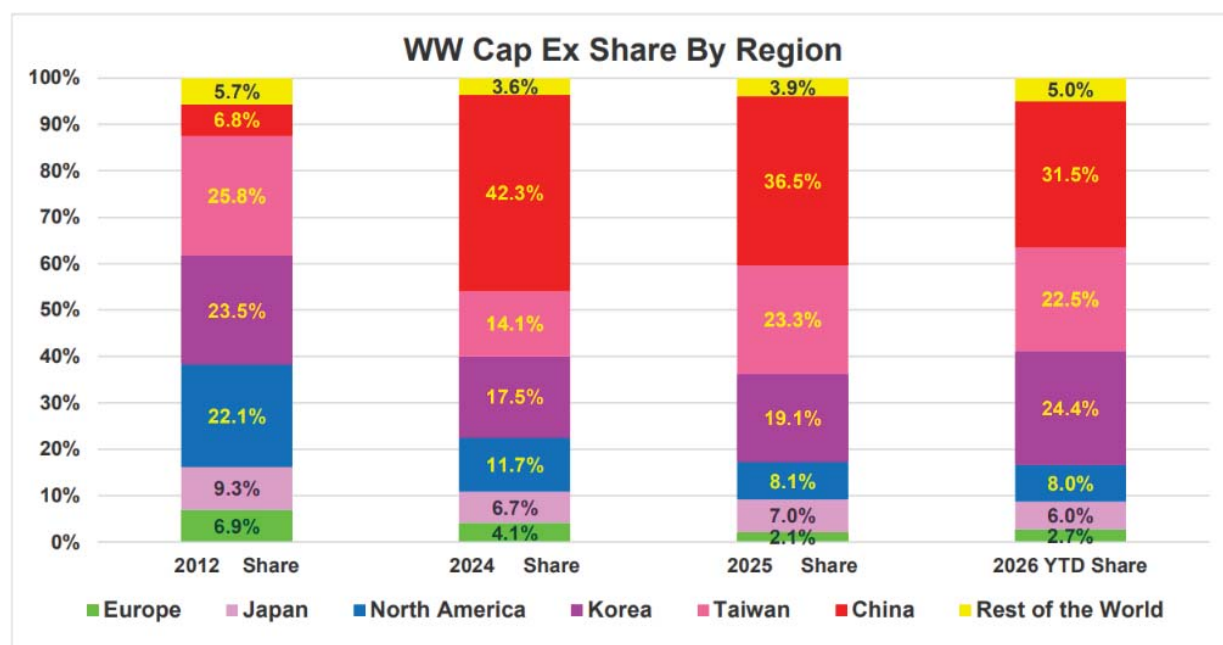


Figure 5 - Worldwide CapEx spend by region (Source: Future Horizons 2026)⁵³

A key vulnerability can also be found in back-end processes where the EU semiconductor industry relies on imports from key back-end manufacturing hubs such as China, Taiwan and Southeast Asian countries (⁵⁴). In fact, packaging and testing of mature node semiconductors are largely performed in Asia (⁵⁵). When it comes to power SiC devices, module packaging and assembly for power devices are often done outside the EU with additional exposure to non-EU sourced substrates and epitaxy. With regards to MEMS the packaging/test step is also frequently done in third countries. This reality creates significant operational risks in crisis situations and may weaken supply assurance for European OEMs, even when front-end manufacturing is located in the EU, as exemplified by the Nexperia case presented above.

(⁵²) [Commission approves €5 billion German State aid measure to support ESMC in setting up a new semiconductor manufacturing facility | Shaping Europe's digital future](#)

(⁵³) Future Horizons, The Global Semiconductor Monthly Report, April 2026.

(⁵⁴) China and Taiwan account for 58.2% of OSAT facilities and South East Asian countries for a further 12.5% Source SEMI/TechSearch International Worldwide Assembly & Test Facility Database 2025

(⁵⁵) None of the Top 20 Outsourced Semiconductor Assembly and Test (OSAT) companies in terms of revenue are headquartered in the EU. Source: SEMI/TechSearch International Worldwide Assembly & Test Facility Database 2025.

2.1.1.5 Memory chips

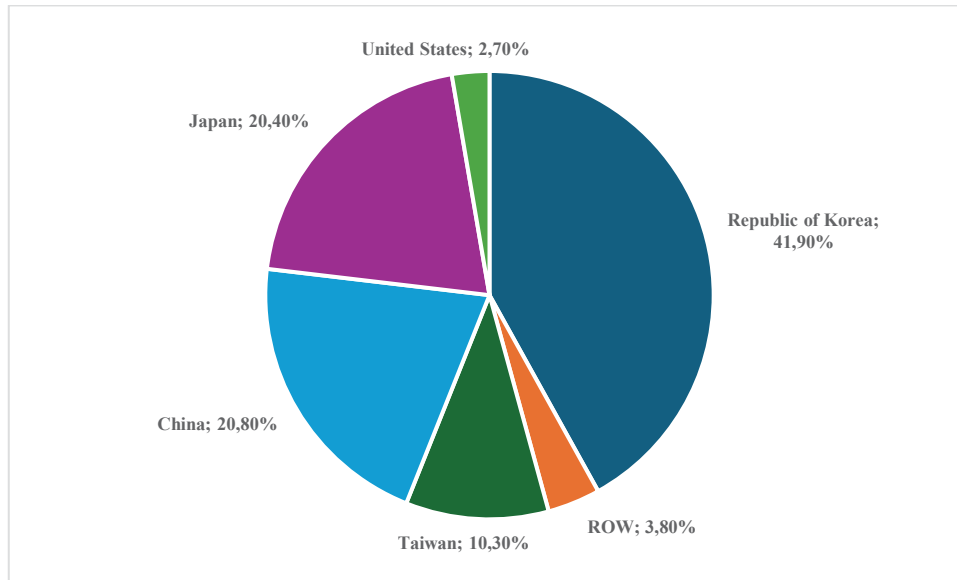


Figure 6- Memory manufacturing capacity by region in 2023 (Source: IDC)⁵⁶

Europe has no significant manufacturing capacity in memory technologies, as shown in **Figure 6**. This is a key vulnerability in light of the criticality of memory chips, particularly DRAM and HBM for AI applications.

As shown in **Figure 7**, the memory market for both DRAM and HBM is dominated by three key manufacturers: SK Hynix (South Korea), Samsung (South Korea), and Micron (United States). In the DRAM market, ChangXin Memory Technologies (CXMT) (China) is emerging as a significant player, whereas the EU has no player in this market.

In fact, South Korea, China and Japan hold 83.1% of all manufacturing capacity, with South Korea being the dominant player in this segment due to the presence of SK Hynix and Samsung.

⁵⁶ IDC, Semiconductors market data by feature size, sector and region, CNECT/2022/MVP/0084 – Second Interim Report. Risks here include economic downturns or market turbulations.

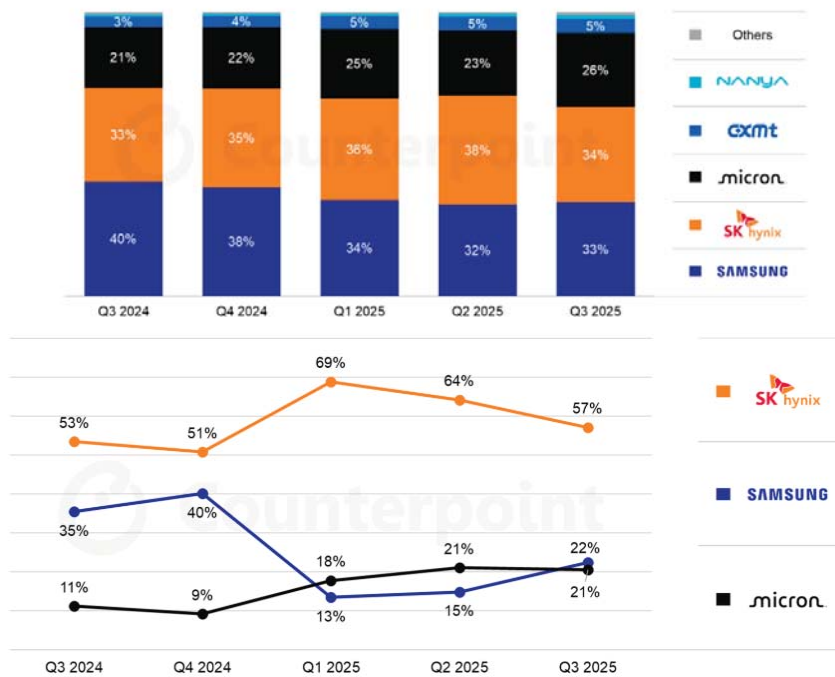


Figure 7- Global DRAM (top) and HBM (bottom) market share Q3 2024 - Q3 2025
(Source: Counterpoint)⁽⁵⁷⁾

As of 2025, the semiconductor supply chain is grappling with a severe memory-chip shortage, with downstream impacts on device makers and consumers in terms of costs and security of supply. In particular, DRAM costs have risen steeply as AI data-centre demand keeps exceeding available supply, deepening the market imbalance.

DRAM						
Discrete products	60	59	58	59	64	72
High-bandwidth memory	58	57	56	57	60	66
NAND						
Discrete products	85	80	78	80	82	84
Solid state drive	82	76	75	77	79	81

Table 1 - Share of memory demand met by current supply (%) (Source: IBS)⁽⁵⁸⁾

Demand for **high-bandwidth memory (HBM)** is rising sharply alongside AI server deployments, while supply growth is constrained by concentrated manufacturing capacity and

⁽⁵⁷⁾ [Global DRAM and HBM Market Share: Quarterly](#)

⁽⁵⁸⁾ IBS, Global Semiconductor Industry Service February 2026 - Analysis of Semiconductor Shortages.

long build-and-qualification lead times ⁽⁵⁹⁾. Manufacturers are prioritising higher-margin HBM and server-grade DRAM output, tightening availability for more commoditised DRAM and lifting pricing across adjacent segments ⁽⁶⁰⁾. This is compounded by limited advanced packaging and stacking capacity required for HBM, which implies that additional wafer starts do not translate quickly into shippable volume.

Demand for NAND used in discrete products and solid-state drives in data centre applications is also rising faster than available supply. Market analysts conclude that significantly expanding NAND capacity is challenging, as most wafer fabrication facilities are already operating near full utilisation ⁽⁶¹⁾.

As seen in **Table 1**, fab capacity for both DRAM and NAND, none of which is in Europe, is well below demand. This is expected to persist until at least 2027 and may end up delaying the deployment of AI infrastructure and data centres.

2.1.1.6 Upstream value chain segments

As further elaborated on in **Annex 4**, the Union remains exposed to persistent risks of semiconductor supply chain disruptions, while significant overdependencies are also evident in other segments of the value chain. In fact, the semiconductor industry relies on a complex network of suppliers providing inputs to each other across the value chain, from Electronic Design Automation (EDA) software, to materials, to manufacturing equipment.

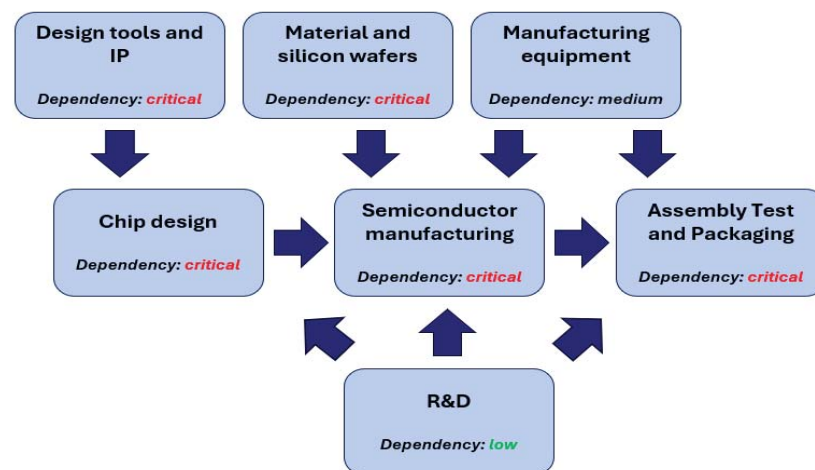


Figure 8 - European dependencies along the semiconductor value chain (see Annex 4)

2.1.1.6.1 Electronic Design Automation

EDA tools are essential for designing integrated circuits and the market is highly concentrated: Synopsys (US), Cadence (US) and Siemens EDA (EU-headquartered)

⁽⁵⁹⁾ [AI's memory chip champion has a value problem | Reuters](#)

⁽⁶⁰⁾ <https://www.trendforce.com/presscenter/news/20251029-12758.html>

⁽⁶¹⁾ IBS, Global Semiconductor Industry Service February 2026 - Analysis of Semiconductor Shortages.

accounted for over 75% of global share in 2024, rising to around 80% after Synopsys's 2025 acquisition of Ansys. EDA software is delivered as an interoperable suite spanning the full, iterative design flow (front-end verification, synthesis, physical implementation, and sign-off), making substitution difficult. The remaining market share is largely from Empyrean (China), which mainly serves domestic customers and is not a credible alternative for European industry, while smaller vendors and open-source solutions lack complete, reliable, foundry verified, end-to-end leading-edge toolchains. Europe's position is also constrained since Siemens EDA largely offers US-origin intellectual property deriving from the acquisition of Mentor Graphics, and is therefore potentially exposed to US export controls, while Synopsys and Cadence retain key advantages in hard-to-replace advanced-node tools, further reinforced by Synopsys' expanded multiphysics simulation via the Ansys acquisition.

This US-jurisdiction concentration creates geopolitical leverage, underscored for example by the Bureau of Industry and Security's (BIS) licensing requirements introduced in May 2025 for EDA tool provision to Chinese customers. A hypothetical comparable restriction against Europe would severely limit Europe's ability to design advanced chips.

2.1.1.6.2 Materials

2.1.1.6.2.1 Critical raw materials

Semiconductor manufacturing draws on materials across much of the periodic table, from relatively abundant silicon to rare earth elements. ZVEI analysis⁽⁶²⁾ indicates that the number of elements used in the semiconductor industry has quadrupled over the past thirty years (**Figure 9**), increasing exposure to concentrated supply chains for certain critical inputs.

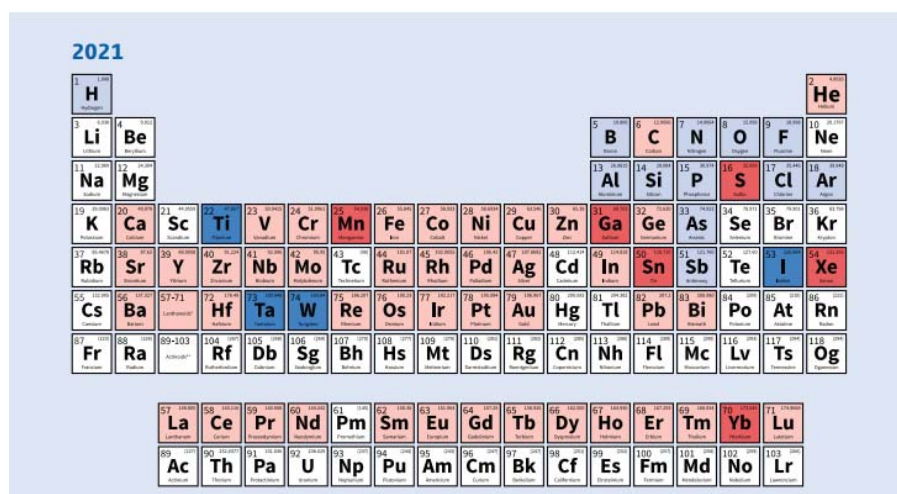


Figure 9 - Elements used in the semiconductor industry, where coloured elements denote use (Source: ZVEI)

Key examples here include gallium (Ga) and germanium (Ge). The Union is heavily reliant on China for gallium for use in integrated circuits (around 70%), with the remainder primarily

⁽⁶²⁾ [Semiconductor-Strategy-for-Germany-and-Europe | ZVEI](#) Light blue indicates elements in use in the 1980s; Dark blue indicates elements in use in the 1990s; Light red indicates elements in use in the 2000s; Dark red indicates elements in use in the 2010s.

in LEDs (around 25%) and photovoltaics. ⁽⁶³⁾ Use in power electronics is increasing. Germanium production is also concentrated in China (around 79%), followed by the United States (around 16%) and the United Kingdom (around 3%). EU demand is mainly for infrared optics (around 52%), optical fibres (around 23%) and satellite solar cells (around 12%).⁽⁶⁴⁾ Diversification appears comparatively more feasible for germanium than for gallium. Gallium enables key compound semiconductors for RF, power and optoelectronics (e.g., GaAs for high-frequency RF devices and GaN for high-power and high-voltage applications), while germanium is relevant for SiGe RF devices and silicon photonics, and features in leading-edge transistor integration.

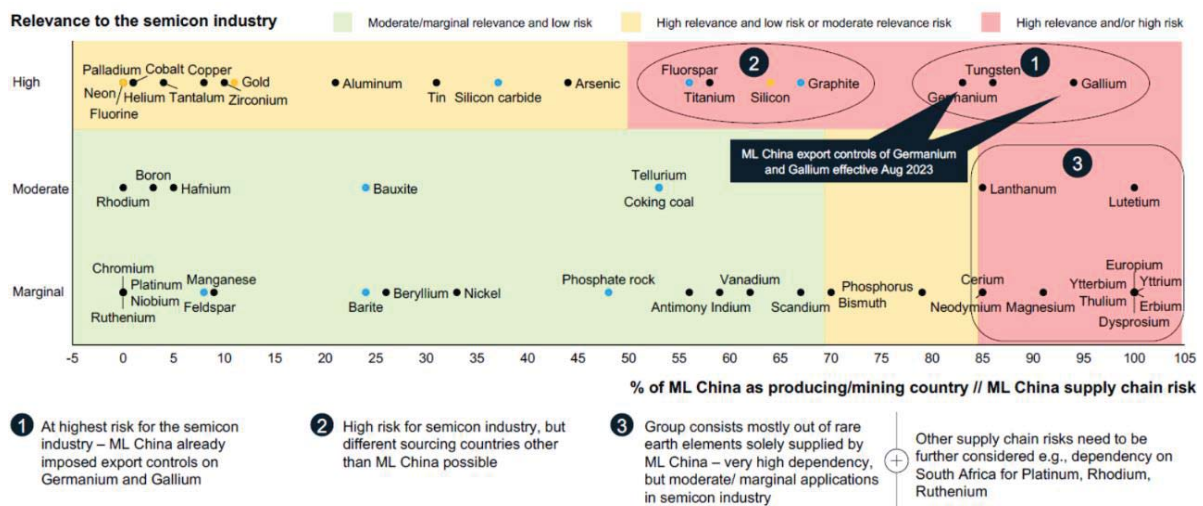


Figure 10 - Critical raw materials in the semiconductor industry (Source: McKinsey)

The examples of gallium and germanium are crucial since, as seen in **Figure 10**, Chinese dominance over these materials has allowed for the introduction of disruptive export controls on gallium and germanium (and related compounds) from 1 August 2023 ⁽⁶⁵⁾, requiring exporters to obtain licences. The measure is widely understood as part of ongoing geopolitical rivalries and trade confrontation and is viewed as a response to the tightening of restrictions on China's access to advanced semiconductor manufacturing equipment and know-how, including lithography-related controls. These export controls have resulted in prices for these raw materials to increase by around 20% ⁽⁶⁶⁾.

2.1.1.6.2.2 Compound semiconductor substrates/epiwafer

A compound semiconductor substrate is a high-purity crystalline wafer (typically SiC, GaAs or InP) that provides the mechanical base and lattice structure for compound devices and the epitaxial layers grown on top, enabling applications such as RF, power electronics and photonics. The substrate supply chain is highly concentrated and regionally segmented, with suppliers specialising by material platform; Yole Intelligence indicates Europe's merchant footprint is relatively narrow (notably Freiburger Compound Materials for GaAs and InP),

⁽⁶³⁾ [SCREEN2 factsheets_GALLIUM.pdf](#)

⁽⁶⁴⁾ [SCREEN2 factsheets_GERMANIUM-1.pdf](#)

⁽⁶⁵⁾ Yole Group, Status of the Compound Semiconductor Industry 2024.

⁽⁶⁶⁾ Yole Group, Status of the Compound Semiconductor Industry 2024.

while substantial global capacity sits in the United States and East Asia (including Japan, China and Taiwan) ⁽⁶⁷⁾. Europe's exposure is partly mitigated in SiC by increasing vertical integration: STMicroelectronics is developing in-house SiC substrates in Catania under its "Silicon Carbide Campus" (supported by an Italian Chips Act-aligned State-aid measure)⁽⁶⁸⁾ and Onsemi is expanding SiC-related capacity in Rožnov (backed by a Czech Chips Act-aligned State aid measure),⁽⁶⁹⁾ building capability inside integrated manufacturers even as the merchant base remains limited.

Immediately downstream, epiwafers add performance-critical epitaxial layers (e.g. SiC, GaAs, InP, GaN-on-SiC). Epitaxy is process-sensitive and qualification-heavy, making switching slow and costly. Yole mapping suggests the EU's identifiable merchant epiwafer presence includes Soitec (France) and Azur Space (Germany), with much of global capability concentrated outside the EU, notably in Japan, Taiwan, the United States and China.⁽⁷⁰⁾

2.1.1.6.3 Ultra-high-purity process gases and chemicals

2.1.1.6.3.1 Gases

Semiconductor manufacturing depends on ultra-high-purity process gases and precursors for deposition, etch, doping, chamber cleaning, surface treatments and lithography support. Since wafer fabrication is sequential and qualification-heavy, the loss of a single qualified molecule at the required purity can halt a process step and disrupt fab operations. Europe produces some standard, enabling gases (e.g., NH₃, Cl₂/HCl, N₂O/NO, SF₆ and certain hydrocarbons), but remains structurally dependent on external suppliers for many critical electronics specialty gases, especially those central to transistor formation and materials integration such as dopants (arsine, phosphine, diborane), key deposition precursors (silane/chlorosilanes, TEOS, germane, WF₆), and essential etch and clean chemistries (HF, HBr, NF₃, F₂/ClF₃ and fluorocarbons), with deuterium used in selected passivation/anneal steps. Upstream supply is also concentrated, with reports that over half of the EU's electronics specialty gas sources are heavily dependent on a single third country (China), amplifying disruption risk; if a critical externally sourced gas is constrained, tool uptime, cycle times and yields can deteriorate rapidly, with knock-on effects across the European value chain and downstream users.⁽⁷¹⁾

2.1.1.6.3.2 Chemicals

Semiconductor fabs rely on ultra-high-purity chemicals across all process steps (cleaning acids and bases, oxidisers, solvents, etch and deposition chemistries, and Chemical-Mechanical-Planarisation slurries), and these inputs are qualified to specific tools and recipes

⁽⁶⁷⁾ Yole Group, Status of the Compound Semiconductor Industry 2024.

⁽⁶⁸⁾ [STMicroelectronics to build integrated Silicon Carbide substrate manufacturing facility in Italy - STMicroelectronics](#)

⁽⁶⁹⁾ [Commission approves €450 million Czech State aid for Onsemi's new semiconductor manufacturing facility](#)

⁽⁷⁰⁾ Yole Group, Status of the Compound Semiconductor Industry 2024

⁽⁷¹⁾ For semiconductor process gases, the applicable specification extends well beyond a nominal purity value (for example, 99.9999%). In practice, device manufacturers and equipment suppliers jointly qualify the gas as an integrated package, encompassing its detailed impurity profile, cylinder and valve materials, packaging configuration, and the performance of the associated delivery hardware. Any change in supplier, production site, or even cylinder type typically necessitates requalification, a process that can require several weeks to months and entails significant engineering effort and test-wafer consumption.

under strict purity specifications, so shortages or quality deviations can halt production and are not quickly solved by switching suppliers.

This section focuses on three illustrative chemicals: photoresists, polysilicon and deposition precursors. Photoresists are indispensable for Deep Ultraviolet (DUV) and Extreme Ultraviolet (EUV) lithography as the light-sensitive film enabling pattern transfer. In fact, they are co-developed and tightly qualified with fabs, making substitution slow and risky. The supply base is also highly concentrated, with Japanese firms estimated at around 90% market share (notably JSR and TOK) ⁽⁷²⁾, a vulnerability highlighted by the 2019 Japan–South Korea export licensing changes for certain semiconductor materials ⁽⁷³⁾. High-purity polysilicon is the feedstock for silicon wafers: while photovoltaic-grade output is dominated by China, electronic-grade supply is more diversified with Germany’s Wacker among leading suppliers alongside firms in the United States, Japan and South Korea. However, both segments depend on metallurgical-grade silicon, whose global supply is strongly China-dependent.

Finally, Atomic Layer Deposition (ALD) and Chemical Vapour Deposition (CVD) precursors are specialised molecules enabling atomic-scale deposition for advanced transistor and interconnect structures. The market was at EUR 1.7 billion in 2024 and is projected to exceed EUR 2.3 billion by 2028. In this segment, the EU holds a leading position through Merck (DE) and Air Liquide (FR), which together account for over half of global share in advanced precursors, although Chinese suppliers are scaling capacity.

2.1.1.6.4 Manufactured inputs

Manufactured inputs such as photomasks and advanced packaging materials are design-specific, tightly qualified and supplied by a small number of producers, so disruption can delay tape-out, constrain output and raise costs. Photomasks are fundamental inputs because each product and process node requires a dedicated mask set; supply is split between captive production (by leading foundries/IDMs) and the merchant market, with captive share rising from 35% to 65% between 2008 and 2020, leaving firms without in-house capability more exposed to tight merchant capacity during upcycles.⁽⁷⁴⁾ Key merchant suppliers include Tekscend (JP), Dai Nippon Printing (JP), Photronics (US), SK-Electronics (JP) and Taiwan Mask Corporation (TW), with Tekscend also operating a Dresden facility supplying leading-edge masks (including EUV). Upstream concentration is even stronger in EUV mask blanks, where AGC (JP) and HOYA (JP) reportedly provide around 93% of supply, creating an additional bottleneck ⁽⁷⁵⁾.

Advanced packaging has similar single-point risks. Nittobo’s T-glass (low-Co-efficient of Thermal Expansion (CTE) glass cloth) used in package substrates to reduce warpage and support yield and reliability in large high-power packages (e.g., CPUs/AI/networking), is reported at approximately 90% market share. Ajinomoto’s ABF dielectric film is reported at

⁽⁷²⁾ [Japan - Semiconductors profile - Trade.gov](#)

⁽⁷³⁾ [The South Korea-Japan Trade Dispute in Context: Semiconductor Manufacturing, Chemicals, and Concentrated Supply Chains](#)

⁽⁷⁴⁾ [EUV mask technologies: evolution and ecosystem for devices](#)

⁽⁷⁵⁾ <https://finance.yahoo.com/news/asml-holding-q4-earnings-investors-124600373.html?utm>

around 95% market share and is essential for dense multilayer build-up substrates that connect advanced CPU/GPU dies to the wider system ⁽⁷⁶⁾.

2.1.1.6.5 Manufacturing equipment

Chip manufacturing is highly equipment intensive. The equipment ecosystem is fragmented and specialised, with different tool families required for distinct process steps. For simplicity, this analysis distinguishes between **front-end manufacturing** and **back-end manufacturing**.

2.1.1.6.5.1 Front-end equipment

Front-end manufacturing (Front-end-of-line (FEOL) and Back-end-of-line (BEOL) wafer fabrication) covers the processes used to create semiconductor devices and interconnects on a silicon wafer, including transistor formation, deposition of dielectric and metal layers, lithographic patterning, etching, and planarisation.

In front-end equipment, Europe's most significant position is in **lithography**, where EU-based suppliers account for approximately **92%** of the market. This is a strong lever in a critical process step, but it is highly concentrated in a single segment and depends on coordination with the United States.

By contrast, the broader front-end wafer-fabrication equipment market is led by the **United States (~40%)**, followed by **Japan (~28%)** and **Korea (~24%)**, with the EU remaining in single digits. This indicates that Europe's influence over upstream manufacturing capacity is not commensurate with its strength in lithography. **Further analysis of the different segments of front-end equipment is provided in Annex 4.**

2.1.1.6.5.2 Back-end equipment

Back-end manufacturing (assembly, packaging and test) covers the final steps that convert processed wafers into finished, packaged devices ready for integration into electronic systems. It includes wafer dicing and thinning, die attach and interconnect, encapsulation (moulding and sealing), inspection and handling, and final electrical test. Packaging provides electrical connectivity for signals and power, supports heat dissipation, and protects the device to ensure long-term reliability.

The back-end equipment market is concentrated and increasingly dominated by Japan. In 2023, Japan accounted for **48%** of the global market (up from **33%** in 2017) and held a dominant position in dicing equipment (**>92%**). Japan also led packaging equipment overall (**51.4%**) and was particularly concentrated in moulding and sealing systems (**75.3%**). Singapore's share declined to **21%** (from **35%** in 2017), reflecting its specialisation in bonding equipment, especially wire bonding, where it accounted for **>81%** of global sales; Singapore also held **97%** of integrated assembly systems (with the remaining **3%** held by Grohmann Engineering, Germany). The EU held **14.5%** of the global market in 2023 (down from **16%** in 2017), with limited presence in several high-throughput segments but material

⁽⁷⁶⁾ <https://www.nittobo.co.jp/eng/business/electronicmaterials/index.htm>

positions in selected bonding and finishing categories. **Further analysis of the different segments of back-end equipment is provided in Annex 4.**

2.1.1.7 Conclusion

Across the semiconductor value chain, the Union remains exposed to material supply chain disruption risks and to persistent, structurally embedded dependencies on third country suppliers. In EDA, market concentration in US-jurisdiction providers and the limited substitutability of interoperable tool suites constrain the Union's strategic autonomy and create exposure to potential extraterritorial measures. In materials, vulnerabilities span upstream from critical raw materials with highly concentrated global production, through compound semiconductor substrates and epiwafers where merchant capacity is limited and regionally segmented, to ultra-high-purity gases and chemicals that are qualification-intensive and therefore difficult to substitute at short notice. While selected European strengths exist, they do not eliminate wider reliance on external supply bases for multiple process-critical inputs, including those relevant to lithography.

In manufactured inputs, design-specific and tightly qualified products such as photomasks and advanced packaging materials exhibit pronounced single-point failure risks, reinforced by high upstream concentration in certain enabling materials. In manufacturing equipment, the Union's strong position in lithography constitutes a strategic asset but is not matched by comparable capability across the broader front-end tool ecosystem, while back-end segments remain concentrated in non-EU suppliers. Overall, this configuration implies that a disruption or restriction affecting a limited number of concentrated upstream inputs can propagate rapidly across design, fabrication and packaging activities, with consequential impacts on European industrial capacity, downstream users and broader resilience objectives.

2.1.2 P2: Insufficient crisis preparedness capabilities

Since 2023, as will be elaborated on further in the problem drivers, geopolitical tensions have increased and several events have highlighted the vulnerability of the EU's semiconductor supply chain – including export controls on critical raw materials, the now withdrawn AI Diffusion Rules by the US ⁽⁷⁷⁾ and the recent Nexperia case ⁽⁷⁸⁾.

Despite the monitoring and crisis-response tools established under Pillar III of the Chips Act, significant gaps remain in the Union's ability to effectively address semiconductor supply chain crises. The EU still lacks sufficiently developed mechanisms, tools and institutional capacities to anticipate, assess and respond to disruptions in a timely and coordinated manner. Evidence gathered in the evaluation of the Chips Act ⁽⁷⁹⁾ suggests that to capture system-wide risks, the scope of crisis response mechanisms needs to be extended to cover base materials,

⁽⁷⁷⁾ [Federal Register: Framework for Artificial Intelligence Diffusion](#)

⁽⁷⁸⁾ [Minister of Economic Affairs invokes Goods Availability Act | News item | Government.nl](#)

⁽⁷⁹⁾ During the evaluation, several interview partners and workshop participants considered the original design of the Chips Act with its focus on front-end fabrication to be misaligned with the current vulnerabilities, overlooking dependencies in substrates, specialty chemicals, advanced packaging, RF and power modules, PCBs and EMS (see page 48 and 49 of the Evaluation report).

substrates, materials, packaging, assembly, downstream electronics, and end-user industries. Not including these elements allows vulnerabilities in the value chain to go unnoticed, limiting the relevance of crisis response for downstream and end-user sectors, and eventually customers ⁽⁸⁰⁾. Outside a formally activated crisis, the Union currently has no binding mechanism to gather information directly from undertakings, leaving the Commission without the means to assess ad hoc supply chain situations, identify emerging bottlenecks, or monitor dependencies in real time before they reach crisis activation thresholds.

The semiconductor value chain remains highly opaque and fragmented to public authorities, and the lack of device-level data makes it difficult to understand and predict global and European supply dynamics. **Pillar III's effectiveness is somewhat constrained by limited Union level visibility into Europe's semiconductor supply chains functioning and resilience of their operations**, thereby weakening crisis preparedness. Despite improved coordination through the European Semiconductor Board ⁽⁸¹⁾ and initial early warning measures, monitoring remains insufficiently integrated across value chain segments such as materials, equipment, design tools, and downstream users ⁽⁸²⁾. Fragmented data sets restrict the Union's ability to anticipate disruptions, leaving initiatives under Pillar III with only partial system-level visibility.

Work under the European Economic Security Strategy ⁽⁸³⁾ illustrates the limitations of the current system: as part of a risk assessment exercise ⁽⁸⁴⁾, the Commission and Member States attempted to assess vulnerabilities in the supply of advanced semiconductor technologies and to gather data through surveys, workshops and interviews covering chip use, stock levels, suppliers, customers and user industries. However, the information collected by the Commission and Member States was limited since industrial stakeholders were not required to provide data on a mandatory basis. As a result, the joint risk assessment could not deliver the sufficiently detailed insight needed for a thorough understanding of the structure of the supply chain, or for the identification of critical dependencies and potential bottlenecks.

Given the global nature of semiconductor supply chains, no single Member State can obtain on its own the insights needed to assess risks or manage disruptions. Supply chains naturally involve cross-border dependencies, which means that national monitoring systems would be unable to address systemic EU risks creating potential blind spots and gaps in the data. Analysis of the Nexperia case has shown impacts in the automotive sector of several different Member States ⁽⁸⁵⁾.

Overall, in the absence of enhanced monitoring capacities and crisis preparedness measures, the Union is unable to better anticipate disruptions, assess risks, coordinate responses and does not possess adequate tools to mitigate the impact of future crises.

⁽⁸⁰⁾ Annex 2

⁽⁸¹⁾ [Register of Commission expert groups and other similar entities](#)

⁽⁸²⁾ Annex 2

⁽⁸³⁾ [Press corner | European Commission](#) – An EU approach to enhance economic security.

⁽⁸⁴⁾ [Communication on European economic security.pdf](#)

⁽⁸⁵⁾ [Europe's carmakers face 'devastating' chip crisis as Nexperia supply crunch continues](#)

2.2 What are the consequences?

The aforementioned challenges provoke considerable **economic costs that come from dependence and a lack of resilience.**

As the EU becomes increasingly reliant on foreign semiconductor supplies, it grows more vulnerable to external coercion and risks a potential ‘weaponisation’ of its supply chain dependencies. Without a strong industrial base in semiconductor design and manufacturing, the EU will not capitalise on its strong R&D ecosystem through productivity gains and the industrialisation of research.

User industries in the EU face significant uncertainties in their supply chains, leading to increased inventories and reduced investment which render manufacturing in the EU less competitive. Moreover, supply chain dependencies expose the EU to heightened geopolitical and security risks, particularly in crisis scenarios where access to critical technologies may be restricted or prioritised elsewhere. They may also affect the EU’s autonomy in security and defence, with the defence industry unable to secure reliable access to vital electronic components, undermining long-term strategic autonomy and the credibility of EU policy commitments.

In summary, persistent dependence on non-EU semiconductor technologies constrains the EU’s ability to exercise technological sovereignty, limiting its control over critical standards, architectures, and its ability to shape future innovation pathways. Even with the investments triggered by the Chips Act, critical gaps remain which hamper the development of crucial infrastructure such as AI datacentres.

2.3 What are the problem drivers?

The problems described above emerge from a mixture of external drivers, structural weaknesses of the European semiconductor sector, and the general framework for doing business in the EU which affect the competitiveness of the semiconductor industry.

2.3.1 *PD1: Geopolitical tensions leading to disruptions and weaponisation of semiconductor supply chains*

Amid rising geopolitical tensions, semiconductors have become a strategic technology, driving heightened global competition and prompting third countries to adopt increasingly aggressive industrial and trade policies across the semiconductor value chain and its end markets. While geopolitical tensions predate the adoption of the first Chips Act, a notable shift since its entry into force has been the sustained weaponisation of the supply chain. Furthermore, an escalation in hostilities can have an indirect impact on trade flows of semiconductors due to shocks on logistics.

As the semiconductor industry takes a more central role in economic security policy considerations worldwide, governments increasingly view secure access to semiconductors as a prerequisite for technological leadership, industrial competitiveness, national security and resilience. This shift has translated into a marked escalation in State intervention in the industry, which is now being felt more acutely since the adoption of various laws and subsidy schemes in all major semiconductor producing regions.

At the heart of the geopolitical dimension of the semiconductor industry is Taiwan that produces over 90% of the most **advanced logic semiconductors**, with its most prominent company TSMC being the leader in semiconductor foundry services, holding 67% of the global market share in Q4 2024.⁽⁸⁶⁾ Taiwan is also an important source of mature-semiconductors, chip design and packaging.

Furthermore, rising frictions in the South China Sea over conflicting territorial claims also raise the risk of potential blockades and major disruptions. If a conflict were to materialise, this could result in a severe shortage of a broad range of semiconductors for EU companies, including the disruption or loss of access to advanced semiconductors such as AI chips and could lead to an estimated global GDP loss in the order of 10%.⁽⁸⁷⁾

Against this backdrop, the US, China, Japan and South Korea have each introduced substantial support schemes for the semiconductor industry, such as subsidy programmes and tax incentives, aimed at expanding domestic advanced manufacturing capacity and design. Both the US and China have implemented or explored restrictive trade measures, including export controls on advanced chips and related technologies. These policies indicate a broader move towards more state involvement in the management of semiconductor supply chains and reflect a growing recognition of their geopolitical and economic significance.

The absence of coordinated funding by the Union and Member States limits the possibility for EU-level policy steer of project selection, to align investments with identified European dependencies and ensure complementarity of investments. In a public consultation, interview partners and workshop participants also pointed to room for improvement in terms of coordination processes between the EU and national levels⁽⁸⁸⁾.

This subsidy race is drastically increasing manufacturing capacity worldwide, as Governments compete to attract new fabs and expand existing ones through massive public support packages. The result is a wave of capacity announcements that risks creating global overcapacities in mature and mainstream chips, intensifying price competition and further distorting the global level playing field, placing European semiconductor firms at a competitive disadvantage⁽⁸⁹⁾.

Furthermore, from a trade policy perspective, the ongoing geopolitical competition has resulted in disruptions to open, rules-based trade, which has been starkly felt by the semiconductor industry. The withdrawn US Framework for Artificial Intelligence Diffusion illustrate how technological dependency exposes the EU to supply chain vulnerabilities and risks of economic coercion. Such a policy would have consequently fragmented the internal market into Tier 1 and Tier 2 classes and resulted in certain Member States having constrained access to AI chips and systems⁽⁹⁰⁾. This illustrates how the weaponisation of

⁽⁸⁸⁾ Annex 4.2 and 5.2

⁽⁸⁸⁾ Annex 4.2 and 5.2

⁽⁸⁸⁾ Annex 4.2 and 5.2

⁽⁸⁹⁾ [Beyond overcapacity: Chinese-style modernization and the clash of economic models | Merics](#)

⁽⁹⁰⁾ [Joint Statement by Executive Vice-President Henna Virkkunen and Commissioner Maroš Šefčovič | European Commission](#)

export controls as geopolitical tools can lead to concrete risks for security and competitiveness.

Conversely, recent restrictions from China on exports of gallium and germanium ⁽⁹¹⁾ risked undermining the production of vital power electronics components, RF and communications equipment and optoelectronic devices, which are also European strengths. The interruption in supply of electronic components from Nexperia has illustrated how in the current context, dependencies even in mature technologies can disrupt European user industries, particularly the automotive sector.

2.3.2 PD2: Underdeveloped European semiconductor design and manufacturing capabilities

Compared to the Union's share of global economic activity, the semiconductor industry in the EU remains underdeveloped in both design and manufacturing, limiting Europe's ability to compete in high-growth segments and increases its dependence on third countries for critical technologies.

When it comes to design, BCG-SIA estimates indicate that the design stage captures over 50% of total value-added in the semiconductor value chain. Yet, the EU **has a limited number of fabless companies** and none in the top 40 in terms of revenues, with the European market share being **less than 1%** ⁽⁹²⁾. The EU commands only a very small share of the global design talent pool, with roughly 4% of the worldwide design workforce. This critical bottleneck in human capital severely limits the EU's ability to capture value in the highest-growth segments.

The EU's position is set to diminish further as the share of European design starts is projected to fall further by the end of the decade from 14.72% in 2018 to 11.75% in 2030 ⁽⁹³⁾. Furthermore, chip design requires the use of tools and IP originating mostly from US companies. Consequently, European chipmakers rely on US-origin IP and software that are subject to export licenses whose terms are set by third countries. This critical dependency underscores the importance of Union-level action in the field of EDA and IP.

The Union's semiconductor industry is also shaped by the long-standing predominance of IDMs who design and manufacture chips, focusing mostly on analogue and mixed-signal chips, microcontrollers and custom logic in mainstream technology nodes. In fact, IDMs account for roughly 97% of the EU's semiconductor manufacturing revenue. Their vertically integrated model has historically aligned well with European end-markets, particularly automotive and industrial automation. However, this approach has its limitations and becomes unsustainable at more leading-edge technologies, explaining a global industry shift towards the fabless-foundry model, with firms specialising in either design or manufacturing due to

⁽⁹¹⁾ [China gallium, germanium export curbs kick in; wait for permits starts | Reuters](#)

⁽⁹²⁾ IDC, Semiconductors market data by feature size, sector and region, CNECT/2022/MVP/0084 – Second Interim Report.

⁽⁹³⁾ IBS, Global Semiconductor Industry Service 2023 – Second in-depth analysis report.

high costs. This model has become the dominant configuration for advanced logic and high-performance chips.

Therefore, in a context where the EU's **fabless ecosystem is underdeveloped**, there is limited market incentive for foundries to deploy manufacturing capacity in the EU. This is particularly the case for leading-edge semiconductors that are vital for AI chips utilised in AI gigafactories and factories, but also other lead markets and applications as explained above. Without a dense cluster of design firms generating consistent, high-value tape-outs, the business case for locating cutting-edge fabs in the Union remains weak. Foundries follow the gravity of demand: where design pipelines are active, risky and expensive nodes become commercially viable. Where those pipelines are sparse or fragmented, even generous public incentives struggle to outweigh the lack of a sustained customer base.

In 2023, according to estimates by International Data Corporation (IDC), the EU had 8.1% of global front-end manufacturing capacity, a share projected to remain constant until 2030 ⁽⁹⁴⁾. When analysing this front-end footprint, one can see that here the EU has limited leading-edge capacity - which is all attributable to the Intel fab in Leixlip (Ireland), and sub-optimal levels of capacity for mainstream and legacy nodes. In back-end manufacturing, the EU largely relies on facilities in South-East Asia and European industry only keeps a small manufacturing footprint in the EU.

The current industrial structure is shaped by the needs of the EU's main industrial sectors, in particular automotive and industrial automation. Here, production is largely focused on more mature technologies such as sensors, microcontrollers and analogue circuitry, which while crucial, are largely lower-margin and are generally more sensitive to the cyclicity of the industry. When it comes to higher value-added segments of semiconductor manufacturing and design, the Union has a limited role. A direct consequence of being absent from leading-edge manufacturing is that the EU has also lost much of the skilled human capital needed to develop these capabilities domestically. **This imbalance leaves the EU vulnerable to geopolitical tensions and economic coercion (see section 1.5.1. concerning the first problem driver) over the manufacturing of advanced semiconductor technologies that underpin AI, telecommunications, security and defence.**

Cost structures further constrain the EU's competitiveness in manufacturing. As seen in **Figure 11**, fabrication costs in the US or Japan are approximately 16% lower than in the European Union. The gap with China, Taiwan and South Korea is even larger, with the cost of constructing a fab in South Korea estimated at approximately **half the cost of an equivalent facility** in the EU.

Semiconductor manufacturing in the EU faces a structural cost disadvantage driven by four main factors: capital, labour, land and energy. **Capital costs** represent the largest share of total fab production costs and are higher in the EU than in most competing regions, due to higher cost of equity, elevated country risk premiums, and the smaller scale and lower

⁽⁹⁴⁾ This stable share must be viewed against a global backdrop in which manufacturing capacity is expanding rapidly. In absolute terms the manufacturing capacity of the Union has increased by over 38%, from 1.07 million wafers per month in 2023 to around 1.48 million wafers per month by 2030 if all investments materialise.

liquidity of European semiconductor firms. **Labour costs** are also structurally higher when measured in unit terms, as relatively high employer social security contributions and lower labour productivity offset the EU's slightly lower nominal wages. **Land costs** account for a smaller share of total costs and place the EU in an intermediate position internationally, being cheaper than in some Asian economies but more expensive than in the US and China.

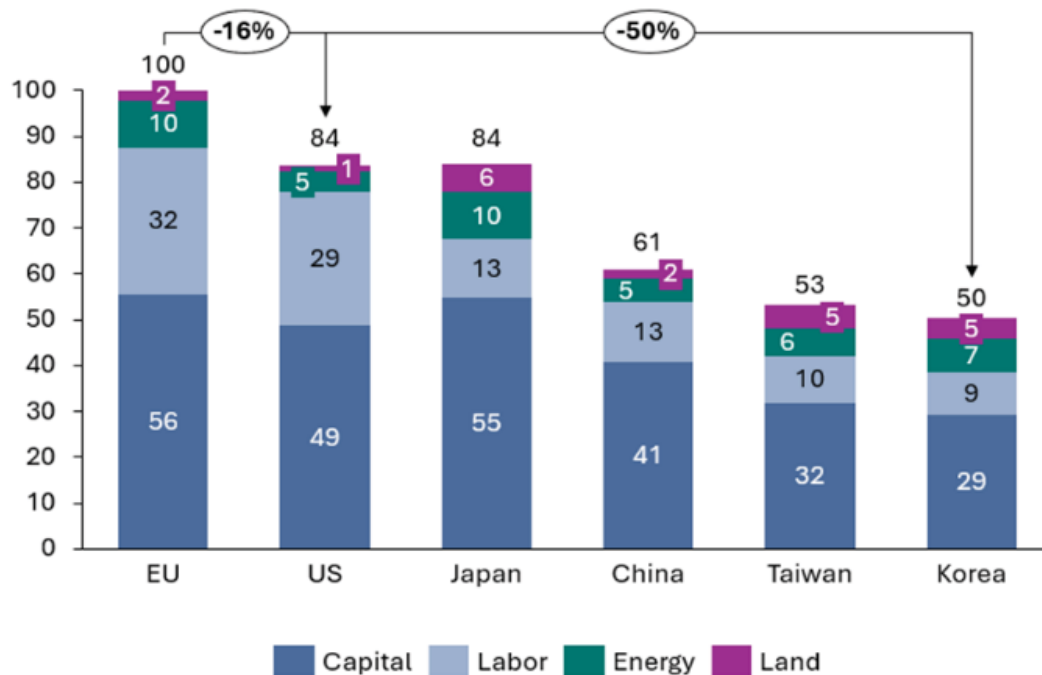


Figure 11 - Overall fabs production cost gap across countries (normalized EU = 100) Source: Yole/Decision⁹⁵

When it comes to energy, prices are also significantly higher in the EU, with electricity costs being roughly double those in the US and China in recent years. ⁽⁹⁶⁾ Beyond the initial capital expenditure, this drives up the costs of running fabs in the EU significantly. In addition, other regions benefit from denser supplier ecosystems, shorter supply chains and larger pools of specialised talent, all of which lower production and logistics costs.

Taken together, these factors result in a structural weakness in the EU's manufacturing capabilities. **This reality leaves the EU with limited capacity to compete in fast-growing segments and increasingly exposed to critical dependencies across technologies, from mature to leading-edge.** Furthermore, emerging fabless start-ups in the EU, active in segments such as AI chips, have to rely on fabrication in third countries. This dependence not only exposes them to geopolitical and export-control risks, but also lengthens development cycles, increases costs and reduces their ability to iterate rapidly. It also deprives the EU of the feedback loops between design and manufacturing that typically drive innovation clusters, making it harder for local start-ups to scale or anchor subsequent production in the Union. A

⁽⁹⁵⁾ Decision Etudes & Conseil and YOLE Group, Competitiveness of the EU semiconductor manufacturing industry, Nov.2025.

⁽⁹⁶⁾ Decision Etudes & Conseil and YOLE Group, Competitiveness of the EU semiconductor manufacturing industry, Nov.2025.

successful approach to change this situation, in the words of one participant of the evaluation, “must not only help develop production capabilities but, more fundamentally, it must create the framework conditions for industry to create [...] an end-market for more semiconductors 'made in the EU'.”⁽⁹⁷⁾

The Union’s competitiveness challenge, combined with geopolitical pressures, underscores the urgency of **Union level action to accelerate permitting processes for Pillar II facilities, i.e. eventual integrated production facilities (IPF)/open EU foundries (OEF), while maintaining high environmental standards.** Approval procedures in the EU are significantly slower than in competing regions: industry reports indicate **permitting approvals take 10-18 months in the EU, compared with about 6 months in South Korea and Taiwan** and less than one month in certain other jurisdictions.

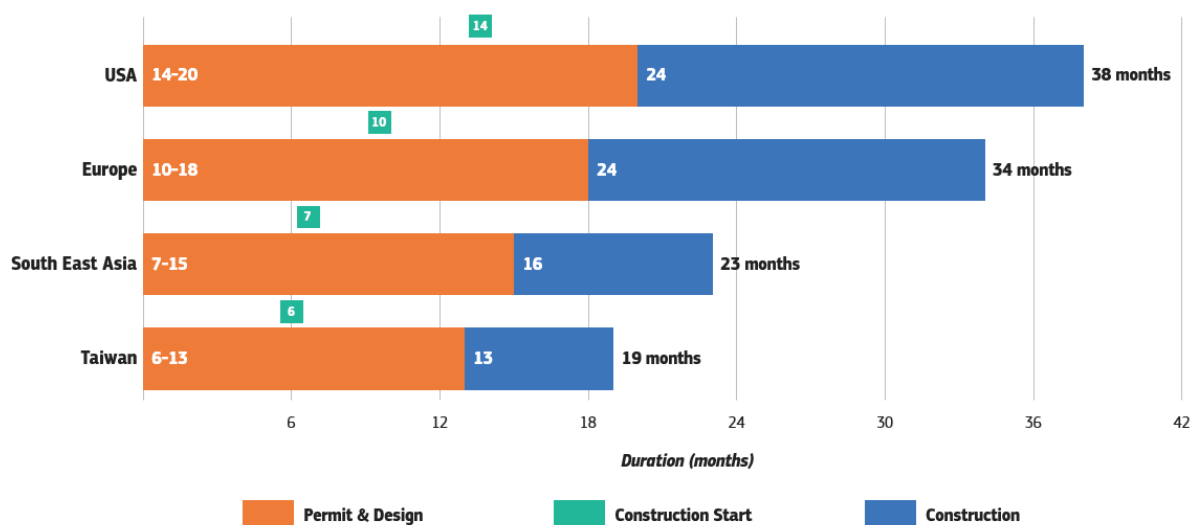


Figure 12 - Average duration of projects for building wafer fabs

Results from the evaluation align with these shortcomings. Respondents in the open public consultation highlighted insufficient manufacturing capacity, limited investment instruments, shortages of skilled labour, and weak domestic demand from hyperscalers and AI companies as the principal obstacles in the development of an EU AI-chip value chain.⁽⁹⁸⁾ A lack of venture capital and risk finance was reported as a particular constraint for design firms, while IDMs and other production-oriented firms pointed to lengthy permitting procedures and high energy costs as major impediments⁽⁹⁹⁾.

2.3.3 PD3: Insufficient support and advanced facilities for scaling up innovative start-ups

The EU’s semiconductor sector suffers from a ‘lab-to-fab gap’, which describes the struggles to translate scientific excellence into products that are successful on the market. Despite

⁽⁹⁷⁾ Annex 2 Section 5.

⁽⁹⁸⁾ Annex 2 Section 4

⁽⁹⁹⁾ Annex 2 Section 5.2.

remaining very competitive in terms of semiconductor R&D and scientific publications (**Figure 13**), European semiconductor manufacturers have steadily lost market share (**Figure 14**).

This loss in market share can be largely explained by the lack of market dynamism in the European semiconductor industry, with long time incumbents still dominating the market. In fact, all major players in European semiconductor manufacturing have their roots in companies founded over 70 years ago. ⁽¹⁰⁰⁾ In device manufacturing, the product lines of European players are based on largely mature technologies. This is an anomaly given the substantial volume of cutting-edge semiconductor research produced within the Union, which should provide a strong foundation for the emergence of new European technologies on the market.

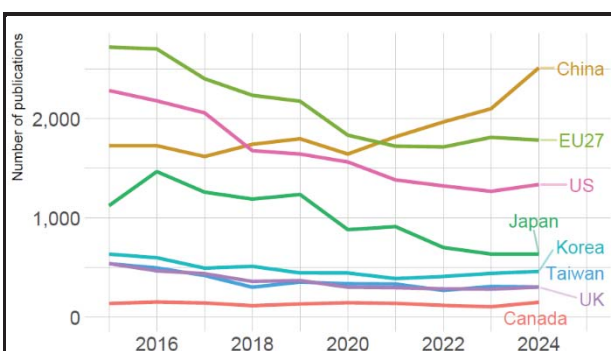


Figure 13 - Scientific publications related to semiconductors (Source: Open Alex article publications)

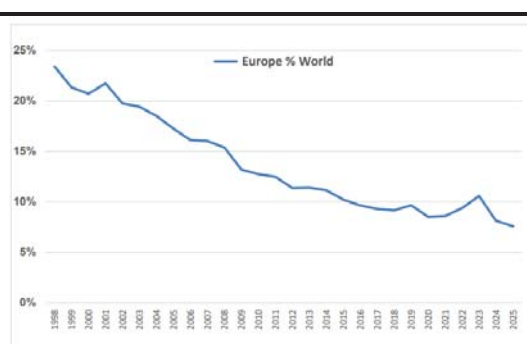


Figure 14 - European market share in the semiconductor industry (Source: Future Horizons May 2025)

This lack of dynamism is related to insufficient support for innovative start-ups in scaling up, a point that was also highlighted by the **Draghi and Letta reports**. ⁽¹⁰¹⁾ The results of the evaluation support this observation: participants in several workshops identified mobilising private capital, particularly European venture capital, as a structural bottleneck for the support of semiconductor design firms. ⁽¹⁰²⁾

According to a recent European Investment Bank report ⁽¹⁰³⁾, European deep-tech startups raised only 20% of the capital raised by their US peers in 2023. Here, the EU performs better in seed and early-stage funding, reaching over 50% of US levels, but this falls to around 10% for scale-up rounds, which are the stages at which semiconductor firms can focus on industrial deployment.

⁽¹⁰⁰⁾ Referring to the 4 European IDMs i.e. STMicroelectronics, Infineon Technologies, NXP, Robert Bosch.

⁽¹⁰¹⁾ [Enrico Letta \(2024\), Much more than a market](#)

[Mario Draghi. \(2024\). The future of European competitiveness: In-depth analysis and recommendations \(Part B\).](#)

⁽¹⁰²⁾ Annex 2 Section 5.3.

⁽¹⁰³⁾ European Investment Bank publications: “The scale-up gap: Financial market constraints holding back innovative firms in the European Union” (July 2024).

Furthermore, only about 5% of global venture capital is raised in the EU, compared to 52% in US and 40% in China, meaning that much of the equity of European deep-tech companies is owned by non-European investors. Venture financing experts widely interpret this as a direct consequence of the persistent fragmentation of the European financial markets and the absence of a real Capital Markets Union, which limits the liquidity available for equity financing. This combined with a more risk-averse culture in the EU, limited insight into the semiconductor industry among investors, as well as fragmented markets and complex regulations make scaling-up across borders more difficult. Facing such challenges, start-ups are enticed to accept financing from the US or Asia, move their HQ to third countries, or are acquired by non-European firms to ensure industrialisation of their IP and financial returns, leading to the loss of strategic technologies, talent and future value creation for the EU.

Besides risk capital, the lab-to-fab gap could also be closed by more interaction between SMEs and academia. Workshop participants as well as interview partners report that SME access to the pilot lines established under Pillar I turned out to be difficult and prohibitively expensive. ⁽¹⁰⁴⁾

Another relevant driver is the lack of leading-edge manufacturing and advanced packaging facilities in the EU, which are essential to bridge the so-called ‘lab-to-fab’ gap. Around semiconductor manufacturing hubs, dense ecosystems tend to emerge, attracting suppliers of equipment, materials, chemicals, as well as design houses, fabless as well as system companies from key user industries. This is because physical proximity shortens feedback loops, accelerates ‘learning by doing’ and enables tight collaborations on design-technology co-optimisation, rapid prototyping and qualification, which are crucial advantages for industrialisation, especially for smaller companies, as they reduce coordination costs and shorten development cycles. A clear example of such dynamic is the Hsinchu Science Park developed in Taiwan around TSMC, brimming with design houses, system companies and technology organisations, thus creating short idea-to-product cycles. However, linkages to industry are also required in the other direction, to the industrial users of advanced chips which are often not located in Europe. This leaves chip design firms without anchor customers a strong home market according to the public consultation. ⁽¹⁰⁵⁾

In this context one can also observe that, since the 1980s, European policy initiatives (such as ESPRIT, JESSI, MEDEA, CATRENE, ECSEL, KDT and now Chips JU) have predominantly focused on research and development programmes, which has led to core R&D strengths and multiple research centres of excellence across the EU. However, as regards financial support to commercial undertakings and to industrial manufacturing facilities, the European regulatory framework, designed to support an effectively functioning Single Market while limiting distortions within the internal market, has in practice allowed public intervention on R&D but much less in support for its market exploitation and industrial deployment. This has over time left the EU at a competitive disadvantage vis-à-vis prevailing practices to offset massive capital expenditures in other regions, and has, in effect, contributed to the underdevelopment of high-tech industrial deployment in Europe.

⁽¹⁰⁴⁾ Annex 2

⁽¹⁰⁵⁾ Annex 2

Taken together, the above highlights the Union's limitations in financing advanced industrial facilities, via targeted public support schemes, to enable innovative semiconductor ventures to scale up in the EU and to contribute to its industrial competitiveness.

2.3.4 PD4: Lack of demand for European advanced chips from user industries

The EU is a significant market for semiconductors. According to recent estimates from IBS, the EU accounts for around **13% of global direct semiconductor demand**.⁽¹⁰⁶⁾ This figure refers to **components** shipped to European system companies, which in turn integrate them into intermediate goods or finished products. However, it does not capture the larger volume of chips already **embedded in imported finished products** that reach European customers, such as smartphones, laptops, servers, networking equipment or cloud infrastructure. This share is estimated to be at around **20% of global semiconductor demand**.

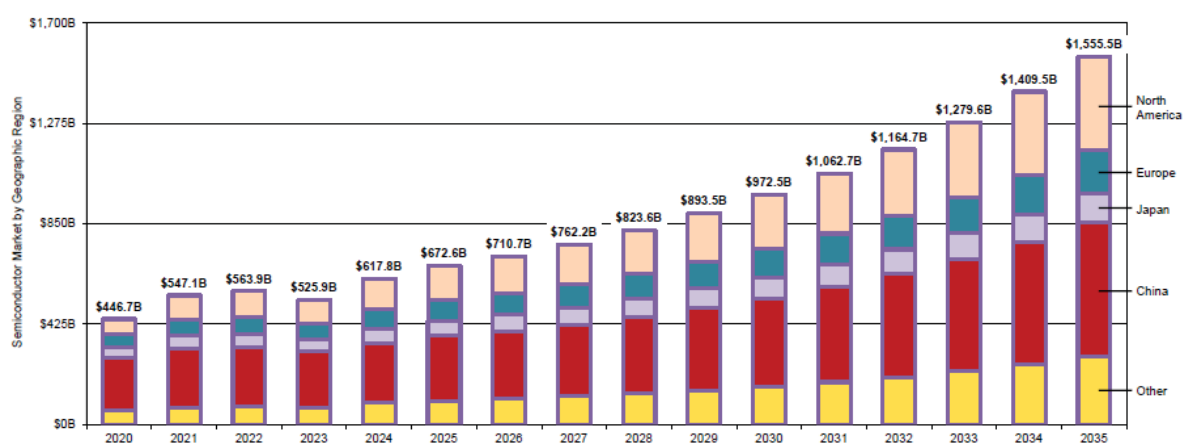


Figure 15 - Forecast of semiconductor demand by region. (Source: IBS, August 2025)¹⁰⁷

Furthermore, the EU has a particularly distinctive direct demand profile, where semiconductor purchases by firms operating in the Union are oriented towards the **automotive** and **industrial** sectors.⁽¹⁰⁸⁾ In 2023, the Union accounted for 39.4% of global demand for automotive semiconductors and 23.1% for industrial semiconductors.⁽¹⁰⁹⁾ This reflects the EU's strengths in power devices, microcontrollers, sensors and analogue components, which underpin many of the Union's industrial and automotive technologies. By contrast, the Union hosts relatively few OEMs or Tier 1 suppliers for consumer electronics, personal computing devices or hyperscale cloud infrastructure. Hence, while direct internal demand is skewed towards mature-node chips, much of its consumption of **leading-edge** semiconductors comes embedded in **imported systems**, making it hard for the EU to drive the industrial demand needed to develop an advanced fabless-foundry ecosystem purely on market grounds.

⁽¹⁰⁶⁾ Demand from firms such as OEMs and Tier 1s that purchase chips as intermediate inputs.

⁽¹⁰⁷⁾ IBS, Global Semiconductor Industry Service, Semiconductor Market by Application Part 1, February 2025.

⁽¹⁰⁸⁾ EU's strengths and weaknesses in the global semiconductor sector, Publications Office of the European Union, Luxembourg, 2025, https://data.europa.eu/doi/10.2760/6302476_JRC141323.

⁽¹⁰⁹⁾ IDC, Semiconductors market data by feature size, sector and region, CNECT/2022/MVP/0084 – Second Interim Report.

The biggest change in EU demand patterns in recent years was the rapid demand growth for AI chips. The **datacentre/AI/cloud** segment of the semiconductor market already represents over 18% of European semiconductor consumption and is expected to reach around **26% by 2030**.⁽¹¹⁰⁾

However, an estimated 96% of the semiconductor market for datacentres is captured by US-owned companies⁽¹¹¹⁾ which contributes to a significant trade deficit between the EU and the US and creates critical dependencies on third-country suppliers in what is currently the fastest growing economic sector. Moreover, the US administration, despite rescinding the Framework for Artificial Intelligence Diffusion, is now advancing on an AI Action Plan built around exporting a “full stack” solution of chips, models, software and standards with strict conditionality. This implies a **significant strategic risk for the EU’s sovereignty, as its AI infrastructure and software** will potentially be structurally dependent on extraterritorial US jurisdiction and policy choices.

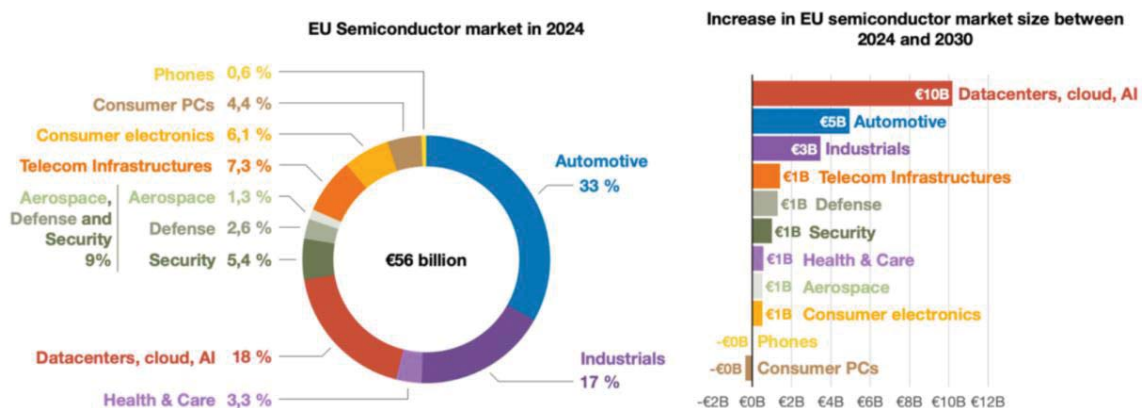


Figure 16 - Semiconductor consumption and absolute increase in market size by application area
(Source: Decision based on Eurostat and WSTS)

Competitive pressure in **mature** and **mainstream** technology nodes has intensified as third countries expand subsidised production capacity. For example, China has substantially increased investment in mature-node manufacturing as part of its self-sufficiency strategy and complemented it with ‘China for China’ policies that prioritise domestic sourcing.⁽¹¹²⁾ These developments have added pressure in segments where many European companies operate. Global semiconductor demand, however, is growing most rapidly in segments where the EU currently has limited direct presence.

Strong investment in data centres, AI systems and cloud services is driving demand for high-performance computing, memory and advanced logic chips, which are segments of the industry in which the EU is weak.⁽¹¹³⁾ In fact, no EU headquartered company has any

⁽¹¹⁰⁾ Decision Etudes & Conseil and YOLE Group, Competitiveness of the EU semiconductor manufacturing industry, Nov.2025.

⁽¹¹¹⁾ Cloud and AI Development Act Impact Assessment.

⁽¹¹²⁾ [China asks carmakers to use up to 25% local chips by 2025](#)

⁽¹¹³⁾ [Europe is losing out big time on the AI and data centre battle | articles | ING Think](#)

leading-edge manufacturing capacity for both logic and memory. Furthermore, as seen in **Table 2**, when looking at the historical and projected number of design starts in the EU at $\leq 7\text{nm}$ (an indicator of design activities for leading-edge semiconductors), the EU has been and is expected to continue to be a minor player.

Metric	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030
Design starts ($\leq 7\text{nm}$)	4	9	14	19	26	38	60	91	123	157	194
Percent Europe (%)	0.65	1.30	0.97	1.29	1.72	1.22	1.87	2.17	2.83	3.48	4.14

Table 2 - Design starts in Europe $\leq 7\text{nm}$ (Source IBS Monthly Report June 2024)

TSMC reported that orders linked to high-performance computing accounted for roughly 60% of its revenue in Q2 2025, reflecting growth in AI chips, networking base stations, PCs and game consoles. ⁽¹¹⁴⁾ Analysis by McKinsey expects these trends to persist, with AI processors forecast to grow with a CAGR of 18-29% annually between 2023 and 2030, and memory chips at a CAGR of around 17-23%, with AI and computing chips capturing over 50% of global semiconductor market growth until 2030. As the whole semiconductor market will grow at a rate of 8-9% annually until 2030, the other semiconductor sectors are expected to expand at a slower pace, hence the EU's share of the global market is expected to diminish further.

Markets for mature-node chips are also under pressure due to changes in demand profile. For example, in **automotive**, the industry is shifting towards more centralised, software-defined architectures with very powerful real-time central processing units **required for the increasingly autonomous and connected vehicles**. As of today, such processors are supplied by non-EU vendors, such as Nvidia, Qualcomm and Intel (Mobileye), often reusing elements of architectures originally developed for smartphone, datacentre or edge-AI inference workloads adapted for automotive-grade requirements. By 2030, around 30-35 million vehicles per year running on ADAS¹¹⁵ Level 2+ to Level 4 systems, including 6-8 million from European carmakers, are likely to require such central high-performance processors ⁽¹¹⁶⁾.

In **telecom** networks, baseband units and edge nodes require high-speed processors in 5G and forthcoming 6G deployments: by 2030 European equipment vendors may require up to 1 million units per year. Furthermore, emerging applications in industrial **automation, robotics, defence and security** will require energy efficient, high-performance AI processing chips at the edge, and the combined EU-linked demand may be estimated at up to 1 million units per year in the period 2030-35 ⁽¹¹⁷⁾. Finally, a promising new consumer market segment

⁽¹¹⁴⁾ [2Q25 Presentation \(E\)](#) Note: for TSMC, HPC includes PCs, tablets, game consoles, servers, base stations and more (see [2024 Business Overview 0.pdf](#))

⁽¹¹⁵⁾ Advanced Driver Assistance Systems

⁽¹¹⁶⁾ <https://www.mckinsey.com/industries/automotive-and-assembly/our-insights/mapping-the-automotive-software-and-electronics-landscape-through-2030>

⁽¹¹⁷⁾ Estimates based upon market forecasts from ABI Research, Goldman Sachs, Markets and Markets, Fortune Business Insights and other analysts on edge AI markets and robotics.

is the one of **smart glasses** ⁽¹¹⁸⁾, that could generate demand in the order of millions of high-end embedded processors per year, and where the EU is potentially well positioned.

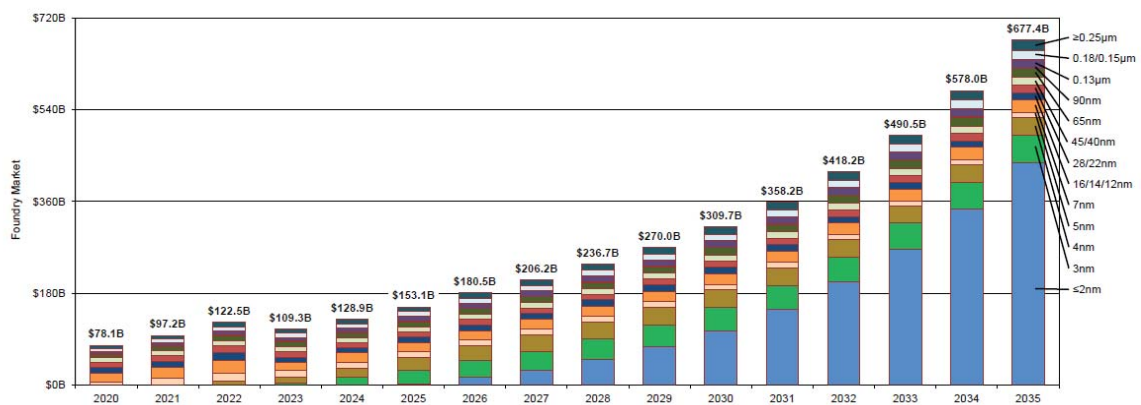


Figure 17 - Foundry market by technology node (source IBS, February 2025)

The EU semiconductor industry could make use of its established experience with automotive and industrial customers to capture higher added-value markets or move into these next generation technologies. However, challenges in this regard include: the lack of demand aggregation, as these sectors rely on customisation or relatively low volumes compared to AI data centres and smartphones; and the steep up-front investment required for developing more leading-edge technologies. Workshop participants described this as a fundamental structural weakness since fragmented demand has prevented economies of scale, limiting Europe's ability to industrialise emerging technologies ⁽¹¹⁹⁾.

It is therefore clear that unless the EU succeeds in channelling demand from these downstream markets towards European solutions, entire swaths of the EU's industrial base could be locked into third country technologies, thus limiting opportunities for the development of European alternatives and exposing the Union to potential economic coercion.

2.3.5 PD5: Insufficient information available to public authorities on the resilience of the European semiconductor supply chain

The Evaluation of the Chips Act clearly showed that while coordination between the Commission and Member States has significantly improved via the European Semiconductor Board (including information on possible disruptions, such as in the *Nexperia case*), the crisis preparedness framework still remains insufficient, for the following reasons:

- The Pillar III framework is largely reactive in nature, with the toolbox of measures being applicable only after a crisis stage is activated. Preventive actions are carried out only after alerts are received in line with Article 22 of the Chips Act.

⁽¹¹⁸⁾ Smart glasses are wearable devices integrated into eyeglass frames that combine miniaturised displays, cameras, sensors, and wireless connectivity to deliver augmented reality experiences and hands-free computing. Applications span industrial maintenance, healthcare, logistics, defence, and consumer use.

⁽¹¹⁹⁾ Annex 2 Section 8

- The preventive actions the Commission and Member States can undertake before the activation of the crisis stage remain limited in nature ⁽¹²⁰⁾.
- The boundaries of when public intervention (preventive action) is warranted before a crisis stage is activated are not set.
- There is limited EU visibility into semiconductor supply chains, coupled with the complexity of said supply chains, makes it almost impossible to assess when to intervene. The types of information that are missing are different in nature (depending on the technology used, type of semiconductor product or process etc.) but often revolve around supply chain data such as supplier relationships, capacities, inventory levels etc. Such information is at the hands of the industry.

In the current context, the semiconductor supply chain remains highly vulnerable to disruptions due to its structural complexity, fragmentation, and reliance on a limited number of actors at critical stages of the supply chain. Recent trade restrictions, including those arising from the COVID-19 pandemic, restrictions imposed on AI chips ⁽¹²¹⁾ and critical raw materials ⁽¹²²⁾, as well as concerns about overcapacity in mainstream semiconductor segments ⁽¹²³⁾, have demonstrated that the Union currently lacks sufficient crisis preparedness capabilities required for timely, decisive and effective action.

Operational capacities for supply chain monitoring, risk assessment, and crisis management at both Union and Member State levels also remain limited. Although the European Semiconductor Board and initiatives under Pillar III of the Chips Act have established an architecture for supply chain monitoring with mandatory data collection in times of crisis (Article 25), and encouragement of voluntary data sharing (Articles 19 and 20), it does not establish broader compulsory data-sharing mechanisms comparable to those existing, for example, in the US where data disclosure can be mandated for national security purposes ⁽¹²⁴⁾. As a result, public authorities are constrained in their ability to anticipate risks, model disruption scenarios, or assess emerging market developments.

The resources and tools available, particularly in terms of specialised staff and analytical expertise, are also insufficient to ensure continuous and real-time situational awareness. Current tools do not yet support advanced forecasting, rapid information-sharing, or coordinated response planning.

⁽¹²⁰⁾ Under Article 22 of the Chips Act, the Commission shall convene an extraordinary meeting of the European Semiconductor Board, composed of Member States representatives, to discuss the severity of the supply disruptions, whether to activate the crisis stage, whether to carry out joint procurements, and to discuss with stakeholders to identify and prepare potential preventive measures. The Commission shall also enter in consultations with relevant third countries to seek cooperative solutions.

⁽¹²¹⁾ https://ec.europa.eu/commission/presscorner/api/files/document/print/en/statement_25_255/STATEMENT_25_255_EN.pdf

⁽¹²²⁾ <https://www.technologyreview.com/2023/07/10/1076025/china-export-control-semiconductor-material/>

⁽¹²³⁾ https://ec.europa.eu/commission/presscorner/api/files/document/print/en/statement_24_1828/STATEMENT_24_1828_EN.pdf

⁽¹²⁴⁾ Under the US Trade Act of 1974, Section 301 is designed to address “unfair foreign practices affecting U.S. commerce”. Section 301(b) can also be used to respond to “unreasonable or discriminatory foreign government practices that burden or restrict U.S. commerce”. Under Section 302(b), the U.S. Trade Representative may self-initiate an investigation under Section 301.

Structural features of the global semiconductor market further compound these preparedness gaps. The sector's strong cyclicality, high capital and knowledge intensity, long production lead times, and significant geographic concentration create systemic vulnerabilities that can amplify even minor disturbances. Without robust monitoring and crisis-response capacities outside of the formal crisis stage under the Chips Act, such vulnerabilities can quickly translate into supply chain disruptions with significant economic and societal consequences.

However, on data gathering under Pillar III, industry stakeholders have expressed legitimate concerns about sharing sensitive information, including commercially confidential data and trade secrets. Strengthened coordination mechanisms, clearer safeguards including EU antitrust compliance, and trust-building measures are required to mitigate these concerns, but they are not yet sufficiently developed.

Taken together, these factors mean that the EU lacks the necessary preparedness to identify, anticipate, and mitigate semiconductor supply chain crises in a timely and coordinated manner.

2.4 How likely is the problem to persist?

There is limited evidence to suggest that the challenges outlined above are transient. Three structural factors indicate that the current problems are likely to persist over medium to long-term.

First, **geopolitical tensions are expected to endure if not further intensify**. These tensions are not driven by short-term political cycles but by long-term shifts in the global balance of power that are leading to persistent competition in the domains of security, technological supremacy ambitions, economic influence, and global governance. The sector's centrality to advanced AI systems and defence capabilities has further elevated its geopolitical significance, resulting in the adoption of far-reaching industrial policies and increasing export controls. Recent measures to restrict the access to AI chips (US) and critical raw materials (China) demonstrate a continued willingness by the US and China to leverage economic dependencies for strategic purposes.

Second, **the semiconductor value chain remains structurally fragile and highly exposed to disruption**. Multiple bottlenecks and a high concentration at different stages of the value chain, from advanced manufacturing of logic chips to materials and equipment, make interruptions likely. While significant investment is underway in the EU, including projects supported under Pillar II of the Chips Act, there are still gaps in capacity ⁽¹²⁵⁾. At the same time, the high degree of geographic concentration in several critical segments of the value chain increases the system's vulnerability to natural disasters and other supply shocks. Even minor disturbances can propagate rapidly across the chain and impact well beyond the initial point of failure. Until additional European capacity becomes fully deployed, the ecosystem will remain inherently prone to instability.

⁽¹²⁵⁾ [Special report 12/2025 - The EU's strategy for microchips](#)

Finally, **the ongoing expansion of semiconductor production capacity in Asia and the US, supported by substantial public support**, is currently outpacing the EU. All leading semiconductor players (China, Japan, the US, South Korea, Taiwan) are intensifying their industrial strategies, expanding fabrication capabilities and consolidating domestic supply chain ecosystems. This sustained momentum indicates that competitive pressure on European manufacturers will not diminish: rather, it is expected to increase as other regions continue to scale leading-edge manufacturing capacity, thus cementing long-term strategic advantages.

3 WHY SHOULD THE EU ACT?

3.1 Legal basis

The current legal bases of the Chips Act Regulation are Article 173(3) and Article 114 of the Treaty on the Functioning of the European Union (TFEU). The Union shall contribute to the achievement of the objectives set out in Article 173(1) TFEU through the policies and activities it pursues, as these objectives are to ensure that the conditions necessary for the competitiveness of the Union's industry exist. In accordance with a system of open and competitive markets, actions are aimed at: speeding up adjustment of industry to structural changes; encouraging an environment favourable to initiative and to the development of undertakings throughout the Union, particularly small and medium-sized undertakings; encouraging an environment favourable to cooperation between undertakings; fostering better exploitation of the industrial potential of policies of innovation, research and technological development. The objective of Article 114 TFEU is the establishment and functioning of the internal market by enhancing measures for the approximation of national rules.

A new legislative act would have the same legal bases as the current Chips Act Regulation. New actions would ensure the conditions necessary for the competitiveness of the Union's industry and improve the level playing field for companies in the internal market, subjecting them to the same requirements across the Union.

Regarding the legal basis of Article 173(3) TFEU, Article 6 TFEU notes that the Union shall have competence to carry out actions to support, coordinate or supplement the actions of the Member States. These areas of action include industry, according to Article 6(b). With regard to the legal basis of Article 114 TFEU, Article 4(1) TFEU notes that the Union shall share competence with the Member States where the Treaties confer on it a competence which does not relate to the areas referred to in Articles 3 and 6. Article 4(2)(b) further notes that shared competence between the Union and the Member States applies in area of the internal market.

As the initiative is subject to shared competence according to Article 4 TFEU and the competence to support, coordinate or supplement according to Article 6 TFEU, compliance with the subsidiarity principle must be ensured. In the case of Article 173(3) TFEU, actions taken should not entail the harmonisation of national laws and regulations but reinforce the competitiveness and resilience of the semiconductor industrial base. The current Chips Act and any new legislative act building on the Chips Act Regulation bolster the strength and resilience of the European semiconductor technology and industrial landscape, enhancing the innovation potential of the semiconductor ecosystem throughout the EU. This includes lowering the reliance on a small set of non-EU companies and regions and expanding the EU's ability to design and manufacture advanced semiconductors. The Chips for Europe Initiative (Pillar I), which will continue to be supported through the new legislative action, is

intended to help achieve these goals by closing the gap between the EU's research excellence and its effective, sustainable industrial deployment.

3.2 Subsidiarity: Necessity of EU action

The objectives of the proposed actions cannot be achieved sufficiently by Member States acting alone. The economic activities relating to the semiconductor industry across the Single Market are deeply integrated. Semiconductor industry resilience across the Union cannot be effective if approached in a severed manner through national or regional silos. The Chips Act came to address this shortcoming, by setting a common Union framework. The challenges of over-dependence on third country semiconductor supply chains and limited crisis-preparedness capacities manifest differently at national, regional and local levels, due to the variation in national industrial sectors and levels of technological capability. Across the EU, however, the problem is broadly widespread rather than confined to a few countries, because all Member States, regardless of their own manufacturing footprint, are deeply embedded in integrated European value chains that rely on globally concentrated design and manufacturing of semiconductors. The underlying causes of these vulnerabilities are the same across the EU, stemming from the globalisation of the semiconductor industry. While Member States can deploy certain measures individually, such as investment incentives, national semiconductor strategies and workforce programmes, they generally lack the scale, coordination mechanisms, and market-steering power needed to address structural dependencies in a globally concentrated industry. Relying solely on national action risks fragmentation, distorting the single market in ways that run counter to Treaty principles or undermine the interests of other Member States competing for the same investment or supply contracts. The problem is inherently cross-border, given the pan-European nature of semiconductor value chains, the interconnectedness of R&D ecosystems, and the fact that disruptions in one Member State can rapidly propagate through the internal market. Leaving action to Member States alone would increase costs and inefficiencies, as parallel and uncoordinated national initiatives would duplicate efforts, dilute bargaining power, reduce interoperability of preparedness measures, and ultimately fail to achieve the scale required to meaningfully reduce the EU's strategic dependencies.

3.3 Subsidiarity: Added value of EU action

The objectives of strengthening the EU's semiconductor design and manufacturing capacity and improving crisis-preparedness can be achieved more effectively at Union level, since the scale and systemic nature of the challenges exceed the capacity of individual Member States acting alone. Significant economies of scale arise when coordinating investment in large-scale manufacturing facilities, shared R&D infrastructure, and cross-border early-warning and monitoring systems, meaning that EU-level action can pool resources, reduce duplication, and deliver outcomes more efficiently than fragmented national efforts. Measures such as the ramping up of production capacities, the speeding up of permitting, priority rated orders and common purchasing aim to ensure a coherent response to future crises and to avoid the fragmentation of the Single Market.

A common policy framework also brings clear benefits, as it replaces divergent national incentives, crisis-response protocols, and reporting standards with common approaches that ensure coherence, reduce administrative burdens, and avoid subsidy races or inconsistent regulatory requirements. The functioning of the internal market is thereby improved, since

coordinated EU action minimises distortions, ensures fair competition for attracting semiconductor projects, facilitates the smooth circulation of critical inputs and chips, and strengthens the resilience of cross-border supply chains that depend on seamless integration across Member States.

4 OBJECTIVES: WHAT IS TO BE ACHIEVED?

4.1 General objectives

The original Chips Act had two general objectives: ⁽¹²⁶⁾

1. To ensure the conditions necessary for the competitiveness and innovation capacity of the Union, to ensure the adjustment of the industry to structural changes. This involves strengthening the EU's research, development and innovation leadership to help the semiconductor industry adjust to structural changes. This is primarily addressed by Pillar I, the "Chips for Europe Initiative", which focuses on bridging the 'lab to fab' gap.
2. To improve the functioning of the internal market by laying down a uniform Union legal framework for increasing the Union's long-term resilience and its ability to innovate and provide security of supply in the field of semiconductor technologies. This objective focuses on increasing the Union's resilience and security of supply in the field of semiconductor technologies. This is primarily addressed by Pillar II, which creates a framework to support "first-of-a-kind" manufacturing facilities, and Pillar III, which establishes a coordination mechanism for monitoring, crisis prevention and response.

The proposed Chips Act 2.0 builds on these objectives with two new general objectives:

1. Increase the competitiveness of the European semiconductor value chain to improve its technological sovereignty and resilience, by accelerating the industrial deployment of research and innovation, ensuring security of supply and reducing strategic dependencies in cutting-edge and mature semiconductor technologies.
2. Enhance crisis preparedness to ensure the EU's security of supply, by increasing the resilience of the European semiconductor supply chain and protecting EU's economic security.

The original Chips Act and the proposed Chips Act 2.0 share a common overarching aim, i.e., **strengthening the Union's semiconductor ecosystem**, but they differ in emphasis and conceptual framing. The evolution is characterised by a shift from a predominantly innovation and internal-market-driven logic towards a **more explicit strategic resilience and technological sovereignty framing**, with stronger focus on supply-chain dependencies and crisis preparedness. Chips Act 2.0 widens the competitiveness and innovation rationale to a broader value-chain perspective and explicitly links competitiveness to the Union's technological sovereignty and resilience. Compared to the original formulation, the Chips Act 2.0 objectives place greater emphasis on accelerating the lab-to-fab transition. This implies an emphasis on ensuring that research and innovation activities translate into not only excellence and leadership but also greater security of supply, and a reduction of strategic dependencies across both cutting-edge and mature semiconductor technologies.

⁽¹²⁶⁾ Article 1 Chips Act, [Regulation - 2023/1781 - EN - EUR-Lex](#)

Furthermore, Chips Act 2.0 elevates crisis preparedness as an explicit general objective, connecting it directly to the Union's security of supply and economic security. While the original Chips Act contains crisis monitoring and response mechanisms under Pillar III, these are conceptually embedded within the objective of improving internal market functioning and ensuring resilience through coordination. The revised framing treats crisis preparedness as a systemic imperative, including outside of declared crises.

While mirroring the general objectives of the original Chips Act, these new general objectives represent a targeted evolution of the current regulation, specifically designed to address the identified problems and their drivers identified in Chapter 2. The new objectives reflect the growing economic security risks created by rising geopolitical tensions and incorporate this dimension into the earlier policy framework.

4.2 Specific objectives

As set out in the intervention logic, the proposed Chips Act 2.0 pursues the following specific objectives:

- SO1: Enhance the capacity, security of supply and competitiveness of the EU semiconductor industry across the value chain, including for leading-edge AI chips
- SO2: Develop a strong user market across key industry sectors
- SO3: Increase intelligence capabilities for crisis preparedness and response

5 WHAT ARE THE AVAILABLE POLICY OPTIONS?

5.1 What is the baseline from which options are assessed?

5.1.1 Current state-of-play

The annexed Evaluation report finds that the Chips Act successfully created a European semiconductor regulatory and policy framework within a notably short timeframe, where none previously existed. Through the three pillars of the Chips Act, it mobilised significant public and private investment, established state-of-the-art EU-level infrastructures, and introduced governance mechanisms to support coordination and crisis preparedness. Stakeholder confidence in the overall strategic direction remains high ⁽¹²⁷⁾, and the Act is widely regarded as a necessary response to geopolitical, technological, and economic pressures. The EU has strengthened its semiconductor research, innovation and early-stage manufacturing base, primarily through EU-level infrastructures such as pilot lines, competence centres and shared facilities, which have improved coordination and reduced duplication across Member States. Access to advanced tools and cross-border collaboration has increased, although several initiatives remain too recent to permit a meaningful assessment.

⁽¹²⁷⁾ See Annex 2 Section 4 “Comparison of the results of consultation activities” for a nuanced assessment

Progress towards large-scale manufacturing deployment and strategic autonomy has taken place and the EU has increased its manufacturing capacity by 30%. ⁽¹²⁸⁾ However, long lead times ⁽¹²⁹⁾ mean new investments have not yet translated into production and a key investment project for a leading-edge chip manufacturing facility has been cancelled. ⁽¹³⁰⁾ One must also consider that the structures of the semiconductor industry are characterised by strong path dependencies. Therefore, rebuilding a semiconductor ecosystem of specialised suppliers and service firms takes time, and success does not come immediately. As a result, the EU continues to depend structurally on non-EU suppliers in critical segments, particularly for advanced nodes.

Furthermore, the lab-to-fab gap persists ⁽¹³¹⁾. While the original Chips Act has raised technology readiness levels, the main challenge has shifted from innovation to industrialisation and scale, with pathways to volume manufacturing still difficult to realise. Scaling constraints are reinforced by limited private capital. Despite significant public funding, late-stage and institutional investment remains weak, reflecting structural features of the European financial system (capital market in particular) and limiting value capture in the EU.

Supply security instruments have improved coordination, but manufacturing deployment remains driven by national frameworks and firm-level decisions. Fragmented markets, weak demand aggregation and limited procurement coordination undermine the commercial viability of new capacity. Finally, EU-level visibility over semiconductor supply chains remains partial. Coordination and early-warning mechanisms have improved, but fragmented access to sensitive data limits system-level monitoring and crisis preparedness.

5.1.2 *Economic impacts*

5.1.2.1 Expected EU semiconductor firms' revenues

Semiconductor firms' revenues

The baseline or 'business as usual' (BAU) scenario shows that the revenues of EU's semiconductor firms, as set out in Annex 4, will expand at a 7.7% CAGR by 2030, and then reduce to 5% from 2030 to 2035. This drop is explained by the expectation that without more leading-edge capacity, the mature node profile of the European semiconductor industry will become less industrially relevant ⁽¹³²⁾ in a market that will increasingly be dominated by AI, as discussed in Section 1.1 and in Annex 4.

Semiconductor value chain

⁽¹²⁸⁾ IDC, Semiconductors market data by feature size, sector and region, CNECT/2022/MVP/0084 – Second Interim Report.

⁽¹²⁹⁾ See Annex 2 Synopsis of the stakeholder consultation activities, section 3.5.2.

⁽¹³⁰⁾ See detailed analysis of the Intel's proposed semiconductor fab in Magdeburg, Germany, and its cancellation, in the Evaluation Report - section 4.1.1.2 on Pillar II.

⁽¹³¹⁾ See Annex 2, sections 3, 4 and 6.

⁽¹³²⁾ IBS Global Semiconductor Industry Service – Analysis of Foundry Market – December 2025

Looking at **the broader value chain**, in a BAU scenario, the EU's strengths in **capital equipment** results in gaining market share from 27.9% in 2023 to 33.5% in 2030 in that segment. This growth is driven primarily by the expected continued dominance of ASML in photolithography, an important chokepoint in both the semiconductor and AI value chain, and the opportunities that arise for EUV lithography machines in the global ramp-up in manufacturing capacity driven by AI. Nevertheless, this dominance in photolithography is increasingly threatened ⁽¹³³⁾, not least from weak demand in Europe, ⁽¹³⁴⁾ and conceals key gaps in a multitude of other tools required for front-end and back-end manufacturing as well as packaging, assembly and testing, as discussed in section 8.1.3 of Annex 4.

Segment	2023	2030
IP	0.3%	0.4%
EDA	20.6%	17.9%
Capital equipment	27.9%	33.5%
Materials	16.8%	18.7%
<i>Substrates</i>	20.5%	22.7%
<i>Other materials</i>	15.9%	17.4%
Semiconductors	10.1%	9.6%
<i>Fabless</i>	0.8%	2%
<i>IDM</i>	17.7%	16.6%
Foundry	0.9%	0.5%
OSAT	0.0%	0.0%
Total value chain share	11.7%	11.6%

Table 3 - The EU semiconductor value chain share of revenues (Source: IDC)

As seen in **Table 3**, the EU's foothold in IP blocks, essential for reusing functions in design, will remain marginal, with its share of revenues rising only slightly from 0.3% in 2023 to 0.4% by 2030. This leaves the Union reliant on a small number of foreign suppliers for essential building blocks that underpin both advanced logic and specialised domain-specific designs. Similarly, when it comes to **Electronic Design Automation** tools, the EU will continue to rely on third-country providers for the essential design flows needed to produce state-of-the-art chips, while capturing 17.9% of global revenues by 2030, down from 27.9%

⁽¹³³⁾ [How China built its 'Manhattan Project' to rival the West in AI chips | Reuters](#)

⁽¹³⁴⁾ Annex 2, Section 4, 5 and 6.

in 2023. Any tightening of export controls or licensing requirements could directly constrain the Union's capacity to design and manufacture competitive semiconductors, including in high performance computing, AI, automotive and security-sensitive applications.

In **materials**, while the EU is expected to have a market share of 18.7% in 2030, up from 16.8% in 2023, 75% of specialty gases at the purity level required for semiconductors will still be sourced outside the EU, with over 50% of them relying on supply chains heavily dependent on China. ⁽¹³⁵⁾ This adds on the dependencies on third countries for critical raw materials such as gallium, which are addressed under other legislative initiatives such as the Critical Raw Materials Act. ⁽¹³⁶⁾

Between 2000 and 2022, the number of **Printed Circuit Board (PCB)** manufacturers in the EU, crucial for the broader electronics ecosystem, dropped from around 560 to less than 175, and the EU's share of revenues dropped from 16% to around 2.3%⁽¹³⁷⁾. The sector remains highly fragmented and dominated by small firms, and the overall market-share trajectory continues to decline. As things stand, only a limited group of European suppliers are able to meet the technological demands created by rapid advances in semiconductors ⁽¹³⁸⁾.

Under the business-as-usual scenario, fragmented and uncoordinated investment across Member States limits the Union's ability to develop competitive complementary capacity along the full semiconductor value chain, thereby increasing dependence on global suppliers and vulnerability to disruptions. Therefore, the Union will **retain critical vulnerabilities and weaknesses** across the value chain, which renders the EU unable to ensure a resilient and secure supply of semiconductor technologies.⁽¹³⁹⁾

5.1.2.2 Manufacturing capacity

The BAU scenario conditions allow for the expansion of the EU's manufacturing footprint, resulting in tangible growth in domestic output and reversing earlier decline. By the end of the decade, the EU's semiconductor manufacturing capacity expands moderately in scale and technological capability: several new and expanded fabs come online, including the STMicroelectronics FD-SOI fab in Crolles (France), the GlobalFoundries foundry in Dresden (Germany), the Intel fab in Leixlip (Ireland), Infineon's Smart Power Fab in Dresden, the ESMC foundry in Dresden, the SiliconBox advanced packaging site in Novara (Italy), and several SiC/GaN wafer and device facilities.

Despite an increase in manufacturing capacity of 30% - from 1.07 million wafer starts per month to 1.39 million wafer starts per month, the EU's **share of global semiconductor production remains at 8.1% by 2030** due to commensurate global expansion. This expansion in absolute terms will strengthen Europe's front-end and back-end manufacturing base and deepen established clusters. These investments also help Europe reinforce ecosystem resilience by sustaining activity in upstream segments, such as equipment and specialty

⁽¹³⁵⁾ See stakeholder consultation in Annex 2.

⁽¹³⁶⁾ [Regulation - EU - 2024/1252 - EN - EUR-Lex](#)

⁽¹³⁷⁾ European Institute for PCB Community (EIPC).

⁽¹³⁸⁾ IPC, Towards a Silicon to Systems Industrial Strategy, 2025.

⁽¹³⁹⁾ Annex 2 Sections 4, 5 and 6.

materials, where European firms hold globally competitive positions without primarily depending on EU-based demand.

The expansion through 2030 should also be viewed in the context of unprecedented State aid provided by Member States, as well as COVID-19-related shortages that incentivised suppliers to expand manufacturing capacity. Beyond 2030, assuming all other factors remain constant, growth is expected to stabilise, shifting primarily to brownfield expansion with more moderate annual growth of 1-3%. As discussed in PD2, environmental and resource constraints, such as rising electricity consumption, water stress in key regions, and lengthy permitting processes further limit the pace at which the EU can expand or upgrade its manufacturing base. **However, under the business as usual scenario, leading edge node manufacturing remains very limited.** In 2023, the EU has limited ≤ 7 nm foundry capacity. ⁽¹⁴⁰⁾ By 2030, the EU's leading-edge capacity by Intel in Ireland may ramp-up, but its foundry service volume will continue to remain modest in absolute terms. Even within the broader ≤ 28 nm category, capacity is limited, with the largest investment of the Chips Act, the ESMC foundry, becoming fully operational only in 2028. The EU's installed base in 2023 is largely at ≥ 40 nm, with mainstream and advanced nodes representing only a very small share of projected capacity by 2030. ⁽¹⁴¹⁾

As a result, the EU's front-end manufacturing profile will remain strongly **skewed toward >28 nm nodes** serving automotive and industrial demand. At the same time, EU semiconductor demand, particularly in automotive, industrial automation, and energy systems, continues to grow faster than domestic supply. In 2023, European semiconductor consumption amounted to roughly EUR 50 billion and is projected to expand at 5-6% annually under the BAU scenario, with automotive demand alone growing at about 8.2% CAGR between 2023 and 2026 ⁽¹⁴²⁾.

Under the BAU scenario, ramping up manufacturing capacity in Europe would remain slower than other competing regions, as set out in PD3. Article 18 of the Chips Act already grants the semiconductor industry 'the most rapid treatment' possible under national legislation: however, it does not set thresholds for permitting times resulting in inconsistent application across Member States, and as such has not significantly reduced permitting times as discussed in PD3.

In terms of technological sovereignty, BAU developments strengthen but do not transform the EU's position. This increase in output will be largely concentrated in the EU's established strengths, such as wide-bandgap semiconductors and mature technologies. These technology families underpin core EU industrial sectors, and the additional capacity helps meet part of the demand from automotive, industrial automation and energy applications. However, **the Union does not establish a competitive foothold in leading-edge logic and memory segments**, where global innovation cycles are fastest, and margins are higher.

⁽¹⁴⁰⁾ IDC, Semiconductors market data by feature size, sector and region, CNECT/2022/MVP/0084 – Second Interim Report.

⁽¹⁴¹⁾ Source Yole/Decision internal report. Market 2030 outlook.

⁽¹⁴²⁾ See Annex 4.

These challenges are compounded by Europe's limited advanced packaging and system-integration capabilities, at a time when global competition is shifting toward heterogeneous architectures, chiplet integration, and 3D packaging.

5.1.2.3 Demand

On the demand side, over the coming years, a steep roll-out of **AI infrastructure** and data centres is expected, driven by the adoption of AI in society, AI Gigafactories and the future Cloud and AI Development Act. In fact, **EU data centre capacity demand is expected to quadruple from 2025 to 2030**, and to go from **12GW to 61.5 GW** in 2036 ⁽¹⁴³⁾.

European consumption will continue to outpace domestic production, driven by **automotive, industrial automation, energy** applications and the ramp-up in **AI data centre** infrastructure. In fact, it is projected that EU demand will expand considerably faster than domestic supply, with an expected CAGR of 7.47% until 2035.⁽¹⁴⁴⁾ Therefore, the gap between the EU's consumption and production widen through 2035, reinforcing high levels of import dependence despite rising capacity.

While the EU will invest heavily in AI Factories and Gigafactories in line with the AI Continent Action Plan, and improved conditions under the Cloud and AI Development Act are expected to spur additional private investment in data-centre capacity, the Union will still **remain reliant on third-country suppliers for AI chips** for both AI training and inference.

5.1.2.4 The cost (price) competitiveness of the EU industry

As analysed in Annex 4 Section 1.1, under a BAU scenario, the EU semiconductor manufacturing ecosystem is expected to remain less competitive than leading Asian manufacturing hubs. As set out in **PD2**, structural cost disadvantages persist across the value chain. EU-based fabs continue to face higher construction and operating costs, longer permitting and build-and-commission timelines, and weaker agglomeration effects than competitors in East Asia. This is also supported by interviews, workshops, and the open public consultation.

The EU's technology and ecosystem profile remains concentrated in automotive, power, analogue, and sensor segments, with limited exposure to leading-edge logic manufacturing. Structural gaps persist in advanced packaging, substrates, and back-end manufacturing, resulting in continued reliance on non-EU facilities for critical stages of production. This dependence introduces additional logistics, coordination, and lead-time costs at the system level and reduces resilience to trade disruptions, even where offshoring remains cost-efficient for firms.

Current cybersecurity legislation, such as the Cyber Resilience Act, will ensure that semiconductor products placed on the European market meet common security requirements, which may favour European suppliers who have a long legacy of secure and trusted products.

⁽¹⁴³⁾ Technopolis Group, Cloud and AI Study for DG CNECT, November 2025

⁽¹⁴⁴⁾ IBS Global Semiconductor Industry Service, Semiconductor Market Analysis by Geographic Region May' 25.

Dependence on imported materials, specialty chemicals, and industrial gases remains largely unchanged. While supplier diversification and recycling mitigate some risks, exposure to geopolitically concentrated supply chains continues to add price volatility and compliance-related cost premia.

Overall, under BAU, public support measures are sufficient to sustain limited capacity expansion but insufficient to overcome Europe's structural cost and ecosystem disadvantages. As a result, the EU's relative position in global semiconductor manufacturing improves only marginally, with no significant convergence towards the cost, scale, or time-to-market performance of leading Asian ecosystems.

5.1.2.5 R&D&I leadership in the EU semiconductor industry

The EU sustains a high level of scientific excellence, supported by R&D at universities, companies, and strong Research and Technology Organisations. Yet, as set out in Section 5.2 of the Evaluation Report, this **research strength only partly translates into industrial innovation and manufacturing capacity**. The establishment of the cloud-based Virtual Design Platform, competence centres, and pilot lines gradually improves access to design tools, technology validation services, prototyping services, and multi-project wafer runs, especially for SMEs and start-ups.

However, systemic barriers remain in the form of late-stage financing gaps, fragmented governance, and dependency on non-EU foundries, which impede firms from scaling prototypes into commercial products, all confirmed by the public consultation ⁽¹⁴⁵⁾. By 2030–2035, these constraints prevent the full realisation of the Chips Act's ambition to bridge the research–industry divide, with many promising actors unable to advance beyond TRL6–8. As a result, the EU's strong research base does not translate into a commensurate increase in domestic design activity or industrial scale-up.

5.1.3 Environmental impacts

Under a BAU scenario, until 2035, Europe's semiconductor industry expands while remaining one of the most environmentally sustainable manufacturing regions globally. Front-end capacity rises from 1.07 million wafer starts per month (wspm) in 2023 to around 1.69 million wspm by 2035 ($\approx$ 20.28 million wspy), maintaining an 8-9 % share of global capacity, but with a lower emissions and resource-intensity profile than most competing regions, particularly East Asia.⁽¹⁴⁶⁾⁽¹⁴⁷⁾. Although absolute electricity demand more than doubles, Europe benefits from a cleaner and rapidly decarbonising power mix, higher penetration of renewable PPAs, and stronger efficiency standards than the US and Asian hubs, leading to a 20-25% reduction in emissions intensity by 2035.⁽¹⁴⁸⁾⁽¹⁴⁹⁾. In contrast to many Asian manufacturing clusters facing severe water scarcity and limited reuse, European

⁽¹⁴⁵⁾ Annex 4 of the Impact Assessment.

⁽¹⁴⁶⁾ [World Fab Forecast | SEMI](#)

⁽¹⁴⁷⁾ [Invisible emissions | Greenpeace](#)

⁽¹⁴⁸⁾ JRC. (2025). *EU's strengths and weaknesses in the global semiconductor sector (JRC141323)*. Luxembourg: Publications Office of the European Union.

⁽¹⁴⁹⁾ McKinsey & Company. (2025). *Semiconductors have a big opportunity—but barriers to scale remain*. McKinsey Global Institute.

fabs routinely achieve 75-85 % water recycling rates ⁽¹⁵⁰⁾, supported by strict permitting and environmental impact assessments, even as total withdrawals reach ~218 million m³/year.

Emissions from fluorinated gases decline faster in the EU than in other regions due to an ambitious EU F-gas Regulation and quicker adoption of climate-friendly technologies ⁽¹⁵¹⁾. While total Scope 1 and 2 emissions still rise with capacity growth (to approximately 1.3-1.6 MtCO₂e Scope 1 and 7.2-8.5 MtCO₂e Scope 2, location-based) ⁽¹⁵²⁾, European fabs operate under higher transparency, stricter environmental standards, and stronger integration of energy- and water-efficiency technologies than most global peers. Overall, compared with other semiconductor regions, **Europe positions itself as a front-runner in sustainable semiconductor manufacturing**, leveraging cleaner energy, world-leading equipment and chemical suppliers, and strong regulatory frameworks to combine industrial expansion with comparatively lower environmental impacts. ⁽¹⁵³⁾

5.1.4 Social impacts

5.1.4.1 Jobs in the EU semiconductor industry

Under a BAU trajectory, employment in the EU semiconductor sector grows steadily but **remains structurally constrained by persistent skills shortages and uneven regional capacity**. Between 2025 and 2030, job creation is driven primarily by fabs and expansions already under construction, including those by Intel in Ireland; STMicroelectronics-GlobalFoundries in Crolles; ESMC, Infineon and GlobalFoundries in Dresden; and STMicroelectronics in Catania, as these projects transition from construction to steady production.

As discussed in Annex 4 Section 2.1, under current policies, skills constraints remain a limiting factor: according to a European Chips Skills Academy (ECSA) report, the sector is projected to add around 156,000 jobs by 2030 and face approximately 271,000 cumulative openings including replacement needs, while graduate inflows are expected to grow by around 1% per year, resulting in a projected annual shortfall of around 16,800 unfilled technical roles by 2030 thus limiting the extent to which announced investments translate into realised employment.⁽¹⁵⁴⁾ Skills needs emerged also as a cross-cutting issue of participants in various workshops, interviews and in the open public consultation. It was also pointed out that semiconductor skills pipelines require decade-long investment horizons, yet relevant programmes operated on shorter budgetary cycles, limiting structural impact.⁽¹⁵⁵⁾

This situation is expected to exacerbate should manufacturing capacity further increase beyond currently announced investments under the Chips Act. A factor that the ECSA study does not consider is the scaling up of European fabless start-ups with the commensurate

⁽¹⁵⁰⁾ SEMI. (2023). *Sustainability in the Semiconductor Manufacturing Supply Chain*. SEMI Global Update.

⁽¹⁵¹⁾ [Fluorinated greenhouse gases - Climate Action](#)

⁽¹⁵²⁾ All calculations are presented in Annex 4.

⁽¹⁵³⁾ [Chip Production's Ecological Footprint: Mapping Climate and Environmental Impact](#)

⁽¹⁵⁴⁾ European Chips Skills Academy (ECSA), Decision Etudes & Conseil. (2024). *European semiconductor skills strategy 2024*. Luxembourg: Publications Office of the EU.

⁽¹⁵⁵⁾ Annex 2 of the Impact Assessment.

demand for skilled chip designers, a scarce resource, this would result in, or the impact that the ongoing AI boom will have on the semiconductor manufacturing equipment industry in Europe.

5.1.5 Governance

5.1.5.1 Supply chain monitoring

Under the BAU scenario, the governance of the supply chain remains constrained by **insufficient insight into supply chain resilience**, as the Commission continues to rely primarily on voluntary information sharing (Arts. 19 and 20 of the Chips Act) and crisis-specific mandatory data collection (Art 25). The stakeholder consultation also confirms that Pillar III has only partially met its objectives. ⁽¹⁵⁶⁾ However, in a pre-crisis stage, a comprehensive understanding of the market is essential. Unlike the proactive and broader provisions established in the US under the Trade Act,⁽¹⁵⁷⁾ which can mandate data gathering for national security purposes, the EU framework still lacks sufficient legal leverage to compel industrial stakeholders to share granular data on stock levels, suppliers, and customers outside of officially declared emergencies. The evaluation confirms these constraints: crisis coordination and monitoring mechanisms remain underdeveloped, and there are no means to monitor and anticipate supply chain disruptions in real time. ⁽¹⁵⁸⁾

The existing provisions for early warning indicators and the crisis toolbox also remain reactive and continue to function largely as activation mechanisms for crises rather than drivers of structural preparedness. While larger companies may increase their risk anticipation and mitigation efforts, significant parts of the European semiconductor ecosystem remain highly vulnerable to geopolitical tensions and supply interruptions. Without new policy intervention, this results in persistent blind spots that prevent the Union to gain a deep real-time understanding of the value chain, to anticipate disruptions to the supply chain before they escalate, to design effective policy responses, to direct investment and to coordinate Member State actions aimed at enhancing supply chain resilience.

Under the BAU scenario, the current Chips Act provides an initial stable and Union-wide framework for the monitoring of parts of the European semiconductor value chain. However, while certain segments are beginning to benefit from ongoing investments and coordination structures, these developments remain partial and have not yet generated a step change in the EU's overall position. Ecosystem resilience improves but dependencies remain throughout the value chain: production capacity grows but is expected to stagnate in the long term; manufacturing sophistication advances incrementally but does not shift the EU into the leading edge; and the Union remains unable to capitalise on its excellent research capacity.

⁽¹⁵⁶⁾ Annex 2 of the Impact Assessment.

⁽¹⁵⁷⁾ Trade Act of 1974, Pub. L. No. 93-618, 88 Stat. 1978 (1975).

⁽¹⁵⁸⁾ See Evaluation of the Chips Act

5.2 Description of the policy options

Policy options for **Chips Act 2.0** were developed based on alternative approaches to industrial and innovation policy. The options are differentiated by the extent to which they rely on two distinct industrial policy models:

- The **horizontal (“market-enabling”) policy approach (PO1)** focuses on improving overall framework conditions through increased support for research, development and innovation, investment in skills, and the creation of a favourable investment environment, **without introducing additional Union-level funding for mass-scale manufacturing and design, notably for AI chips.**
- The **vertical (“proactive”) industrial policy approach (PO2)** builds on the horizontal measures but complements them with targeted financial interventions, notably through **Strategic Projects** supported under the proposed **European Competitiveness Fund**. This approach builds on the European technological assets supported under of the first Chips Act, in particular pilot lines, and translate them into industrial deployment. By introducing a clear EU-level dimension to funding industrial projects and enabling cross-border, value-chain-wide investments, this approach aims to reduce fragmentation while strengthening Europe’s competitiveness, resilience and technological sovereignty.

Policy options should be read cumulatively, as each subsequent option includes all the measures of the previous one and adds further elements:

5.2.1 Policy Option 0: *“The status quo/baseline scenario”*

This would involve the continued implementation of the current Chips Act without any modification. It will maintain the existing R&D&I programme under Pillar I and maintain the same approach to supporting investments through State aid (using the “first-of-a-kind” framework through the existing State aid rules) with no additional Union or Member State budget under Pillar II. Under Pillar III, it will also maintain the current crisis response mechanism, which operates with depends on a voluntary data-gathering regime (except in a crisis). This policy option will not include any policy measures going beyond the scope of the existing Chips Act.

5.2.2 Policy Option 1: *“Measures that focus on the framework conditions”*

In line with the **horizontal approach** to industrial policy, this policy option is based on measures focusing on framework conditions (permitting standards, energy supply, infrastructure, labour skills, etc.) alongside R&D&I interventions.

5.2.2.1 PM1: Increased R&D&I support through the Chips JU

This measure will build on the R&D&I activities under the Chips Act and go further by increasing support in line with the possibilities of the digital windows of the proposed 10th Framework Programme and the European Competitiveness Fund to maintain European leadership in semiconductor research and support the transition from the ‘lab to the fab’.

The focus now shall be on more industrially relevant activities that have a clear path to industrialisation. This shall especially be the case when it comes to pilot lines, which in the

first Chips Act are deployed by Research and Technology Organisations. In their next iteration, industrial partners shall be expected to exploit their results.

Sub-measures here could include new or expanded pilot lines, support for research and deployment focusing on the production of quantum chips, doubling down on the support provided via the Design Platform, a renewed Chips Fund 2.0 and additional funding for R&D&I activities under the successor of the Chips JU. Areas of the new pilot lines could include smart glasses, non-volatile memories, 3D integration. The proposed European Competitiveness Fund is expected to provide novel means to support activities with EU direct management funds that are more attuned to industrial deployment.

5.2.2.2 PM2: Clarification of the scope of ‘first-of-a-kind’

The proposed clarification of the definition of first-of-a-kind (FOAK) shall serve as a more detailed explanation, intended to remove ambiguity and ensure that the entire semiconductor value chain is consistently covered. Under the current definition, the scope of FOAK could have been interpreted by Member States and stakeholders unevenly, *de facto* limiting support to certain segments of semiconductor manufacturing due to the lack of clarity for more upstream and downstream activities that are equally critical to the semiconductor industry. This policy measure builds on this architecture by further clarifying the scope of the first-of-a-kind (FOAK) framework.

Therefore, **PM2** provides for the **clarification of the first-of-a-kind scope**, specifically incorporating elements to increase the focus on **resilience within the FOAK assessment**:

- The **first-of-a-kind scope** is clarified to explicitly include the **entire semiconductor value chain, by clarifying that FOAK** does not only focus on FOAK "**facilities**" but on "**initiatives**," to clarify that FOAK is not only focused on new or substantially upgraded semiconductor manufacturing facilities with an IDM or foundry model, but may also cover other projects in the value chain such as materials or equipment.
- The FOAK definition is clarified to **explicitly cover innovative investments that provide resilience in the semiconductor supply chain**, including for mature technology nodes. **Underrepresented facilities** that address **chokepoints in the supply chain** (such as **mainstream or packaging**) could qualify as **first-of-a-kind** if they strengthen the Union's resilience. The **Nexperia case** demonstrates that these facilities carry a critical **economic and resilience dimension** for the Union. It may be the case that several parallel projects are recognised as first-of-a-kind, as long as it can be proven that those projects do not crowd out existing or planned private activities or create overcapacity. Hence, in light of economic security considerations, certain manufacturing investments that are critical for reducing dependencies on third countries or third country entities may warrant support where, next to innovation, resilience is an element to take into account in the assessment and the investment contributes to the security of supply.

Clarifying the scope of FOAK to ensure projects with a clear resilience dimension can fall within the FOAK definition would enhance coherence with EU objectives such as economic security, while remaining consistent with State aid and competition law principles.

While the mentioned activities are already covered by the current framework based on the Commission's practice, stakeholder feedback indicates that this is not always sufficiently clear in practice, which results in hesitation by Member States to pursue such projects.

Therefore, the clarified FOAK scope would improve legal certainty and reduce interpretative divergence.

5.2.2.3 PM3: Fast-track permitting procedures

Fast-track permitting procedures will build on the proposal for the 'Regulation on speeding up environmental assessment'¹⁵⁹ and potential other upcoming legislation. In that respect, the Chips Act 2.0 will be adopting similar provisions to the Industrial Accelerator Act (IAA) proposal for semiconductor-related facilities, as semiconductors do not fall under the scope of the proposed IAA (¹⁶⁰).

5.2.2.4 PM4: European Semiconductor Regions of Excellence Label

The European **Semiconductor Regions of Excellence seal** would serve as a soft measure giving recognition to regions implementing a framework of enabling policies. This seal would recognise the key role that regions play in supporting the semiconductor industry. The criteria for granting this seal includes **regional measures to support infrastructure, value-chain development and skills**, the establishment of a **one-stop-shop** for all regulatory approvals, **designated land for industrial deployment, single-points of contact for administrative processes** and other framework conditions.

The seal would recognise regions that have direct measures in place to support the semiconductor value chain and attract investments, and aims to encourage additional regions to also take supportive measures. A network of labelled regions would be supported to exchange good practices.

The exact requirements for such a seal would be set out in a delegated act. Regions' adherence to this measure would be monitored by the Commission.

5.2.2.5 PM5: Establishment of a Business-to-business Semiconductor Supply Chain Platform

A **Business-to-Business Platform** ("the Platform") would enhance supply chain transparency and resilience through an industry-led process. The Platform would operate as a secure **digital twin of the supply chain**, enabling participating firms to upload relevant information in a secure environment. Companies would benefit from aggregated insights on supply chain risks, thus supporting internal resilience-building and reducing their own market-information costs. Companies would benefit directly from sharing their data by gaining access to aggregated insights on the overall supply chain. These insights should encourage undertakings to take proactive actions to enhance their supply chain resilience without public sector intervention. For the Commission, a proactive and resilient private sector ensures a lower risk

¹⁵⁹ [COM\(295\) 984 final | Regulation on speeding-up environmental assessments](#)

¹⁶⁰ [Industrial Accelerator Act - Internal Market, Industry, Entrepreneurship and SMEs](#)

of activation of the crisis stage and deployment of the emergency toolbox. The Commission would provide initial support for establishing the platform and cover the setup costs through a competitive call. The participating companies should decide on the governance structure of the Platform and designate its legal representative, while the financing model of the Platform should be thought out by the beneficiary of the call. The platform should eventually be self-sustaining.

Participation in the Platform will be voluntary, except for Strategic Projects and Semiconductor Technologies Facilities, which will be required to join as a precondition for receiving public funding. As envisaged by the Data Governance Act, the Platform will operate in a secure processing environment, respecting all Union legislation including EU antitrust compliance. In the event of a pre-crisis, as a preventative action, previously discussed with and advised on by the European Semiconductor Board, the Commission would have the possibility to request aggregate information from the Platform.

5.2.2.6 PM6: Information requests for aggregate data sent to the Platform in pre-crisis stage

In situations where an alert is triggered ⁽¹⁶¹⁾, the Commission could send a request for information to undertakings. This measure enhances the information available to public authorities outside the formal crisis stage. It follows a **two-step approach**:

- Working closely with the European Semiconductor Board, the Commission could request information to the Platform, supported where possible by aggregated, non-sensitive data from the Platform. The request for information should be sent to the legal representative of the Platform, state its legal basis, purpose, be limited to what is necessary and proportionate in terms of volume of the data and frequency of access to the data requested, have regard for the legitimate aims of the Platform and set out the time limit within which the information is to be provided, and possible penalties according to Article 33 of the Chips Act.
- If the answer is not sufficiently comprehensive, the Commission may issue mandatory requests for information to individual companies that are not participating in the Platform. These requests for information shall state the legal basis and purpose of the request, be limited to what is necessary and be proportionate in terms of volume of the data and frequency of access to the data requested, set out the time limit within which the information is to be provided and possible penalties for incorrect, incomplete or misleading information.

Where the Commission becomes aware of a risk of serious disruption in the supply of semiconductors, or has concrete and reliable information of any other relevant risk factor or event materialising, it shall without undue delay carry out the preventive actions set out in Article 22 of the ECA.

⁽¹⁶¹⁾ As set out in Article 22 paragraph 2 of the Chips Act.

5.2.2.7 PM7: Increased investment in skills initiatives

This measure would promote coordination and investment in skills for the European semiconductor sector via **targeted upskilling and reskilling programmes** to support the rapid adaptation of the existing workforce in the framework of the Skills Partnership for Microelectronics under the Pact for Skills ⁽¹⁶²⁾. Members of the Pact already have access to data on upskilling and reskilling needs, advice on relevant funding instruments to support life-long learning in their regions and countries, and partnership opportunities within a growing community. Here, up-skilling and re-skilling initiatives focus not only on semiconductor firms but also the broader value chain.

These activities would be intensified under Chips Act 2.0 and also be supported via actions under FP10 as implemented by the successor to the Chips JU whose tripartite governance involving the Union, Member States and industry enables the definition of initiatives that respond to different realities in Member States, regions and segments of the semiconductor industry.

5.2.3 Policy Option 2: “Strategic sovereignty”

This policy option adds a more vertical approach to industrial policy under the revised Chips Act, while also including the policy measures listed above (from PM1 to PM7).

5.2.3.1 PM8: Strategic Projects

This measure would adapt the Chips Act to the new realities and possibilities provided by the upcoming Multiannual Financial Framework, particularly the proposed European Competitiveness Fund, which will potentially allow direct management funds to support Strategic Projects ⁽¹⁶³⁾ focused on industrial deployment. Strategic Projects are an answer to the specific economic conditions in the semiconductor industry characterized by large investment volumes and high fixed costs, ecosystem clustering, and path dependencies. Such projects would be developed by fostering a **mix of public and private investment**, including potential additional public investments by Member States through a combination with the concept of FOAK. This would enable EU-level supported investment across the semiconductor value chain through the proposed European Competitiveness Fund. It would complement the current Pillar II framework by introducing direct EU funding, thus increasing the overall scale of public investment, strengthening the cross-border dimension through the integration of manufacturing, design, and supply chain activities, and placing greater emphasis on strategic autonomy and technological sovereignty. Strategic Projects would allow for cross-border, value-chain wide investment that would seek to create synergies across the European semiconductor ecosystem. They would also aim to better integrate SMEs and SMCs along the value chain. The approach is also in line with the **first recommendation of Draghi report** for a “*centralised EU budgetary allocation dedicated to semiconductors, allowing Member States’ co-investment on priority initiatives and industrial projects of high EU added value.*”

⁽¹⁶²⁾ [Microelectronics | Pact for Skills](#)

⁽¹⁶³⁾ Article 8 of the European Competitiveness Fund proposal.

In deploying Strategic Projects, a public-private partnership funding framework **similar to the one used for the AI Gigafactories** could be used, mixing grants (co-financed by the EU and Member States in compliance with State aid rules) and private investments from industry, which would in turn be supported by the European Investment Bank and the European Investment Fund, as well as other sources of public and private investment funds ⁽¹⁶⁴⁾.

By structuring the investment through a mix of grants and financial instruments (equity, loans, guarantees), the Union could aim to mobilise both public and private sector participation while de-risking capital-intensive projects. When it comes to grants, both EU and Member States participation could be envisaged with a variable level of contribution between the EU and Member States, depending on the Strategic Project.

To qualify, a project must comply with certain criteria:

- (i) deliver clear EU added value and support European priorities;
- (ii) have a cross-border dimension;
- (iii) strengthen the resilience, indispensability, and prosperity of Europe's semiconductor ecosystem;
- (iv) contribute meaningfully to Europe's technological sovereignty and leadership.

Strategic Projects would be paired with demand-side measures (PM9, PM10) to increase demand predictability and therefore improve utilisation rates, which is a critical factor for the competitiveness of facilities with high fixed-costs.

Strategic Projects are explicitly designed as cross-border value-chain investments creating spillovers that are economically durable: skills development, local supplier-customer engagement, shorter innovation cycles, higher throughput. These effects improve productivity and reduce costs with a flywheel effect supporting growth across the entire EU ecosystem.

5.2.3.2 PM9: Innovation procurement and support for grand challenges

5.2.3.2.1 Innovation procurement

To contribute to the sustainability and viability of Strategic Projects (PM8), the revised Chips Act will make demand stimulation through **innovation procurement** (pre-commercial procurement and procurement of innovative solutions) an objective under Pillar I of the Chips Act. This objective will complement the Chips Fund in scaling up start-ups in Europe. A first application of this principle could be the deployment of AI chips designed in the EU. This measure would target start-ups and SMEs that are scaling up and would be applicable to firms across the semiconductor value chain.

Under PM9, Pre-Commercial Procurement (PCP) ⁽¹⁶⁵⁾ could be used to create open EU-wide competition for prototype development and testing, with R&D contracts up to TRL 8. These

⁽¹⁶⁴⁾<https://www.eib.org/en/press/all/2025-491-eib-group-and-european-commission-join-forces-to-finance-ai-gigafactories>

⁽¹⁶⁵⁾ European Commission. *Pre-commercial procurement: Driving innovation to ensure sustainable high quality public services in Europe*. Communication from the Commission to the European Parliament, the Council, the European Economic and Social Committee and the Committee of the Regions. COM(2007) 799 final. Brussels:

contracts could be awarded in phases, with suppliers selected based on performance and EU added value. Where results meet the set requirements, public buyers can purchase and deploy the best-performing solutions taking the obligation of current public procurement directives to organise a competitive and transparent procedure into consideration ⁽¹⁶⁶⁾. The involvement and stimulation of the private sector as a buyer of European innovation is also foreseen through grants for procurement.

The first foreseen application of this measure is AI chips and systems for compute infrastructure, where procurement can be managed by European AI Factories. Deployment would include prototype orders, benchmarking in AI Factory environments, and if successful, follow-on procurement. The same logic could be repeated at a later stage also with AI Gigafactories, with broader ambitions for energy-efficient compute solutions built around European technology.

Similar approaches can be followed in tandem with “grand” challenges for other domains depending on strategic priorities:

- Automotive / autonomous driving processors: safety-critical compute, sensor fusion, AI inference
- Secure processors: e.g. trusted CPU platforms for public sector and critical infrastructure
- Ultra-energy-efficient computing: low-power architectures for edge, industrial, robotics, drones.
- Telecom and network infrastructure chips: secure connectivity, RAN acceleration, network processing
- Defence, space and secure communications: high-reliability and sovereignty-critical chips
- Key enabling tools and equipment where Europe has strong capabilities but limited first deployments: e.g. advanced packaging test/inspection, metrology, design automation components, verification toolchains.

The key target beneficiaries of the measure would be EU-based start-ups/SMEs and scale-ups, particularly fabless companies, as well as public buyers and strategic end-user industry sectors, that will benefit from the delivered results. Further, depending on the focus of the call, other key value-chain actors, such as equipment, IP, tools, packaging and testing, and the wider EU semiconductor ecosystem.

5.2.3.2.2 Grand challenges

The scope of grand challenges is the bridging of the gap between pilot line results and industrial adoption by structuring close collaboration between pilot lines and Research and Technology Organisations, start-ups and SMEs, and end-user industries (automotive, industrial, telecom, defence, healthcare, datacentres). The focus of this measure will be on concrete technology tracks such as advanced packaging/chiplets (2.5D/3D), silicon photonics,

European Commission, 2007. Available at: <https://eur-lex.europa.eu/LexUriServ/LexUriServ.do?uri=COM:2007:0799:FIN:EN:PDF>.

¹⁶⁶ Directive 2014/24/EU on public procurement. This regulatory framework is under revision: [Revision of the Public Procurement Directives](#) | [Public Buyers Community](#)

low-power edge-AI platforms, power semiconductors (SiC/GaN) and secure hardware (trusted chips). The model shall be entrenched in application-driven programmes with users in domains such as autonomous driving hardware, robotics, and wearables (e.g. smart glasses), by accelerating prototyping, qualification and integration into real products with clear market value.

5.2.3.3 PM10: Recommend a security of supply declaration for semiconductors in public procurement

This measure would apply to public procurement, auctions and other forms of public intervention involving semiconductors or semiconductor-enabled systems used in critical and strategic sectors within the Union in scope of Annexes I and II of Directive (EU) 2022/2555 (NIS2). It would be a soft policy measure with the aim to increase supply chain transparency and the share of semiconductors supplied by EU undertakings (domestic) or undertakings from countries which can provide an equivalent level of supply chain reliability (equivalent), for instance via the signature of free-trade agreements, participation in multilateral framework such as the General Procurement Agreement or strategic partnerships on semiconductor supply.

Concretely, PM10 would allow public procurement authorities to request from tenderers a supply chain declaration analysing the provenance of semiconductors in the tendered products, outlining their supply chain resilience strategy, in particular with regards to dual sourcing. The declaration would also need to assess the quota of semiconductors supplied from domestic undertakings or equivalent. The public procurement authorities may use the supply chain resilience strategy as outlined in the declaration, and the quota of domestic or equivalent semiconductor suppliers, as award criteria along with price.

The proposed PM10 would be complementary and without prejudice to the “Security of ICT Supply chains” framework laid out in the Commission’s proposal for a Cybersecurity Act 2 (CSA2). While the CSA2 proposal focuses on the cybersecurity aspect, PM10 would address the security of supply aspect, targeting a persistent demand-side market failure that undervalues long-term resilience in procurement decisions, particularly where price-based competition risks favouring subsidised and potentially unreliable suppliers. The limited transparency of long supply chains risks exposing critical sectors in the Union to dangerous dependencies, which could grow unnoticed and then create disruptions as happened in the Nexperia case.

The primary addressees of this measure are public authorities and operators in critical sectors, which would benefit from more secure, resilient and trustworthy semiconductor supply chains. Semiconductor manufacturers from the European Union and from equivalent countries would benefit from reinforced market access and investment certainty. Ultimately, end users and citizens would benefit from improved security, reliability and continuity of essential services and infrastructure across the Union.

5.2.4 Overview of policy options

An overview of the policy options in line with the three-pillar structure of the Chips Act is provided in the table below. The economic, social, and environmental impacts of these

options are assessed in Chapter 6 of this impact assessment, while a comparison of the options is provided in Chapter 7 of this report.

<i>Pillars</i>	<i>Policy Option 0: the baseline/ business as usual scenario</i>	<i>Policy Option 1: Measures that focus on the framework conditions</i>	<i>Policy Option 2: Strategic sovereignty (Includes measures of PO1 and additional measures)</i>
Pillar I: The ‘Chips for Europe’ Initiative	Continue the existing R&D&I program in the Chips JU.	PM1: Increased R&D&I support through the Chips JU.	PM1: Increased R&D&I support through Chips JU. PM9: Innovation procurement and support for grand challenges based on procurement (PCP). Lab-to-fab industrial accelerators
Pillar II: Security of Supply and Resilience	The current “first-of-a-kind” framework.	PM2: Clarification of FOAK’s scope to include the value chain and its relationship with IPF, OEF. Clarification of FOAK to highlight security of supply and resilience aspects	PM8: Strategic Projects stemming from the ECF proposal. PM2: Clarification of FOAK’s scope to include the value chain and its relationship with IPF, OEF and Strategic Projects. Clarification of FOAK to highlight security of supply and resilience aspects
Pillar III: Monitoring and Crisis Response	The existing crisis response mechanism based on a voluntary data-gathering regime.	PM5: Establish a Business-to-business semiconductor supply chain Platform. PM6: Information requests for aggregate data sent to the Platform in pre -crisis stage	PM5: Establish a Business-to-business semiconductor supply chain Platform. PM6: information requests for aggregate data sent to the Platform in pre -crisis stage
Other interventions	No additional policy measures.	PM4: The European Semiconductor Regions of Excellence seal PM7: Increased investment in skills initiatives PM3: Shorter and streamlined permitting processes.	PM7: Increased investment in skills initiatives PM3: Shorter and streamlined permitting processes. PM10: Recommend a security of supply declaration for semiconductors in public procurement

5.3 Options discarded at an early stage

Current semiconductor supply chains remain highly geographically concentrated, with several essential technologies sourced from less trustworthy third countries⁽¹⁶⁷⁾. This introduces systemic vulnerabilities: single-point supply chain failures, coercive economic practices, long-lead disruptions and risks to public safety. Certain critical sectors cannot operate effectively without a regular, trusted, and verifiable supply of advanced semiconductor components.

⁽¹⁶⁷⁾ [Special report 12/2025 - The EU’s strategy for microchips](#)

To materially reduce strategic dependencies, one considered policy response – “trusted chips preference” - was to establish legally binding obligations to use trusted chips for operators of critical infrastructure as listed in Annex 4 of the Chips Act. This option would go beyond procurement preference.

Furthermore, direct mandatory information-request provisions for all companies were considered that would have enabled the Commission, **under all circumstances**, to obtain not only qualitative assessments and aggregate data, **but also granular, company-level information, including business-confidential data where necessary**.

However, this policy option of “trusted chips preference” and “mandatory information requests” was discarded due to overlap with existing legislative acts, such as in the area of cybersecurity and ongoing revisions of the cybersecurity framework. Furthermore, this option could impact the competitiveness of EU user industries.

6 WHAT ARE THE IMPACTS OF THE POLICY OPTIONS?

The impacts of the different policy options are assessed below based on the methodology set out in Annex 4, the results of the open public consultation and Call for Evidence summarised in Annex 2, analysis gained from over 20 targeted workshops with specific stakeholders’ groups, desk research and external studies. Only the relevant types of impacts affecting each Pillar are assessed. Overall, the initiative is not expected to have any impact on fundamental rights. The baseline scenario, outlined in Section 4.1 describes the implications and costs associated with taking no further action.

6.1 PO1 “MEASURES THAT FOCUS ON IMPROVING THE FRAMEWORK CONDITIONS”

Policy Option 1 takes a non-interventionist approach to strengthening the EU’s semiconductor ecosystem. Unlike Policy Option 2, it provides no additional Union funding and introduces no additional direct financial support for manufacturing or supply chain resilience. Instead, it focuses on improving framework conditions and horizontal support measures.

6.1.1 Economic impacts

6.1.1.1 Impacts on EU semiconductor firms’ revenues

Semiconductor firm revenues

For EU-headquartered semiconductor firms, **PO1** would largely maintain the status quo. However, through **PM3**, the policy option would ease the business environment for the semiconductor industry, through simplification efforts via shorter permitting times for the deployment of manufacturing capacity. This measure would allow the Union to tackle the external competitiveness issues that it faces as set out in Figure 12 of **PD2**, as permitting and design timelines differ significantly between Taiwan, Southeast Asia and the EU. Analysis in Annex 3 shows how European firms stand to save up to EUR 625 million in administrative costs if permitting delays are addressed as set out in **PM3**.

A 2025 study by the OECD has shown that high regulatory burdens and compliance costs are “a factor associated with weaker labour productivity growth and business dynamism” ⁽¹⁶⁸⁾. Reducing these burdens would enable European firms to shift scarce resources to more productive activities, which would in turn support an increase in revenue growth.

This would be complemented by the European Semiconductor Regions of Excellence seal (**PM4**), through which participating regions would have deployed enabling initiatives in the areas of skills, infrastructure and administrative processes, thus supporting the reduction of administrative burdens and supporting productivity growth. Its impact will vary by regional baseline and cannot yet be quantified, as requirements will be set by delegated act.

Intensified skilling and re-skilling initiatives (**PM7**) support revenue growth indirectly by easing skills shortages that constrain productivity, ramp-up and time-to-market (see section 5.1.3.3).

In essence, **PO1** is expected to have a limited impact on the market share trajectories of EU-headquartered semiconductor firms manufacturing in Europe. While **PM3** would marginally improve operating conditions through faster permitting and administrative simplification, these measures primarily reduce friction rather than materially strengthening firms’ competitive position. Similarly, the European Semiconductor Regions of Excellence seal under **PM4** would provide visibility and signal regional commitment, but in the absence of differentiated financial incentives, its effect on investment decisions and capacity expansion is likely to remain modest. **PM7**. As a result, **PO1** would broadly preserve existing market dynamics, supporting continuity rather than driving a step-change in the global competitiveness or market share growth of EU semiconductor firms.

6.1.1.2 Semiconductor value chain

PM2 would clarify the scope of FOAK to include the wider semiconductor value chain. Here, the new FOAK definition would concentrate on clearly defined strategic priorities where EU action is needed and can deliver the highest benefit in terms of security of supply and technological leadership as set out in **PM2**. This clarification will enable Member States to provide a more compelling case to semiconductor firms investing in the Union, anchoring higher value-added activities within the Union and support the sustained expansion of the European semiconductor value chain, rather than isolated capacity growth. This shall in turn support more competitive firms which may increase revenues. At the same time, such a measure could potentially fragment Member State’s budgets to a broader number of firms, thus risking less concentrated support.

The Semiconductor Regions of Excellence seal (**PM4**) would also introduce a regional dimension to the Chips Act by encouraging regions to support the semiconductor value chain through for example infrastructure investment and skills initiatives. Since the seal will recognise regions who have direct measures supporting the value chain, it may also encourage regions that do not host semiconductor firms directly but are home to firms that contribute to

⁽¹⁶⁸⁾ OECD (2025), OECD Economic Outlook, Volume 2025 Issue 2: Resilient Growth but with Increasing Fragilities, OECD Publishing, Paris, <https://doi.org/10.1787/9f653ca1-en>.

the broader value chain, to also focus on the strengthening of said ecosystem. This shall be complemented by more comprehensive skills initiatives tackling both semiconductor firms but also the value chain under **PM7** which will have similar impacts as described above for semiconductor firms.

Therefore, Policy Option 1 would reinforce the EU's semiconductor ecosystem along existing strengths, but without much coordination for concerted European action on value chain resilience. **Nevertheless, through a clarification of the FOAK definition, a larger share of planned projects would be expected to proceed compared with the baseline scenario (BAU).**

6.1.1.3 Impacts on manufacturing capacity

Policy Option 1 could moderately increase Europe's attractiveness for investment and enable a larger number of potential projects to be realised when compared with BAU but this would largely depend on market dynamics and Member State and regional budgets.

Available evidence suggests that the EU's expansion potential currently lies in mature and application-specific technology nodes, where it already has a significant foothold. Reducing regulatory burdens in permitting (**PM3**) and alleviating infrastructure bottlenecks (**PD2**) through the Semiconductor Regions of Excellence label (**PM4**) would increase the likelihood that planned projects in these segments materialise, thereby enabling incremental increases in production over time. These effects would occur against the backdrop of the EU's comparatively less favourable business environment. By setting voluntary standards for regions to support their local semiconductor industry and streamline regulatory compliance requirements, the Semiconductor Regions of Excellence label would reduce administrative overhead for industry stakeholders.

As set out above and in Annex 3, in Taiwan, these phases typically take between 6 and 13 months, whereas in the EU they usually require 16 to 18 months ⁽¹⁶⁹⁾. This implies that permitting and design in the EU are approximately 3 to 10 months longer than in Taiwan. Using midpoint estimates, ⁽¹⁷⁰⁾ the average amounts **to roughly 7.5 months additional time**. As set out in Annex 3, the assumption that each year of delay adds around 5 % of total project value ⁽¹⁷¹⁾ implies an additional cost equivalent to 3.125 % of overall investment. Concretely, for a representative EUR 20 billion advanced semiconductor fabrication plant, this corresponds to **roughly EUR 625 million** in additional expenditure. Therefore, a reduction in permitting times (**PM3**) would substantially improve Europe's competitiveness and in turn increase the viability of setting up manufacturing facilities in the EU.

However, the capacity of **PO1** to generate substantial new manufacturing capacity in leading edge technologies, will largely depend on organic growth and the capacity of Member States to support such investments through State aid. The more likely outcome is that **PO1** would

⁽¹⁶⁹⁾ see Figure 12 - Average duration of projects for building wafer fabs

⁽¹⁷⁰⁾ Around 9.5 months for Taiwan and 17 months for the EU

⁽¹⁷¹⁾ <https://www.csis.org/analysis/streamlining-permitting-process-fab-construction>

consolidate the EU's existing strengths in mature and application-specific nodes, support equipment upgrades in current facilities and reduce critical dependencies.

6.1.1.4 Impacts on demand

No demand stimulation measures are foreseen under Policy Option 1 and therefore no change in impact when compared to the baseline is expected.

6.1.1.5 Impacts on the cost (price) competitiveness of the EU industry.

Under BAU, the EU remains the highest-cost manufacturing location among major regions.⁽¹⁷²⁾ **PO1 would not significantly close this structural gap**, as it mainly stems from capital-intensive investment conditions beyond the scope of this option. However, as highlighted by the Draghi report, by improving predictability, reducing regulatory complexity and streamlining permitting procedures, **PO1 could enhance competitiveness and support incremental productivity gains**.

On capital costs, faster permitting as set out in **PM3** as well as better-coordinated infrastructure planning and clearer regulatory requirements under **PM4** would reduce delays and contingencies that, as discussed in **PD2**, currently inflate investment costs through extended construction timelines and higher financing costs. Under Policy Option 1, smoother project execution would lower risk premia and help keep projects within budget, **particularly in Semiconductor Regions of Excellence** whose infrastructure and procedures are suitably adapted.

A clarified FOAK approach (**PM2**) would give Member States greater flexibility to support the entire value chain and thus support European industry in overcoming the cost constraints discussed in **PD2** due to localisation effects that lower logistics costs, reduce supply-chain vulnerabilities, and instil co-development.⁽¹⁷³⁾

Other costs such as energy and labour costs are largely shaped by broader market conditions and would not be affected by this option. However, investments in skills (**PM7**) and more predictable framework conditions would raise labour productivity, support smoother ramp-up and enhance yields. By easing skills shortages, improving the general investment conditions and governance challenges, firms could reduce downtime, improve throughput and better leverage automation.

In these segments, **modest reductions in effective capital and operating costs**, combined with more reliable project delivery, **would lower risk margins than under BAU**. While the PO1 would strengthen the competitiveness of EU suppliers in automotive, industrial and power-electronics markets, where customers value cost efficiency and supply reliability. The effectiveness of accelerated permitting and streamlined FOAK will depend on Member

⁽¹⁷²⁾ Benchmarking shows that production costs in the US are roughly 16% lower, while costs in leading Asian ecosystems can be up to 50% lower.

⁽¹⁷³⁾ Co-development advantages include faster process co-optimisations and joint research activities that are common in dense ecosystems.

States' implementation capacity, which may produce uneven gains and potentially favour incumbents.

6.1.1.6 Impacts on public budget

Overall, the budgetary impact on EU, national and regional budgets would remain moderate compared with the existing Chips Act envelope.

At **Union level**, the main budget effects stem from increased R&D&I commitments within the the next MFF (2028–2034), notably through FP10 and the digital window of the proposed ECF. Support would focus on research, pilot lines and innovation activities implemented through existing instruments. Skills-related spending would increase relative to BAU, subject to availability of budget under the next MFF, and would be channelled through established funding streams. All this is subject to agreement on the next MFF, its programmes, and allocation of budgets from programmes to actions described here. This document does not alter or circumvent the design and architecture set out in the Commission's proposal on the MFF 2028–2034, nor does it pre-empt its implementation.

Administrative and coordination costs for establishing the Business-to-business **Semiconductor Supply Chain Platform (PM5)** are estimated at around **EUR 70 million**. These figures are based on an analysis of comparable data infrastructures such as CATENA-X.⁽¹⁷⁴⁾ Implementation would also require approximately **six FTEs** within the Commission to gather, maintain and analyse data. These resources are necessary to anticipate disruptions, coordinate preparedness measures and ensure the effective functioning of the monitoring mechanism under Policy Option 1.

For Member States⁽¹⁷⁵⁾, a clarified FOAK definition (**PM2**) would facilitate public support for semiconductor investments. This could increase national spending when compared with BAU, although the magnitude would depend on national priorities and fiscal headroom.

6.1.1.7 Impacts on R&D and innovation ecosystem

PO1 is expected to generate positive impacts on European R&D activity within the semiconductor ecosystem and related sectors through increased funding (**PM1**) via the proposed FP10 and ECF. The consultation process highlighted design capabilities as a recurrent priority, including support for fabless actors, open-source architectures and processor development. Under **PO1**, these priorities would primarily be addressed through reinforced Pillar I instruments under **PM1** (pilot lines, competence centres, quantum, design support and the Chips Fund 2.0), improving technology maturity and knowledge diffusion but with limited direct links to industrial-scale deployment. This additional support would also strengthen the scientific and technological capabilities of universities and Research and

⁽¹⁷⁴⁾ [Delivered! 5 Stars! Catena-X: A 3-year, EUR 250 million software start-up success | DIH](#)

⁽¹⁷⁵⁾ It is not possible to quantify the potential increase in national expenditure, as this would depend on the specific form of simplification introduced, the fiscal space and policy priorities of individual Member States, and their willingness to expand or redesign national schemes. While streamlined procedures could reduce administrative costs and may lead to higher demand for support from firms, any resulting increase in national spending would remain uncertain and cannot be reliably estimated ex ante.

Technology Organisations. A secondary, indirect effect may result from reinforced complementary national actions since higher EU-level investment, that is contingent on co-funding, could incentivise Member States to increase their own R&D efforts in order to leverage synergies and maintain competitiveness. Such a dynamic could further boost the EU's capacity to advance semiconductor research and innovation.

Technology transfer and knowledge spillovers are likely to intensify as a consequence of increased R&D activity. The semiconductor sector already exhibits strong linkages between academia and industry, and existing Chips Act projects have established cooperation structures that reduce barriers to knowledge exchange. Enhanced collaboration should therefore facilitate the diffusion of scientific and technical know-how, including from foreign firms expanding their activities in the EU to domestic enterprises and universities.

The funding of **new actions on R&D&I (revised Pillar 1)** in Chips Act 2 will depend on the whether the digital windows of the proposed FP10 and the ECF are of sufficient size and scale to maintain European leadership in semiconductor research and support the industrialisation from the 'lab to the fab'. Since it is expected that the Chips JU will serve as the prime vehicle for the deployment of this funding, the modalities of how this R&D&I support will be deployed will be elaborated **in the upcoming policymaking process related to the follow-up legislation to Council Regulation 2021/2085** establishing Joint Undertakings.

When it comes to the impact of a renewed Chips Fund 2.0 in the next Chips Act, one can consider the outcomes of the current Chips Fund, which is implemented through the EIC accelerator and Invest EU. The Chips Fund has led to a total public investment of EUR 425 million and has resulted in the funding of 55 semiconductor and quantum startups, leveraging an average of EUR 3.8 of private investments for each Euro of equity investment from public funding.

6.1.1.8 Impacts on SME/start-up ecosystem

The **lab-to-fab gap** is widely recognised as a key barrier to start-up dynamism in the European semiconductor ecosystem. However, underlying drivers of this gap, such as limited venture capital and administrative burdens, reflect long-standing structural challenges for European start-ups. These issues fall beyond the scope of the Chips Act and require broader action. SMEs often face higher barriers to entry in Chips Act instruments, as application processes impose disproportionate administrative and compliance costs compared with larger firms.

Policy Option 1 is expected to generate only modest improvements for the start-up and SME ecosystem. Start-ups and SMEs would benefit indirectly from an improved regulatory framework as well as potential technology transfer and financial support from the aforementioned intensified R&D&I activities.

6.1.2 Environmental impacts

Under PO1, the estimated increase in environmental impact is moderate and reflects normal industry developments associated with capacity expansion. Considering the projected increase in manufacturing capacity under PO1, largely through brownfield expansions, calculations indicate that Scope 1 emissions would be around **0.064 tCO₂e per wafer**, while Scope 2

emissions would account to approximately **0.325 tCO₂e per wafer** on a location-based basis and **0.288 tCO₂e per wafer** on a market-based basis⁽¹⁷⁶⁾. These results are in line with the imec.netzero multi-parametric life-cycle assessment model of the environmental footprint for the fabrication of integrated circuits in a high-volume semiconductor fab – **0.08 tCO₂e per wafer** for Scope 1 emissions and **0.42 tCO₂e per wafer** for Scope 2 emissions.⁽¹⁷⁷⁾ Water withdrawal is estimated to increase by about **10.75 m³ per wafer**.

Under PO1, more favourable policy frameworks would lead to a manufacturing capacity growth rate of 4% from 2030 onwards. This would lead to a capacity of 20.3 million wafers per year, which in turn would account to between 1.3 – 1.6 Mt CO₂ in Scope 1 emissions and 6.6 – 8.52 Mt CO₂ in Scope 2 emissions (location-based). Overall, the environmental costs under PO1 are estimated to be between EUR 1.5 – EUR 2.4 billion (taking into consideration aggregated Scope 1 and 2 emissions (location-based)).

Accelerated permitting, clearer and more predictable regulatory frameworks, and improved infrastructure coordination can support earlier deployment of resource-efficient technologies and facilitate access to low-carbon and renewable energy. Targeted support for research, development and innovation under **PM1** is also expected to improve energy, water and material efficiency over time.

From a climate perspective, PO1 is broadly aligned with EU climate objectives, including the 2030 emissions reduction target and climate neutrality by 2050. The small increase in emissions per wafer, combined with Europe's low-carbon electricity mix and growing renewable capacity, limits the risk of a significant rise in absolute greenhouse gas emissions. Overall, the environmental and climate impacts of PO1 would be **incremental, manageable and compatible with decarbonisation pathways**.

6.1.3 Social impacts

6.1.3.1 Impact on skills.

PO1 through PM7 aims to rapidly address ongoing skills shortages, which in Europe is currently estimated at **100,000 engineers**⁽¹⁷⁸⁾, **while establishing a robust talent pipeline for the semiconductor ecosystem**. This focus is supported by feedback from the open public consultation, **where 94% of respondents agreed that serious talent shortages** require investment in attraction, skilling, reskilling and training policies (with 65% strongly agreeing). This option would combine short-term interventions designed to mobilise available labour with long-term structural reforms to strengthen the EU's education and training capacities. It would respond directly to industry demands, labour market projections and Member State feedback gathered during the evaluation of the Chips Act.

⁽¹⁷⁶⁾ All calculations are presented in Annex 4, section 4.

⁽¹⁷⁷⁾ [Die Setup - imec.netzero](#); technologies: N28 (Logic Mobile SoC, 300 mm), Germany - average ; 10 mm die size X and die size Y: yield 85%; IPCC Tier 2C with combustion abatement model.

⁽¹⁷⁸⁾ McKinsey & Company. (2024). *McKinsey on semiconductors: Creating value, pursuing innovation, and optimizing operations* (No. 9, March 2024). McKinsey & Company.

Evidence points to a significant tightening of the talent pipeline: analysis referenced by the European Chips Skills Academy indicates that **around 30% of the current semiconductor workforce is expected to retire between 2023 and 2030**, increasing replacement and upskilling needs. In addition, an ECSA stakeholder survey identifies **chip design profiles as a critical shortage**, with **52% of firms** reporting them among the most sought-after roles. These constraints reinforce the rationale for PM7 as a prerequisite for scaling advanced manufacturing and the EU's fabless ecosystem.

PO1 would support **targeted upskilling and reskilling programmes** to support the rapid adaptation of the existing workforce. These programmes would enable engineers to transition from digital design to analogue and system design and equipment manufacturing workers with the competencies needed to operate AI- and robotics-based tools and manage associated data processes.



Figure 18 - EU regions facing a talent gap versus talent surplus in semiconductor industry
(Source: European Skills Strategy 2025)

To ensure long-term resilience, PO1 foresees significant **expansion of training capacities in critical semiconductor fields**. Dedicated training hubs would be created for highly specialised profiles such as system designers, analogue designers and cybersecurity experts, where severe shortages are expected by 2030. In addition, the option targets reinforcement of electrical and electronic engineering programmes, with a particular focus on Member States where capacity is insufficient or declining. PO1 would promote the deployment of modern digital learning infrastructures, including virtual labs, simulation platforms and remote learning environments, to ensure high-quality training across the Union. Concrete implementation of these activities would rely on the Chips JU and its successor.

The lack of available design talent in the Union has contributed to firms expanding their design workforce in other regions rather than in the EU, underscoring the relevance of

targeted skills investments to retain and grow high-value activities in Europe.⁽¹⁷⁹⁾ **Therefore the successful delivery of skills measures under PO1 would rely on strong industrial participation.** Companies would be encouraged to support the development of curricula with universities and vocational providers, contribute to specialised short courses and training modules, and systematically engage in updating educational content according to technological evolution. **Furthermore, considering that skills are a national competence, the effectiveness of PM7 under PO1 also relies on the capacity of Member States and regions to absorb the increased resources.**

6.1.3.2 Impacts on territorial cohesion.

As stated by the European Semiconductor Regions Alliance (ESRA), the European semiconductor value chain “thrives on proximity, where co-located firms, research institutions, and supply chain partners create synergies that amplify innovation and production” ⁽¹⁸⁰⁾. This points to how important the European semiconductor value chain can be as an engine for regional development and cohesion. PO1 introduces **under PM4 the Semiconductor Regions of Excellence label**, which would set voluntary standards for regions to support their local semiconductor industry and streamline compliance requirements.

This measure would recognise regions who have direct measures in place to support the semiconductor value chain in their region and aims to encourage additional regions to also take supportive measures. The increased reputation of a region, for its excellence in the semiconductor sector, through the **PM4** label, will improve the visibility of said regions as potential targets of investment into their local semiconductor ecosystem. A Network of European Semiconductor Regions of Excellence would be established to exchange best practices and encourage regions to develop complementary industrial strategies in synergy. In this way, **PO1**, especially under **PM4**, is expected to have positive impacts on cohesion and regional prosperity. The level of effectiveness of this measure will depend to a large extent on the reputational value the label acquires to compel regions to take the necessary steps to grow their semiconductor ecosystem.

6.1.3.3 Impacts on security of supply

PM2 would clarify the scope of FOAK to encompass the wider semiconductor value chain and to allow the financing of projects of public interest where these demonstrably contribute to **the EU’s security of supply and economic security**, thereby addressing key vulnerabilities in the EU semiconductor supply chain as identified under **P1**. By strengthening support for identified supply chains, **PM2** would help safeguard the functioning of the Single Market and significantly enhance EU-level crisis preparedness and response, notably through improved availability of chips in crisis. **PM10** would incentivise the supply of semiconductor in critical infrastructures from domestic undertakings or from third countries which can guarantee security of supply. While the overall benefits cannot be fully quantified, they are

⁽¹⁷⁹⁾ [Final-Skills-Strategy-2025-Nov2025.pdf](#)

⁽¹⁸⁰⁾ ESRA, [Home - European Semiconductor Regions Alliance](#)

expected to generate a **substantially positive impact on security of supply** by ensuring continuity of essential goods and services during crises across the Union.

6.1.4 Governance

6.1.4.1 Impacts on governance

PO1 introduces a set of industry-driven transparency tools aimed at improving situational awareness and strengthening the Union's capacity to anticipate, detect and mitigate semiconductor supply chain disruptions, while minimising administrative burden and protecting business confidentiality (**PM6**). Under this option the Union would support the establishment of a **Business-to-Business Semiconductor Supply Chain Platform (PM5)** for companies across the semiconductor value chain building on the recommendations of the Working Group on Supply chains from the Industrial Alliance. ⁽¹⁸¹⁾ The Platform would operate as a **secure digital twin of the supply chain**, enabling participating firms to upload information, which would then be anonymised and aggregated. Companies would benefit from aggregated insights on supply chain risks, thus supporting internal resilience-building and **reducing their own market-information costs**. The platform would be managed by a trusted intermediary on a secure data-sharing infrastructure and in compliance with Article 101 TFEU. The Platform would mitigate part of these risks by **enabling trusted, privacy-preserving multiparty computation** and faster, more reliable information-sharing across the semiconductor supply chain. By providing earlier visibility on supply constraints, demand surges, and potential single points of failure, the Platform could reduce **downstream exposure to global shocks and limit the economic impact of disruptions**. The type of information shared through the Platform would be largely determined by participating industrial stakeholders and is expected to relate to key supply chain metrics, such as availability-to-promise (including available quantities and lead times). To ensure broad participation and compliance, the measure would be accompanied by supporting actions (i.e., technical assistance and interoperability standards) aimed at reducing implementation costs and facilitating effective uptake. The cost for the large companies is estimated at around EUR 100 000 for the initial year (including setting up the API connectors) and then EUR 50 000 for the yearly operations. ⁽¹⁸²⁾

PM5 is expected to generate substantial economic benefits by reducing the severity and duration of potential supply chain disruptions. Public authorities and industry benefit from the Platform's real-time risk mapping, which enables faster crisis response and reduces downstream disruption costs. Evidence gained from the workshop on supply chains and the Call for Evidence ⁽¹⁸³⁾ showed that **supply chain transparency infrastructure** should be considered a core priority. Participants called for establishing platforms that collect and share real-time information about disruptions, capacity, and supply levels whilst respecting commercial sensitivities. ⁽¹⁸⁴⁾

⁽¹⁸¹⁾ [Working Group on Supply Chains | ALLPROS.eu](https://www.allpros.eu/)

⁽¹⁸²⁾ Annex 3 of the Impact assessment.

⁽¹⁸³⁾ [SEMI Europe Publishes 30 Recommendations for a Forward-Looking European Chips Act | SEMI](https://www.semiconductors.org/europe/30-recommendations-for-a-forward-looking-european-chips-act/)

⁽¹⁸⁴⁾ Annex 2 Section 8

The caveat is that **quantifying the precise impact of such a measure is inherently difficult as geopolitical and security risks are the main factors.** For the purpose of this impact assessment, the analysis focuses on illustrating **what is economically at stake in the absence of improved coordination and early-warning mechanisms.** In 2023, two major consuming sectors of semiconductors - motor vehicles and transport equipment (EUR 934 billion) and machinery and equipment (EUR 600 billion) - generated over **EUR 1.53 trillion in production value.** ⁽¹⁸⁵⁾ Without an EU-wide monitoring and crisis-anticipation mechanism, this output remains vulnerable to semiconductor supply shocks. In a **worst-case scenario** driven by major geopolitical disruptions, **more than EUR 1.5 trillion in annual economic activity in these sectors alone could be at risk** if alternative capabilities are not secured within one year.

Two examples from recent years provide additional observable evidence. During the 2021–2022 global semiconductor shortage, the European automotive industry incurred losses estimated at over EUR 100 billion. ⁽¹⁸⁶⁾ While the semiconductor market is inherently cyclical, the structural vulnerabilities that contributed to this crisis persist and as described under **PD1**, have in some respects intensified due to the current geopolitical context. Industry data suggests, for example, that the chip shortfall linked to the Nexperia case could result in more than **EUR 5 billion in lost output** for the affected sector in the final quarter of 2025 alone. ⁽¹⁸⁷⁾

Additionally, the option would further refine the Chips Act’s information request on an ad-hoc basis, to assess potential pre-crisis stages with a view to identifying the appropriate and proportionate content of such a request (**PM6**). The requests would ensure that industrial stakeholders are not required to disclose business-confidential or commercially sensitive data. Instead of granular, company-specific datasets, the Commission could ask for **information request** - supported where possible by aggregated, non-sensitive data sourced from the Platform and if judged insufficient directly by companies. Such requests **would only be applicable under strict safeguards.** This soft approach reduces compliance burdens, ensures principles of proportionality, and enhances trust and cooperation between industry and public authorities. Burden per request for information can be estimated at **10 days/person and hence less than 0.1 additional FTEs.** ⁽¹⁸⁸⁾ This can be translated into EUR 2782 per request and hence negligible and appropriate, compared to the potential savings in anticipating a crisis. Transmission of these requests would take place through a secured communication and information could only be used for the purpose of this request.

The safeguards would be similar to the ones provided in the articles 25 and 32 of the Chips Act (which concern information gathering after the crisis stage is activated and treatment of confidential information respectively). The safeguards should remain flexible enough though to enable the Commission to request information. The requested information shall be limited to what is necessary: **to assess the nature of the potential semiconductor crisis and to identify and assess potential mitigation or emergency measures at Union or national**

⁽¹⁸⁵⁾ <https://ec.europa.eu/eurostat/web/products-eurostat-news/w/ddn-20240724-1>

⁽¹⁸⁶⁾ [Missing chips cost EUR100bn to the European auto sector | Allianz](#)

⁽¹⁸⁷⁾ [Europe’s Carmakers Brace for Severe Chip Supply Crisis](#)

⁽¹⁸⁸⁾ Annex 3 of the Impact assessment.

level before a formal crisis activation (thus for preparedness of the Commission and Member States in case private sector preparedness measures are not enough and public intervention is required) or **to assess whether initiating the procedure referred to in Article 23 of the Chips Act (crisis activation) may be necessary and proportionate.**

These requests for information shall state the legal basis and purpose of the request, be limited to what is necessary and be proportionate in terms of volume of the data and frequency of access to the data requested, set out the time limit within which the information is to be provided and possible penalties for incorrect, incomplete or misleading information. This request for information should always be accompanied with a request to join the platform.

This approach ensures consistent data availability and harmonised monitoring practices across the Union. This targeted access to detailed datasets would allow the Commission to assess specific bottlenecks, dependencies or disruptions with high precision, before reaching the crisis activation stage, thereby improving the effectiveness of proactive crisis-avoidance or mitigation measures. Appropriate safeguards would be applied to ensure strict protection of business-confidential information, proportionality of requests, **and compliance with EU data protection and competition rules.**

The combined implementation of **PM5** and **PM6** would significantly strengthen the EU's ability to anticipate and mitigate semiconductor supply chain risks, particularly by improving **SO3** monitoring capabilities. This would enable a more agile, effective, and proactive response to potential crises.

6.2 PO2 “STRATEGIC SOVEREIGNTY”

PO2 includes several key measures: designating Strategic Projects in line with the proposed Competitiveness Fund to support initiatives under Pillar II, deploying innovation procurement and lab-to-fab accelerators, and strengthening the Union's capacity for crisis preparedness. **PO2** would also absorb all the policy measures under **PO1**.

6.2.1 Economic impacts

6.2.1.1 Impacts on EU semiconductor firms' revenues

6.2.1.1.1 Semiconductor firms

Strategic Projects (**PM8**) are expected to increase the revenues of EU semiconductor firms, with outcomes depending on the technological orientation of the investments. Assuming a potential public budget envelope of EUR 15 billion from the EU via the ECF and from Member States for the **sovereign manufacturing stream**, two scenarios can be considered. As set out in Annex 4 Section 5, if new capacity broadly follows the current European wafer mix, which is dominated by mature and specialty nodes, this investment would approximately generate **up to EUR 6.6 billion** in additional annual revenue. In an alternate scenario where part of the investment supports a leading-edge logic fab while the remainder follows the existing mix, the higher value added would result in a significantly larger market impact of **up to EUR 11.5 billion per year**. Together, these scenarios provide lower- and upper-bound estimates of the revenue effects of Strategic Projects, depending on whether investment reinforces the current industrial structure or enables a partial shift towards advanced manufacturing. For simplicity of analysis, this projection considers only front-end

manufacturing since quantifying revenues from back-end facilities is more complex due to the heterogeneous nature of back-end facilities, which are discussed further in Annex 4 Section 5.

Under the **chip design stream** of **PM8**, the Union and Member States, through their support of designs of strategic importance to the Union such as those for AI chips, are expected to have a net positive impact on the revenues of European semiconductor firms. Public support is likely to de-risk early-stage design activities, accelerate time to market, and enable firms to address high-growth segments with strong global demand. This, in turn, would for example support higher licensing income, increased sales of proprietary designs, or gain in market share for EU-based fabless companies. By strengthening the Union's presence in advanced and application-specific chip design, notably for AI and high-performance computing, these measures are expected to contribute to higher value added and more resilient revenue streams, compared to a continuation of current market trends without targeted public intervention. Because the chips design stream could potentially support a wide variety of designs, end uses, and technology combinations, with heterogeneous business models and revenue channels, it is difficult to quantify its aggregate impact on semiconductor firms' revenues in a robust manner.

The implementation of grand challenges under **PM9** would substantially boost revenues for EU fabless SMEs by leveraging innovation procurement to provide early demand, enable reference deployment and accelerate market entry for leading-edge designs. It would reduce upfront capital constraints and shorten time-to-market, allowing SMEs to reach commercialisation milestones faster and demonstrate market readiness to attract private investors and further sales orders. By formulating mission-oriented requirements in key strategic areas (cloud, automotive, edge, robotics), these challenges would foster differentiated European IP and application-specific chips, enabling SMEs to capture market share in high-growth segments.

Furthermore, as explained in Annex 6, the use of innovation procurement (**PM9**) would enable SMEs to validate technologies early on, making them more attractive for venture capital and investment.

Through support for **lab-to-fab accelerators (PM9)**, semiconductor firms are expected to benefit from faster translation of research results from Europe's world class research institutes into commercially viable products thus reducing development timelines and associated costs. By lowering technological and financial barriers, these measures would enable firms to bring new designs and process innovations to market more quickly, improving their ability to capture early revenues in fast-moving segments.

Together, **PM8** and **PM9** will significantly contribute to achieving SO1 and SO2. By 2035, they will contribute to enable the creation of 200 EU-incorporated semiconductor value-chain start-ups (spinouts or new ventures) that reach at least a seed funding round. Additionally, by 2035, PM9 will contribute to grow the EU's indigenous demand for European solutions by securing EUR 5 billion in innovation procurement for semiconductor-enabled solutions across the automotive, industrial, energy, AI, health, and telecoms sectors, and will deliver at least one flagship co-development project per sector.

6.2.1.1.2 Value chain

Under the value chain stream of Strategic Projects (**PM8**), the Union would have the means to co-invest with Member States in industrial support for companies across the semiconductor value chain, thereby strengthening revenue generation beyond a single segment (for example, manufacturing) and supporting more balanced growth across upstream and downstream activities.

The value-chain wide and cross-border nature of Strategic Projects would **strengthen cluster dynamics, reduce fragmentation and enable progress in segments that require coordinated progress across several stages of development**. Such investments would de-risk investment in the value chain and thereby encourage European firms to develop new capabilities or build competitive advantages that would enable increases in market share and increased revenues. They would contribute to better integrate SMEs and SMCs into the European semiconductor ecosystem with the potential to increase the value chain's resilience by for instance providing innovative solutions or alternatives to current dependencies.

6.2.1.2 Impacts on manufacturing capacity

PO2 marks a step change from the BAU scenario and PO1, where support from the Union's budget is focused on classical R&I support under the research framework programme. Under PO2, through **PM8**, assuming a EUR 15 billion public investment for front-end manufacturing that in turn generates an additional EUR 25 billion in private investment, in line with aid intensities seen in previous FOAK cases, it is estimated that investment through **PM8** would generate, if coupled by improved framework conditions, around **222,000 additional wafers per month** if projects broadly follow the current European wafer mix and up to **108,000 wafers per month** if the investments would include a leading edge facility.

Since budgets are not yet defined and therefore concrete impact analyses are difficult, an assessment was undertaken to illustrate the potential scale of outcomes from Strategic Projects, based on a total investment envelope of EUR 40 billion (public and private combined).

In the analysis of impacts, two scenarios were considered: either all projects would follow the profile of previous FOAK; or the project mix would include one leading-edge front-end manufacturing facility (Scenario 2), with the rest following the profile of previous FOAK projects.

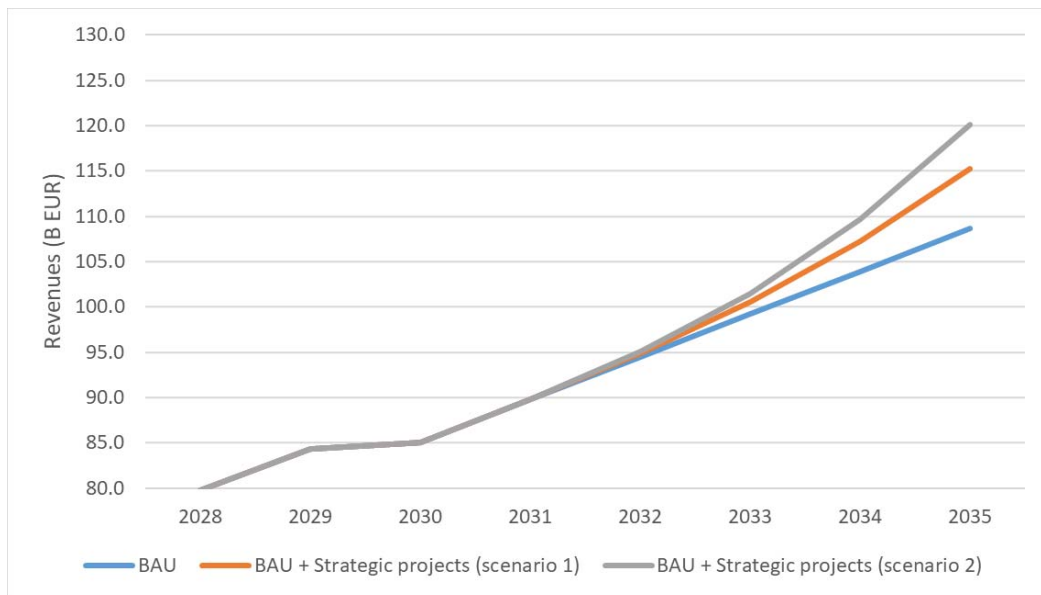


Figure 19 – Projected revenues generated through Strategic projects

Assuming this level of investment, funding for Strategic Projects would increase EU semiconductor manufacturing capacity within the range of ~108,000 to ~222,000 wafers per month, depending on the technology mix. Expansion following the current profile of the Union’s manufacturing capacity yields higher volume, but lower value added (≈ EUR 6.6 billion additional annual revenue), while partial reallocation towards leading-edge manufacturing delivers lower capacity expansion but higher revenues (≈ EUR 11.5 billion per year). Outcomes reflect a trade-off between volume-driven growth and higher-value advanced-node production.

As set out in Annex 4, by analysing previous examples in the previous FOAK projects, a EUR 40 billion investment facilitated by Strategic Projects would generate 7301 direct jobs and 16,000-36,500 indirect jobs.

The lower wafer count under the second scenario is explained by the fact that a leading-edge facility would absorb more of the budget. However, this scenario would give Europe the sovereign means to manufacture leading-edge chips, crucial for AI systems amongst other applications.

Under the ‘sovereign manufacturing’ stream of **PM8**, support for back-end facilities is also foreseen to address vulnerabilities discussed in **PD2**, however forecasting manufacturing capacity in advanced packaging is less straightforward than for front-end fabs because output cannot be expressed in a single, comparable “wafers per month” metric. Packaging throughput depends on heterogeneous product mixes and process routes (for example, 2.5D/3D integration, fan-out, interposers, chiplets), with capacity constrained by different tools and steps and measured in units such as packages, substrates or panels rather than wafers. As a result, nominal tool capacity is highly sensitive to design choices (die size, layer counts, bump pitch, yields and test requirements), making forward-looking capacity estimates less comparable and less predictable than in front-end manufacturing. Furthermore, support under the ‘**supply chain resilience**’ stream of **PM8** would enable the scaling up of manufacturing across the value chain from materials to equipment to design tools.

6.2.1.3 Impacts on demand

The envisaged capacity would be unsustainable without sufficient commensurate demand. As explained in previous chapters, the EU's demand for AI chips in data centre infrastructure and at the edge is expected to rise as AI continues to be deployed across industry and society⁽¹⁸⁹⁾. The upcoming AI Gigafactories, the expected rise in data centre capacity through the upcoming Cloud and AI Development Act coupled with advances in robotics including humanoids but also, autonomous cars, other autonomous defence systems such as drones, immersive-reality technologies (wearables, smart glasses) and the broader AI-driven transformation of all sectors of the European economy create a great opportunity for the Union to channel this rising demand into the emergence of a new generation of fabless companies⁽¹⁹⁰⁾.

However, as set out in **PD3**, many start-ups face a critical gap beyond access to venture capital: the absence of potential anchor customers who can provide early revenue and help establish the credibility of their products. In addition, stakeholders during public consultation repeatedly expressed support for the introduction of demand-aggregation frameworks, enabling coordinated procurement across high-impact sectors such as defence, telecommunications, automotive, health and space. It is for this reason, that **PO2** incorporates a measure (**PM9**) related to **innovation procurement**. Such measure would allow start-ups and SMEs to be involved in projects involving not only the classical support for R&D but also eventual procurement by both public and private sectors, with this procurement being derisked by the Union's investment. This will mark a departure from the BAU approach where support is usually reserved for R&D grants. Innovation procurement is also a useful mechanism for the implementation of thematic grand challenges for leading-edge chip designs in different application areas such as datacentre AI accelerators, automated driving processors, edge AI solutions or AI processors for AI Factories and Gigafactories. Over time, more predictable demand would also help anchor ecosystem actors such as specialised materials suppliers and design houses within the EU market, contributing to broader market growth and contribute to the alleviation of **PD2**.

Empirical evidence⁽¹⁹¹⁾ indicates that competitive public procurement contracts for innovation can generate **persistent revenue effects (up to EUR 0.5 per euro of contract value)** and **crowd in private investment (around EUR 0.2 per euro of public demand)** over the medium term. Public procurement is also associated with **measurable reductions in firm-level risk and uncertainty**, particularly during periods of financial stress, supporting investment and resilience in capital-intensive sectors.

The intervention to incentivise chips from domestic or domestic-equivalent undertakings in public procurement of critical infrastructures (**PM10**) is implemented through a limited adjustment to existing procurement conditions and does not create new regulatory bodies or

⁽¹⁸⁹⁾ Decision based on Eurostat and WSTS.

⁽¹⁹⁰⁾ [McKinsey Technology Trends Outlook 2025 | McKinsey](#)

⁽¹⁹¹⁾ Budrys, Z. (2025). *Consumer of last resort: Government procurement, firm-level evidence and the macroeconomy* (Working Paper). Retrieved from https://zymantasbudrys.com/wp-content/uploads/2022/10/ZymantasBudrys_JMP_LastConsumer.pdf. Refer to Annex 4, section 6 for more details.

compliance systems. Furthermore, contracting authorities already routinely specify security- and certification-related requirements for chips. Requesting a semiconductor supply chain declaration will remain optional, but recommended, for procurement authorities, which may take security of supply considerations into account when designing the technical specification and contract clauses, and consider the information provided in the declaration as criterion other than price when awarding the contract. Potential unit-cost effects are expected to be limited, as semiconductors for critical applications are often already provided by domestic undertakings and semiconductors represent a minor cost component within overall ICT procurement, except for data centres, for which domestic or equivalent undertakings already currently supply the near totality of the chips for the EU market. As a result, the measure is not expected to significantly increase public procurement expenditure while safeguarding security of supply for public infrastructures.

Estimating the policy-relevant market requires mapping semiconductor consumption across NIS2-defined sectors and applying a public procurement share to the resulting totals. The total **EU semiconductor consumption in NIS2-relevant sectors is estimated at approximately EUR 25.6 billion in 2025**, spanning industrial electronics including energy and water (EUR 5.4bn), digital infrastructure including telecoms and servers (EUR 14.9bn), automotive limited to NIS2-relevant applications (EUR 3.6bn), security and safety systems (EUR 1.2bn), health (EUR 1.0bn), defence (EUR 0.4bn) and aerospace (EUR 0.3bn).¹⁹² Applying a public procurement share of 15 to 30%, consistent with OECD estimates for comparable economies¹⁹³, yields a chip value in publicly-procured NIS2 equipment of between approximately EUR 3.8 billion and EUR 7.7 billion.

Currently, undertakings which are neither domestic nor equivalent have a limited market presence in the semiconductor categories most relevant to NIS2 sectors, though the picture varies by product type. In the mature-node segments that dominate industrial, energy and automotive applications (analogue components, discrete semiconductors and microcontrollers) non-domestic suppliers have not yet captured significant EU market share. In industrial and energy procurement, the leading suppliers of analogue and power semiconductors remain predominantly European and North American, with Chinese competitors such as Hangzhou Silan and BYD Semiconductor together holding low single-digit market shares. In automotive and telecoms infrastructure, no non-domestic firm currently features among the top five suppliers by revenue in the relevant product categories.¹⁹⁴

The data centre and AI segment, despite representing the highest chip values, carries the lowest exposure to suppliers who are neither domestic nor equivalent (signatories of agreements which would apply to the supply of semiconductor). Advanced-node components (AI accelerators and high-bandwidth memory) are exclusively designed by US companies and front-end manufacturing is concentrated in Taiwan and South Korea.

¹⁹² Data by Decision Etudes & Conseil, forthcoming, 2026.

¹⁹³ [Government at a Glance 2025 | OECD](#)

¹⁹⁴ [Q4 2025 Results | Infineon Technologies](#).

The most extreme hypothetical scenario, in which public procurement authorities in all sectors would choose to apply the most restrictive criteria on non-domestic semiconductor suppliers, would be a de-facto ban of non-domestic semiconductors. This would have the most significant practical effect on industrial, energy and transport sectors, where mature-node off-the-shelf components represent a potential area of growing exposure as non-domestic suppliers seek to gain market share through artificially low pricing. Even in these sectors, however, switching costs rather than unit price differentials are the primary concern: replacing components typically requires extended qualification timelines, design adaptation and in some cases recertification, meaning that the measure's effects would materialise primarily over a medium- to long-term horizon.¹⁹⁵ Exception clauses for cases of unavailability, disproportionate cost or technical incompatibility are therefore operationally essential, particularly in the short term, and would need to be applied with sufficient precision to avoid supply disruptions in time-sensitive procurement contexts.

The **self-declaration mechanism** places most of the compliance burden on tenderers, who are best placed to map their own supply chains, rather than on contracting authorities, who typically lack the commercial data or technical expertise to verify chip provenance independently. This approach avoids the creation of new regulatory bodies or product-level approval procedures and is administratively lighter than a pre-certification regime. However, self-declaration alone does not eliminate the need for oversight: competent authorities would still need to audit a proportion of declarations and verify the credibility of supplier origin claims, requiring dedicated technical capacity at EU or Member State level.

Tenderers may sometimes be several steps removed from the original chip vendor, as OEMs frequently do not track chip-level provenance through their supply chains, and for commodity or off-the-shelf components, the specific chip models and their geographic origin may not be commercially disclosed (one aspect that the proposed measure is expected to change).¹⁹⁶ They would need to bear some costs, which however would have to be weighed against the costs of increasingly-likely supply chain disruptions due to poor visibility of dependencies, as happened during the COVID-19 pandemic or with the Nexperia case.

6.2.1.4 The cost (price) competitiveness of the EU industry

As under **PO1**, the EU is expected to remain at the higher end of the global cost curve for semiconductor manufacturing, reflecting structural factors such as comparatively higher energy and labour costs (as set out in PD2). However, **PO2** would further reduce investment and operational risks through a combination of Strategic Projects (**PM8**) and demand-side initiatives (**PM9**, **PM10**) alongside continued support via First-of-a-Kind (FOAK) projects, complemented by enhanced supply chain transparency and the framework conditions improvements already present under **PO1**. On capital costs, **PO2** is expected to improve investment feasibility beyond **PO1**. Under **PO1**, faster permitting, coordinated infrastructure planning and clearer regulatory processes would continue to reduce delays and associated financing costs relative to BAU. Under **PO2**, these effects would be emboldened through EU-level co-funding for Strategic Projects (**PM8**), which would lower upfront capital

¹⁹⁵ [Vulnerabilities in the semiconductor supply chain | OECD](#)

¹⁹⁶ [Comments of the Semiconductor Industry Association on the NIST Internal Report NIST IR 8536 2pd | SIA](#)

requirements for selected large-scale investments and reduce the cost of capital by lowering risk premia. This would partially mitigate the EU's structural cost disadvantage described in **PD2**.

Demand-side measures such as innovation procurement (**PM9**) and incentivised procurement from domestic or equivalent undertakings (**PM10**) are expected to support capacity utilisation by strengthening downstream demand and supporting the scaling-up of European fabless and system firms. Higher utilisation rates, by a scaled-up European fabless ecosystem, would support lower unit costs for foundries by spreading fixed costs over a larger output base and reducing the effective capital expenditure per unit of output relative to BAU. While construction and equipment costs would remain broadly unchanged, lower financial risk and reduced underutilisation risk would improve the realised cost position of supported facilities. Supply chain transparency (**PM6**) would not materially reduce OPEX, though better visibility of critical inputs could enable the Union to proactively address issues and reduce unplanned stoppages and operational volatility. This could support improved cost predictability, with indirect positive effects on competitiveness through reduced downtime.

When it comes to price competitiveness, as further elaborated on in Annex 5, PO2 would strengthen the EU's position in specialised higher-value segments where reliability, co-design and advanced packaging are critical differentiators, all elements that could be supported by **PM8**. While global cost hierarchies would still reflect structural factors such as energy prices and ecosystem density, **PO2** would meaningfully enhance the EU's competitiveness and enable diversification beyond current markets and strengths into future, high-growth markets. Strategic Projects could support specialised nodes or packaging technologies with higher value per wafer, improving pricing flexibility relative to BAU.

6.2.1.5 Impacts on public budgets

This subsection assesses how **PO2** would affect public budgets relative to the baseline, covering EU and national expenditure and administrative costs. Under BAU, significant resources are already committed to the semiconductor ecosystem with approximately EUR 43 billion in combined EU and national support for 2023-2030. **PO2** would go beyond this baseline by introducing EU-funded (and Member States co-funded) Strategic Projects (**PM8**), demand-side tools (**PM9**, **PM10**) and mandatory information mechanisms for qualitative data, resulting in **higher and more concentrated public expenditure**, including administrative costs, than under either **BAU** or **PO1**.

At EU level, the largest fiscal effect would come from the creation and co-financing of Strategic Projects (**PM8**). Unlike **PO1**, which increases R&D&I support but does not fund manufacturing investments, **PO2** requires substantial EU contributions for cross-border projects in sovereign manufacturing, advanced packaging, design and supply chain resilience. These allocations would represent a significant deviation from the baseline in both scale and intensity, covering capital investment and multi-year coordination. Demand-side measures, such as innovation procurement, would also require EU resources beyond **BAU** and **PO1**, dependant on procurement volumes.

Union budget depends on the outcome of the next MFF discussions. However, EU level support, the main source of funding would come from the proposed ECF, should it materialise. On the national side, possible sources of financing include cohesion funds.

Under **PM8**, a public-private investment in the range of **EUR 40 billion** would ensure a sufficiently robust investment package on front-end manufacturing to address the leading-edge manufacturing vulnerability thus protecting the Union from geopolitical dependencies or economic coercion as set out in **PD1** while also having further room for investment in front-end facilities in line with Europe's demand profile that continue building on the ongoing FOAK investments.⁽¹⁹⁷⁾ Recent State aid intensities for FOAK projects in Europe, aid is usually at around 30-40% of the project's total costs. This would imply a public investment (EU and Member States) of **EUR 15 billion**.⁽¹⁹⁸⁾

PM8 would also cover back-end investment in advanced packaging and testing, especially 2.5D/3D integration and chiplet-based architectures. These capabilities are increasingly decisive for performance and time-to-market in AI/HPC, automotive and other applications, and would reduce critical EU overdependencies on third-country packaging capacity.

Considering the fact that the Union will for the first time be deploying direct management funding via the ECF for manufacturing capacity, additional administrative resources will be necessary. As set out in Annex 3, around **12 FTEs** would be required to supervise and administer Strategic Projects.

Further measures would be necessary to support design and the broader value chain, although considering the heterogeneous nature of such activities, it is difficult to quantify such support in generic terms. A notable example would be support for strategic design assets (including IP blocks) in the area of AI chips. Here, for leading edge technologies budgets can be significant. In fact, the cost of development of an advanced design at a 2nm technology node may reach up to USD 1 billion,⁽¹⁹⁹⁾ with public support under Strategic Projects supporting a portion of this figure.

In PO2, national budgets would be supported by the EU budget via the ECF when compared with BAU and with **PO1**. Strategic Projects require coordinated co-funding by EU, national and industry partners, implying that participating Member States' budgets would face lower budgetary pressure than when compared to granting State aid alone. Furthermore, this expenditure could generate fiscal returns such as higher long-term tax revenues.

Furthermore, successfully scaled Strategic Projects may generate fiscal returns through personal income taxes and social contributions from direct and indirect employment, as well as corporate taxation linked to additional semiconductor revenues. Based on estimated employment effects (direct and indirect), and additionally generated revenues, the initiative is expected to yield positive net fiscal flows over time, partially offsetting public support. Based on the modelling presented in Annex 4 in Section 5 Strategic Projects might imply annual direct fiscal returns of between EUR 380 million and EUR 662 million.

⁽¹⁹⁷⁾ Further discussed in Annex 4.

⁽¹⁹⁸⁾ All listed budgets are for illustrative purposes only and are without prejudice to the negotiations of the upcoming Multiannual Financial Framework for 2028-2035.

⁽¹⁹⁹⁾ IBS, Global Semiconductor Industry Service, Analysis of Design Costs, September 2024.

6.2.1.6 Impacts on R&D and innovation ecosystem

Semiconductor R&D and innovation would benefit substantially from **PO2**. Strategic Projects under the proposed ECF will be enabling the industrialisation of a greater share of research from publicly funded programmes, including from the pilot lines under Pillar I. Given that much of the innovation in the semiconductor industry involves process optimisation and requires close interaction between laboratory work and manufacturing environments, the expansion of production activities in the EU supported by the Chips Act could also stimulate additional R&D through the need to co-locate research with fabrication. A potential bottleneck, however, is the shortage of skilled scientists and engineers, especially when moving to below 2nm nodes, a challenge already well-documented in the European semiconductor sector.

Furthermore, greater public backing may encourage firms to commit more of their own resources to higher-risk R&D projects, knowing that stronger public support reduces the financial uncertainty associated with such efforts. In addition, empirical evidence suggests that participation in innovation-oriented public procurement is associated with 10–20 percentage point higher probabilities of product innovation, and around 6 percentage point higher probabilities of process innovation, compared to otherwise similar firms ⁽²⁰⁰⁾, ⁽²⁰¹⁾ (see Annex 4, section 6 for more details).

6.2.1.7 Impacts on SME/start-up ecosystem

Start-ups and SMEs would also benefit significantly from **PO2**. The semiconductor industry relies on a wide network of highly specialised smaller firms across the value chain, and increased investment through Strategic Projects under the ECF, together with an expanded scope for First-of-a-Kind projects, would stimulate additional demand for these specialised inputs.

Chip design is another area where start-ups and SMEs stand to gain especially since the EU's fabless companies are almost entirely SMEs whose work is within scope under Strategic Projects (**PM8**).

Furthermore, through the deployment of innovation procurement, start-ups and SMEs can benefit from anchor customers that grant them the first revenues while also serving as a testbed for validation of technology and a pull-factor for further investment. Therefore, beyond firm-level revenues, innovation procurement under **PM9** would strengthen the SME/start-up ecosystem through innovation-to-market routes with clear technical milestones, testing environments and first deployments. By providing reference projects, access to testbed and integration partners, this approach reduces market-entry risks and information asymmetries for investors and customers, improving SME's ability to raise follow-on

⁽²⁰⁰⁾ Andrea Bastianin, Paolo Castelnovo, Lorenzo Zirulia, Overcoming the innovation threshold through innovative public procurement: evidence from CERN, *Industrial and Corporate Change*, Volume 34, Issue 5, October 2025, Pages 871–900, <https://doi.org/10.1093/icc/dtaf004>

⁽²⁰¹⁾ Dragana Radicic, Effectiveness of public procurement of innovation versus supply-side innovation measures in manufacturing and service sectors, *Science and Public Policy*, Volume 46, Issue 5, October 2019, Pages 732–746, <https://doi.org/10.1093/scipol/scz026>.

financing and scale internationally while stimulating cluster effects across the full hardware/software stack and across the European semiconductor value chain.

Design-focused SMEs could also benefit from new investments in advanced chip fabs. Such facilities would shorten and accelerate innovation cycles by reducing reliance on long third-country supply chains and exposure to fluctuating lead times, enhance customer trust when handling sensitive technologies, and offer manufacturing opportunities for lot sizes that large global fabs may consider too small or too specialised.⁽²⁰²⁾ This support would complement existing BAU measures such as the Design Platform, pilot lines, Competence Centres and an expanded Chips Fund, all measures currently in place under the Chips Act. Taken together, increased technological support, improved framework conditions including financing, and the emergence of new manufacturing capacities could be transformative for design-oriented SMEs and start-ups, providing accessibility, speed, security, specialisation and ecosystem benefits that are difficult to obtain from traditional global players.

6.2.2 Environmental impact

When it comes to environmental impact, two scenarios are considered in Section 4 of Annex 4. In **scenario 1**, ⁽²⁰³⁾ the additional capacity generated by PM8 through EUR 15 billion in public investment would reach around 1.8 Mio wafers per month, leading to around 22.0 Mio wafers per year overall capacity. This expansion would be associated with estimated total scope 1 emissions of 1.4 - 1.7 MtCO₂e and scope 2 emissions of 7.1 - 9.2 MtCO₂e on a location-based basis, and water withdrawal of around 236.5 Mio m³ per year⁽²⁰⁴⁾. Total water withdrawal represents an 8.5% increase compared with the baseline; a magnitude comparable to mainstream capacity expansions outside Europe. **Scenario 2** combines the expansion of mainstream nodes with the establishment of one leading-edge fab.

New mainstream capacity would amount to the addition of around 997,596 wafers per year resulting in a total capacity of around 20.4 Mio wafers per year, with estimated total scope 1 emissions of 1.3 – 1.6 MtCO₂e, scope 2 emissions of 6.6 - 8.5 MtCO₂e on a location-based basis, and water withdrawal of about 222.5 Mio m³ per year. The leading-edge fab, modelled on industry data and assumed to reach 300 000 wafers per year, would generate around 74 555 – 79 005 tCO₂e for scope 1 and 290 740 - 310 509 tCO₂e for scope 2 on a location-base basis (assuming average annual increase of 5.79% in emissions per wafer due to rising process complexity). All details of the calculation are provided in Annex 4 - section 4.

Overall, scenario 2 would result in total emissions of about 1.4 - 1.7 MtCO₂e for scope 1, 6.9 - 8.8 MtCO₂e for scope 2 on a location-based basis with a total water withdrawal of approximately 222.3 - Mio m³ per year. While European fabs currently recycle around 10–14% of water, non-European fabs in water-scarce regions such as Taiwan achieve reuse rates of about 80%, indicating significant potential for Europe to improve efficiency and competitiveness through advanced water management. In parallel, the shift to leading-edge

⁽²⁰²⁾ A methodological toolbox to monitor the semiconductors' supply-chain, Publications Office of the European Union, Luxembourg, 2024, doi:10.2760/5085463, JRC138921.

⁽²⁰³⁾ Projects following the technology mix typical for European firms.

⁽²⁰⁴⁾ All calculations are presented in Annex 4.

nodes and advanced packaging would increase material use, as mask layers rise from around 40 at 65 nm to up to 110 at 5-3 nm and additional packaging steps are required. As a result, Europe's total material consumption could increase by up to 65%, broadly in line with trends already observed in leading non-European semiconductor manufacturing hubs.

6.2.3 Social Impacts

6.2.3.1 Impacts on the labour market

Strategic projects and demand-side measures in PO2 will lead to considerable positive effects on jobs in the European semiconductor industry. These effects will be even larger when employment effects during construction of new fabs and further up the supply chain are also considered. A modelling of potential employment impacts shows that due to the Strategic Projects alone, if EUR 15 billion in public funding is dedicated to sovereign manufacturing, one should expect between **4,700 and 7,300 new direct jobs** ⁽²⁰⁵⁾ and an additional **16,000 to 36,000** indirect jobs (depending on other external factors, but projected with a good degree of confidence from the current first-of-a-kind investment). Direct jobs in the semiconductor industry are also reported as high-quality, as reflected in above-average salaries.⁽²⁰⁶⁾ Stronger support for design activities in start-ups and SMEs will also add to employment growth, since these are currently more labour-intensive than automated semiconductor production.

6.2.3.2 Impacts on territorial cohesion

The European semiconductor value chain ***“thrives on proximity, where co-located firms, research institutions, and supply chain partners create synergies that amplify innovation and production”*** ⁽²⁰⁷⁾, which makes the fostering of regional semiconductor ecosystems a powerful engine for regional growth and cohesion. PM8 aims to deliver investments across the European semiconductor value chain. From a cohesion policy perspective, this can lead to spillover effects and multiplication of investment across regions that may not be directly involved in the semiconductor value chain, but in its upstream markets.

PO2 is therefore expected to deliver significant benefits for cohesion and regional prosperity, with the additional funding serving as an incentive for regions to adopt enabling measures and invest in the development of their semiconductor ecosystems.

6.2.3.3 Impacts on security of supply

The availability of EU-level co-funding under PO2 would **enable the Union to invest in facilities that would serve the common European interest by ensuring the availability of critical manufacturing capacity, particularly when it comes to leading-edge chips**, where

⁽²⁰⁵⁾ See Annex 4.

⁽²⁰⁶⁾ For example, in the US case, according to the White House Council of Economic Advisers, the median annual wage in semiconductor and other electronic component manufacturing exceeds that in overall manufacturing and is nearly double the median for retail trade jobs <https://bidenwhitehouse.archives.gov/cea/written-materials/2024/03/20/u-s-semiconductor-jobs-are-making-a-comeback/>

⁽²⁰⁷⁾ ESRA, [Home - European Semiconductor Regions Alliance](#).

the Union has critical dependencies on third countries as discussed in **P1**. Furthermore, **PO2** would also enable greater integration and depth across the semiconductor value chain than the baseline. A Strategic Project could potentially involve several stages of the value chain, including design, manufacturing, advanced packaging and resilience-related activities. This structure would instil a cross-border dimension across Member States and encourage tighter collaboration between manufacturers, design firms, equipment suppliers and materials producers.

7 HOW DO THE OPTIONS COMPARE?

This chapter provides a **comparison of policy options** against the criteria of effectiveness, efficiency, and coherence as well as the principles of proportionality and subsidiarity.

7.1 Effectiveness

SO1: Under the baseline scenario, capacity expansion would continue to rely primarily on market-driven investment decisions within the existing framework. While some incremental growth is expected in areas where the EU already holds structural strengths, persistent bottlenecks related to investment risk, feasibility constraints and limited coordination are likely to constrain expansion in more capital-intensive and technologically advanced segments. As a result, the baseline scenario would only partially contribute to enhancing security of supply and would not materially address strategic gaps in advanced manufacturing and packaging. Persistent issues related to permitting duration, regulatory uncertainty and skills availability would continue to affect investment decisions and project execution, resulting in a suboptimal investment environment

Policy Option 1 would improve conditions for capacity expansion by addressing non-financial barriers, notably through faster and more predictable permitting, clearer regulatory requirements and a clarified framework for First-of-a-Kind facilities. These measures are expected to facilitate investment execution and reduce uncertainty. However, in the absence of targeted Union-level support or demand-oriented instruments, capacity expansion would likely remain concentrated in segments where the EU is already competitive, with limited impact on underrepresented technologies such as advanced logic or packaging. Additionally, Policy Option 1 focuses on horizontal framework improvements, including faster permitting, regulatory clarity and targeted skills measures. These actions are expected to ease long-standing non-financial barriers, improve predictability and support more reliable project implementation across the value chain.

Policy Option 2 builds on these horizontal measures while adding Union-level coordination through Strategic Projects. This additional layer aims to address feasibility constraints for large and technologically critical investments and promote deeper integration across design, manufacturing and advanced packaging. Policy Option 2 combines framework improvements with Strategic Projects and demand-side instruments. These measures would address feasibility constraints for large-scale and technologically critical investments by reducing investment risk and supporting earlier and more predictable utilisation of new facilities. This approach is expected to enable capacity development in both mainstream and advanced segments, including those relevant for sensitive and security-critical applications.

SO2: Under the baseline scenario, user industries would continue to face supply uncertainty and limited incentives to source semiconductors produced in the EU. Here, adoption of new semiconductor and AI-related technologies would largely depend on global market conditions and external suppliers, with limited impact on demand formation within the Union.

Policy Option 1 may contribute indirectly to demand development by improving supply stability and investment conditions, which could encourage adoption over time. However, it does not include instruments specifically designed to stimulate demand or provide offtake opportunities for new technologies. Policy Option 2 introduces demand-side mechanisms, notably innovation procurement, which would provide earlier and more predictable offtake for semiconductor and AI-related products. These measures are expected to facilitate faster adoption by user industries and strengthen linkages between EU-based production and downstream demand.

SO3: Under the baseline, monitoring and crisis preparedness would remain fragmented and largely reactive, limiting the Union's ability to identify vulnerabilities and anticipate disruptions.

Policy Option 1 would improve coordination and information exchange but would not fundamentally alter the scope or depth of monitoring capabilities. Policy Option 2 strengthens information requirements and establishes a Business-to-Business Semiconductor Supply Chain Platform, enabling more systematic and timely insights into vulnerabilities across the value chain. This would support earlier identification of risks and more proactive EU-level preparedness.

7.2 Efficiency

The baseline scenario entails no additional administrative, compliance or budgetary costs. However, it is the least efficient option, as it leaves major structural inefficiencies unresolved and allows substantial implicit economic costs to persist. Evidence from the evaluation and problem analysis shows that under the baseline, lengthy permitting procedures generate significant delay-related costs. Semiconductor projects in the EU face permitting timelines that are on average 7-8 months longer than in leading Asian jurisdictions, corresponding to cost penalties of around 3% of total project value (approximately EUR 600-650 million for a EUR 20 billion fab). In addition, limited monitoring and preparedness lead to reactive rather than proactive crisis management and large downstream losses. Recent shortages resulted in tens of billions of euros in lost output, including EUR 5 billion in the automotive sector linked to the Nexperia disruption and EUR 50-100 billion economy-wide losses reported during 2021–2022. While avoiding direct compliance costs, the baseline therefore performs poorly in efficiency terms.

Policy Option 1 improves efficiency by addressing process inefficiencies and coordination failures primarily through horizontal framework measures. Incremental costs relative to the baseline are limited. Additional administrative and compliance costs for industry are modest and mainly linked to coordination and information exchange; no continuous reporting or new operational requirements are introduced. Based on comparable EU frameworks and observed administrative burdens in similar regulatory settings, these costs correspond to low single-digit person-days per year for large firms. Costs for Member States and EU authorities relate mainly to enhanced coordination and limited monitoring capacity and are largely absorbed

within existing structures. Policy Option 1 does not introduce additional operational costs (such as energy or resource use), as it does not mandate new production capacity, new equipment or changes in production processes beyond firms' existing investment decisions. Against these limited costs, PO1 delivers noticeable efficiency gains by shortening permitting timelines, increasing regulatory predictability and reducing investment risk and delay-related costs.

Policy Option 2 builds on PO1 by introducing Strategic Projects, demand-side instruments and enhanced pre-crisis intelligence, resulting in higher incremental costs, but also more ambitious outcomes. Incremental costs include costs for industry, concentrated on firms voluntarily participating in Strategic Projects, notably through capital co-investment. Administrative and reporting costs linked to enhanced monitoring remain limited and proportionate: reporting is triggered only on an as-needed basis in pre-crisis situations, with preliminary estimates indicating up to 10 person-days per reporting cycle for large firms, and no continuous monitoring obligation. Public costs for Member States arise from co-financing Strategic Projects and strengthened administrative capacity. Under PO2, additional operational costs (including energy and resource use) arise only from voluntary capacity expansion under Strategic Projects and are inherent to increased production rather than to regulatory compliance obligations. These costs are directly linked to measurable benefits. Strategic Projects are expected to generate EUR 6.6-11.5 billion in additional annual revenues, while EU co-funding reduces investment risk, lowers the cost of capital and enables earlier and more predictable utilisation of new capacity. Enhanced intelligence reduces the probability and severity of supply disruptions, mitigating losses that have previously reached tens of billions of euros.

Overall, PO2 can be considered efficient. While it entails higher costs and implementation risks than PO1, these are proportionate with the scale of the economic security risks addressed. The cost of inaction would leave the Union exposed to persistent vulnerabilities and potentially very large disruption-related losses that would significantly exceed the incremental costs of the intervention.

While Policy Option 1 achieves efficiency gains through a low-cost, proportionate intervention with limited administrative and compliance burdens, and Policy Option 2 entails higher incremental costs and implementation complexity, the latter also delivers higher expected benefits in terms of avoided disruption losses, risk reduction and revenue generation; as a result, both options can be considered to achieve a comparable level of efficiency when assessed as the ratio between costs incurred and results achieved.

7.3 Coherence

Internal coherence. All options are internally coherent, as they build on the three-pillar structure of the Chips Act, providing a consistent intervention logic that address a multitude of policy areas from R&I to manufacturing and crisis preparedness under a common governance framework. The scope of Chips Act 2.0 is unchanged across options.

Coherence with EU policies and legal frameworks. The baseline remains formally coherent with existing EU policies and internal market, competition and State aid rules, as it essentially maintains the current framework. However, it makes limited use of complementarities with newer priorities on competitiveness, economic security and strategic technologies. Policy

Option 1 strengthens coherence with EU competitiveness and internal market objectives by improving framework conditions through faster permitting, regulatory clarity and skills measures. It aligns well with the Digital Decade Policy Programme, industrial policy and climate objectives, as it does not mandate new capacity or alter environmental standards and raises no new State aid or competition concerns.

Policy Option 2 shows the strongest alignment with the EU's evolving strategic agenda, including the European Economic Security Strategy, STEP and the Competitiveness Compass. By combining framework measures with Strategic Projects and demand-side instruments, it enhances coherence with EU funding programmes and investment priorities. Targeted support creates potential trade-offs with competition and State aid principles, but these are mitigated through EU-level coordination and compliance with existing State aid rules. Increased manufacturing activity may raise energy demand, requiring consistency with climate and energy policies.

Coherence with international commitments. All options are consistent with the EU's international commitments, including WTO rules. The baseline and Policy Option 1 rely on non-discriminatory framework measures. Policy Option 2, while more interventionist, remains compatible with trade rules by focusing on resilience, innovation and security of supply without introducing discriminatory or trade-restrictive measures.

	Effectiveness in meeting objectives			Efficiency	Coherence
	SO1: Enhance the EU's capacity and security in mainstream and advanced chips, including AI chips	SO2: Develop a strong user market across key industry sectors	SO3: Increase intelligence capabilities for crisis preparedness and response		
PO0 (BAU):	0	0	0	0	0
PO1	+	+	++	++	++
PO 2	+++	++	++	+++	+++

Legend: 0 no / neutral impact; + minor positive impact; ++ positive impact; +++ significant positive impact; - minor negative impact; -- negative impact; --- significant negative impact

8 PREFERRED OPTION

8.1 Reasons for the preferred option

The revision of the Chips Act takes place in a context of geopolitical challenges for the EU, persistent supply chain vulnerabilities and rapid technological developments, particularly in AI. As set out in Chapter 2, the Union continues to rely heavily on a small number of non-EU actors for semiconductor design and manufacturing capabilities. These overdependencies have already resulted in disruptions with significant economic and societal impacts. At the same time, the EU lacks sufficient tools to anticipate and manage semiconductor supply shocks. As Call for Evidence respondents consistently emphasised that there is need for

sustained, long-term strategic commitment at Union level to achieve the EU's ambitions in this sector - reinforcing the assessment that incremental or short-term measures are insufficient to address structural vulnerabilities in the value chain.⁽²⁰⁸⁾ **Policy Option 2 is the preferred option because it provides a coherent and ambitious albeit proportionate response to these structural challenges.**

Policy Option 2 strengthens and extends the current Chips Act through three mutually reinforcing components: **EU-co-funded Strategic Projects, targeted demand-side measures and a more robust monitoring and crisis-preparedness framework.** These measures address the core problems identified, namely the EU's overdependence on third-country suppliers and its insufficient supply chain intelligence capabilities, and they help establish the conditions for a more competitive, resilient and sovereign semiconductor ecosystem.

Strategic Projects would help to bolster the Union's capacities in critical segments of the value chain. While the initial Chips Act has triggered multiple investments the Union maintains precarious technological dependencies. **Strategic Projects provide a coordinated Union framework** to mobilise and pool resources for facilities of strategic European relevance, including leading-edge manufacturing, advanced packaging, specialised foundries, design capacity and key upstream supply chain segments. By reducing financing risks and ensuring cross-border spillovers and coherence, these projects respond directly to the structural gaps identified in the problem analysis and are central to increasing capacity, competitiveness and technological sovereignty.

Secondly, there are demand-side instruments, **notably innovative procurement and procurement of chips.** These measures respond to a structural weakness of the EU economy, whereby its main industries consume significant volumes of semiconductors - predominantly of mature technologies - while generating only limited direct demand for the advanced chips that drive global investment decisions. Much of the Union's consumption of leading-edge chips is embedded in imported systems, limiting the business case for locating advanced manufacturing and design activities in Europe. AI is expected to change this with demand for AI chips for AI Factories, Gigafactories and datacentres rising at a steep rate. By providing predictable early offtake for strategically important chips, demand-side measures reduce utilisation risks in the ramp-up of new facilities and accelerate technological uptake in key user industries such as automotive, industrial automation, robotics, telecoms and defence. This supports the emergence of a stronger internal market for advanced semiconductors and reinforces Europe's broader industrial competitiveness as set out in Annex 5.

The third component concerns **monitoring and crisis preparedness**, an area where the evaluation identified clear shortcomings. Despite progress under Pillar III of the current Chips Act, voluntary and ad-hoc information collection has not provided the effectiveness required to anticipate risks or coordinate timely responses. The preferred option therefore establishes a **Business-to-Business Semiconductor Supply Chain Platform**, supported by the possibility for the Commission to **use requests for information.** This framework enables continuous access to risk-relevant data, including information on dependencies and single points of

⁽²⁰⁸⁾ Annex 2 Stakeholder Consultation (Synopsis Report).

failure, **under strict confidentiality safeguards and EU antitrust compliance**. It strengthens the Union's capacity to detect, assess and mitigate disruptions and to coordinate measures across Member States. This enhanced intelligence function is essential to ensuring the Union's economic security in an increasingly complex and contested global environment. Overall, Policy Option 2 provides the most coherent and effective pathway to achieving the general objectives of the Chips Act 2.0: strengthening Europe's semiconductor competitiveness²⁰⁹ and resilience and reinforcing the Union's capacity to anticipate and manage supply chain crises. It does so by addressing the root causes identified in the problem analysis and by providing targeted solutions for each of the four specific objectives. *Strategic Projects* directly address the EU's missing or insufficient capacities in key segments of the value chain (SO1). By reducing investment risks and aligning national and Union-level initiatives, they also improve the European investment environment (SO3), enabling projects that would otherwise not materialise under current legislation. Demand-side measures complement this by stimulating early and predictable uptake of advanced semiconductor technologies in Europe's major user industries (SO2). Here, reaching the set target of EUR 5 billion in innovation procurement would enable the validation of European technologies which are currently unavailable on the market and thus giving user industries the possibility to procure indigenous solutions. These instruments help overcome the EU's weak market pull for leading-edge chips, shorten time-to-market for innovative products and strengthen the interdependence between EU-based manufacturing and downstream user industries.

The enhanced monitoring and crisis-preparedness framework addresses the Union's gap in granular and timely information that limits its ability to detect vulnerabilities and coordinate responses (SO4). The **Business-to-Business Semiconductor Supply Chain Platform** provides the intelligence required for effective early-warning, preparedness and mitigation strategies.

The preferred option is consistent with Articles 173(3) and 114 TFEU, as its core measures address challenges that Member States cannot resolve alone without fragmenting the internal market. Strategic Projects require EU-level coordination and pooled funding to ensure that new manufacturing, design and packaging capacities strengthen the Union's strategic position in a coherent and complementary manner, avoiding duplication of efforts. Likewise, demand-side instruments function effectively only at Union scale; without common frameworks, divergent national incentives would risk distorting competition and weakening the internal market for advanced technologies.

The enhanced monitoring and crisis-preparedness framework reflects the need for Union action: semiconductor supply chains are cross-border, and only an EU-level Platform can provide the integrated visibility necessary for timely and proportionate responses. These measures are proportionate, as they introduce obligations only where voluntary cooperation has proven insufficient, target well-defined market failures and apply strict safeguards to information requirements. The Call for Evidence respondents called for strengthened industry-government dialogue and a more prominent role for the ESB to improve strategic coordination. This feedback supports the governance enhancements envisaged under the

²⁰⁹ For further information, see Annex 5.

preferred option, including improved coordination, transparency and preparedness, without fundamentally altering the institutional architecture.

The expected impacts of the preferred option reflect its targeted and strategic nature. Economically, it supports the **deployment of critical manufacturing and design capabilities**, enhances ecosystem depth and reduces disruption-related losses through strengthened intelligence. Socially, it contributes to the creation of **highly skilled employment with high wages** and creates **improved conditions for innovation**, including for SMEs and start-ups. Environmentally, while expanded capacity increases absolute resource use, new facilities are expected to operate with higher efficiency.

8.2 Implementation

8.2.1 Strategy for implementation

For the Union to address its dependencies it must take a two-fold approach:

- **Strengthen our strengths** – delivered by the first Chips Act, which mobilised EUR 80 billion in manufacturing investments aligned with the needs of European user industries, and reinforced Europe's world-class Research and Technology Organisations through an unprecedented EUR 2.5 billion investment in pilot lines. This shall continue through the implementation of initiatives similar to the ones undertaken under the first Chips Act.
- **Venture into new markets** – by fostering a new generation of European semiconductor companies and helping them scale. This is increasingly important as AI and robotics diffuse across society and industry. Meeting the resulting demand for compute, both in centralised data centres and at the edge, will create new markets and application areas. Capturing these opportunities will depend on disruptive innovation, which is typically difficult for incumbents to deliver at speed. By venturing into new markets across the semiconductor value chain, particularly for more leading-edge technologies, the Union will then create the conditions for manufacturing capacity to increase which in turn would strengthen security-of-supply and resilience.

When operating in tandem, the tools set out in PO2, notably increased RDI investment (PM1), Strategic Projects (PM9) and Innovation Procurement (PM10) complemented by the existing measures under the Chips Act such as the Design Platform and the Chips Fund, create new opportunities to deliver the second part of the approach.

8.2.1.1 Scaling-up a new generation of European semiconductor market actors

The new measures proposed in PO2 allow for the creation of new companies and the de-risking of development of new technologies across the value chain from specialised materials to design to the deployment of process technology in new foundry capacity. This is a vital pre-requisite to re-instil dynamism into the European semiconductor ecosystem.

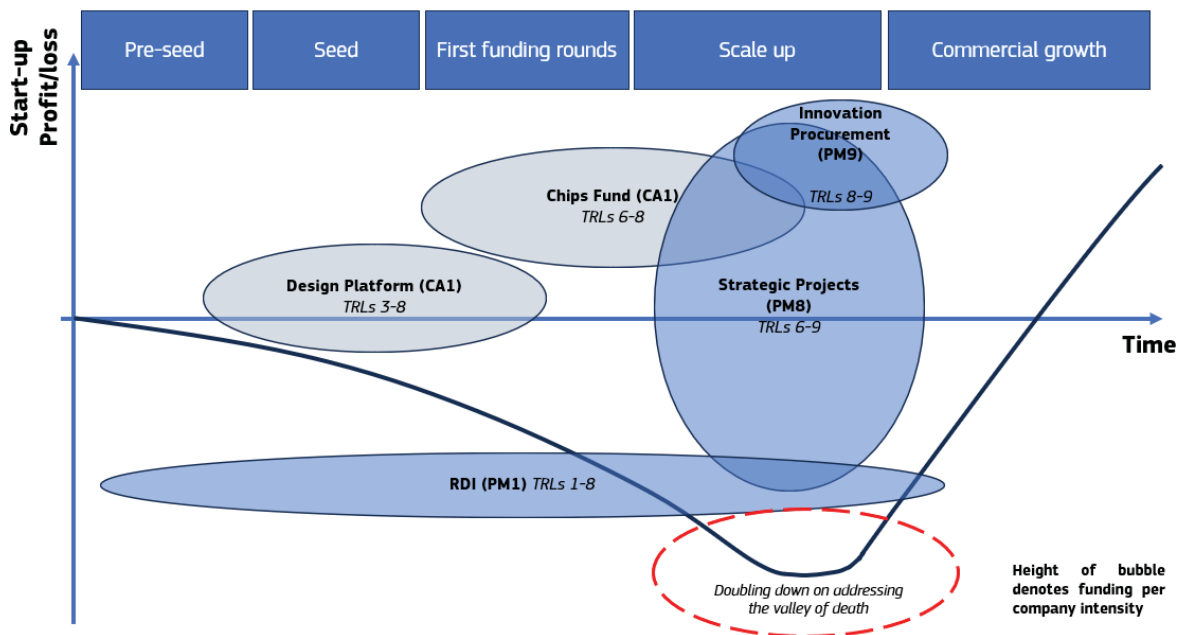


Figure 20 - Chips Act 2: A more comprehensive toolbox for scaling up semiconductor start-ups

The measures proposed in Chips Act 2 provide all the elements required for a concerted European effort to support a sovereign semiconductor industry - starting from research (**PM1**) to industrial deployment via Strategic Projects (**PM8**) and eventually also demand stimulation via innovation procurement (**PM9**).

These measures can be applied to a wide variety of contexts, but for the sake of example, they will be applied for the case of the development of a sovereign European AI Inference chip. A potential approach is foreseen as follows:

PM1 would support basic and applied research in the development of new breakthrough technologies, and foster innovation, addressing different computing paradigms and process technologies.

Once this technology is proven to a sufficient level, industrialisation could be potentially supported as a Strategic Project via **PM8**. Eventually support for innovation procurement via **PM9** would be granted, which creates predictable demand with anchor customers and enables reference deployment of EU chips in strategic segments, starting with AI Factories and Gigafactories driving internal demand for advanced AI chip design. At the same time, industrial accelerators will convert pilot-line outputs into user-ready solutions. The above can be applied to different sectors, such as automotive, defence, telecom and critical infrastructure.

Public authorities may also prioritise the procurement of this sovereign solution via non-market criteria in **PM10**, creating a structural premium for secure supply and protecting EU downstream sectors from future dependency risks.

With sufficient private co-investment and buy-in (which would always be the vast majority of investment), such a combination of measures would represent a complete system of intervention that could lead to the nurturing of commercially viable European solutions.

With sustained investment, a critical mass of emerging semiconductor companies could be built. These firms would be positioned to seize the opportunities set out in Section 1.1 and to capture demand from an era of expanding AI data-centre capacity and the mass adoption of robotics.

As seen in **Figure 21**, data centre demand is expected to increase at a rate of 12% per year – reaching 62GW in 2036. Taking a general assumption that one GPU consumes approximately 1kW of energy ⁽²¹⁰⁾ – this would imply around 62,000,000 chips which represents a significant demand that could potentially be tapped into by European actors.

Furthermore, the ongoing deployment of AI Factories and the planned investment in AI Gigafactories, backed by the EUR 20 billion in the InvestAI facility and envisaged to support up to five facilities, are another example of upcoming deployment of AI compute infrastructure. Under this initiative, the ambition is to deploy 5 datacentres with 100MW of compute capacity each.

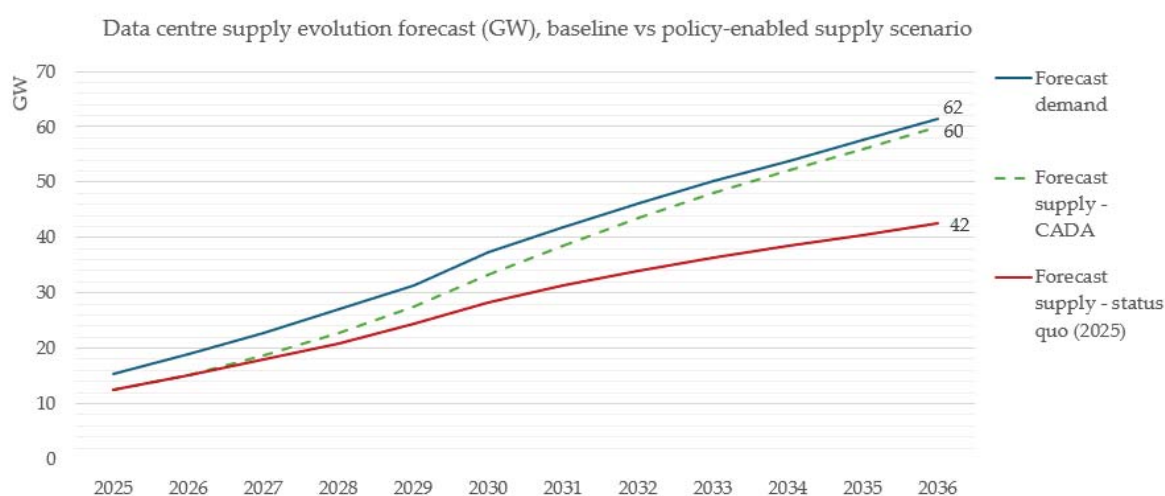


Figure 21 - Evolution of the gap between data centre demand and supply (figures in GW)

Source: Technopolis

The AI Gigafactories as a publicly steered initiative can serve as an important vehicle for the validation of European technologies. Here, **PM9** may be deployed for the procurement of experimental European technology for validation purposes through pre-commercial procurement and public procurement of innovation. Should 5% of the capacity of the AI Gigafactories be dedicated to the validation of European solutions, this would serve as an opportunity to deploy 25 MW of compute capacity that is European sourced.

²¹⁰ [Nvidia turns up the AI heat with 1,200W Blackwell GPUs | The Register](#)

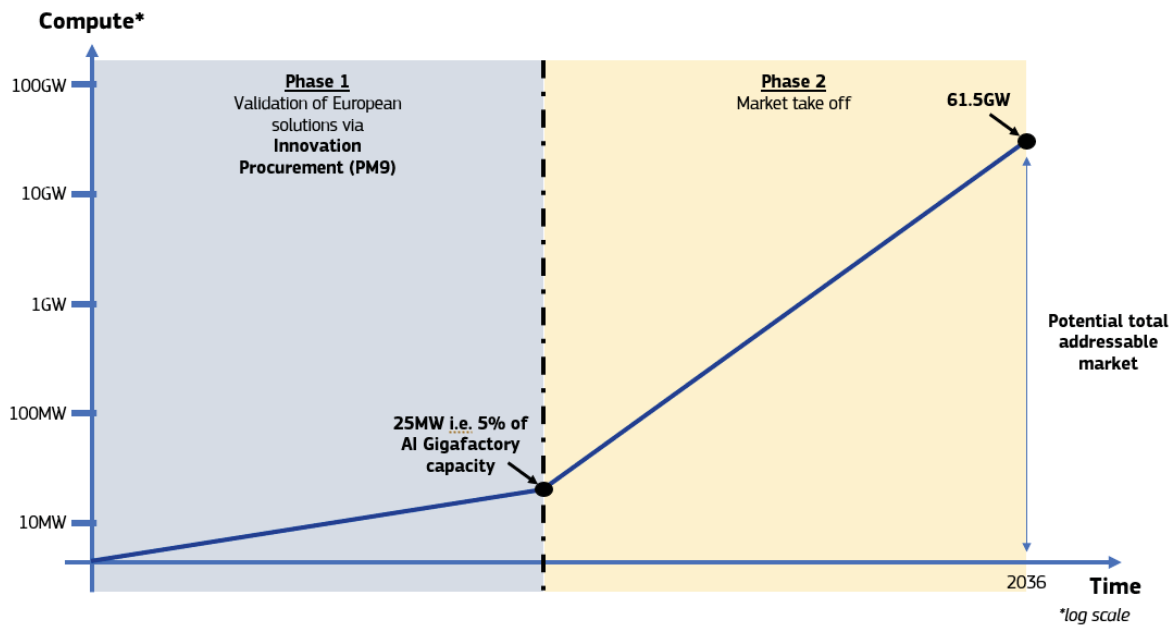


Figure 22 - Uptake of sovereign EU AI compute

This validation would then in turn give these market actors credibility on the market which can be used to pursue the larger EU data centre market and also compete globally.

8.2.1.2 Embedding resilience – selective investments on crucial components of the value chain

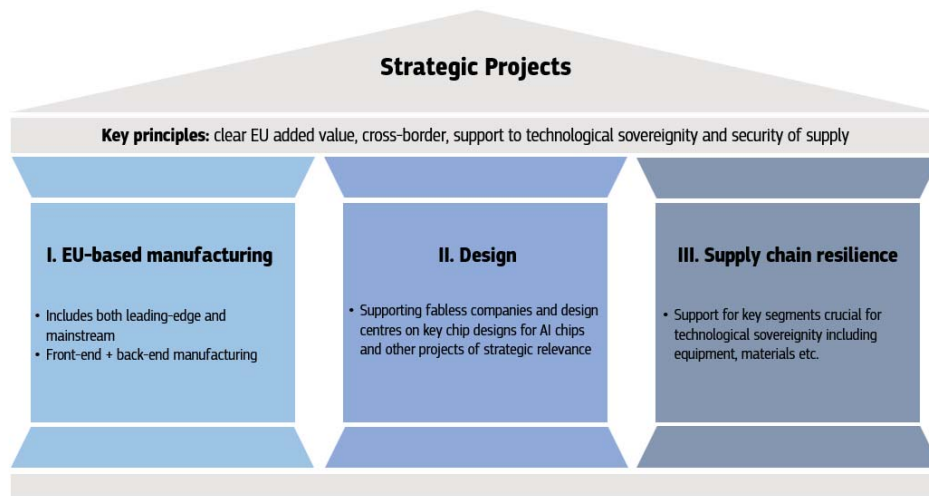


Figure 23 - Architecture of Strategic Projects (PM9)

As set out above, the EU, despite some strengths, has significant dependencies across all the semiconductor value chain. Re-shoring the entire value chain, is neither realistic nor desirable and therefore this necessitates that choices are made.

Crucial amongst these is the lack of leading-edge front-end manufacturing capacity and an advanced packaging facility together with some meaningful manufacturing capacity in memory technologies in Europe which are core-components of an AI value chain. Addressing

such vulnerabilities shall be a principal pursuit when implementing the revised Chips Act for two reasons:

8.2.1.2.1 Crucial strategic importance

Firstly, supply disruption of these semiconductors would deny Europe the possibility to deploy crucial AI infrastructure, both at the edge and in the data centre, which in the medium term will be of vital importance for the maintenance of economic growth and the functioning of essential societal services and industry.

Furthermore, the increasingly differentiating factor that this technology could have when it comes to security and defence, including cybersecurity, means that lack of sovereign access may render Europe vulnerable to violations of public order and security.

8.2.1.2.2 Market opportunity

Secondly, this segment of leading-edge technologies is the fastest growing segment in the semiconductor market. It is the driver of unprecedented growth in the industry that is expected to reach USD 1 trillion in revenues by 2026, an acceleration of 4 years from the consensus of market analysts. **Europe's lack of participation in this segment is resulting in a rapid loss of market share and risks rendering the EU irrelevant in the global semiconductor market.**

Recent evidence indicates that leading-edge AI chip markets are characterised by short-run capacity constraints and limited price responsiveness. For example, advanced 2.5D packaging capacity, particularly TSMC's Chip-on-Wafer-on-Substrate (CoWoS) platform used for frontier AI chips, has been reported as sold out through 2025 and into 2026, with oversubscription at least until mid-2026.⁽²¹¹⁾ When it comes to front-end manufacturing, it is expected that foundry capacity will be scarce until at least end of 2027 and will probably persist as data-centre and AI compute demand increases exponentially, with foundries not being able to keep abreast.

Category	Logic node	Product	2026 Q1	2026 Q2	2026 Q3	2026 Q4	2027 Q1	2027 Q2
Logic	≤2nm	Accelerator	90	80	72	76	80	84
Logic		CPU	77	75	73	77	81	87
Logic	5/4/3nm	Accelerator	74	76	80	85	89	93
Logic		CPU	76	80	87	90	92	94
Logic	7nm	Miscellaneous products	82	81	79	81	84	86

Figure 24 - Percent of supply versus demand for semiconductors (Source: IBS)²¹²

⁽²¹¹⁾ Fusion Worldwide. (2025). *Inside the AI bottleneck: CoWoS, HBM, and 2/3nm capacity constraints through 2027*. <https://info.fusionww.com/blog/inside-the-ai-bottleneck-cowos-hbm-and-2-3nm-capacity-constraints-through-2027>

⁽²¹²⁾ IBS, Global Semiconductor Industry Service February 2026 - Analysis of Semiconductor Shortages.

Therefore, given multi-year expansion lead times, short-term output is effectively capacity-bound. In such conditions, price increases do not rapidly translate into higher quantities, implying a steep short-run supply curve. Demand has also proven resilient: despite elevated prices during the constraint phase, deployment of frontier AI hardware did not materially contract, suggesting limited short-run substitutability and strong willingness to pay among cloud vendors and AI companies.

Furthermore, investment in manufacturing capacity via Strategic Projects for more mature technologies that are of critical importance for certain user industries such as automotive and security and defence will be pursued to continue building resilience for European user industries.

8.2.2 Budget

All funding assumptions are without prejudice to ongoing negotiations related to the next Multiannual Financial Framework (MFF) for 2028-2035. The considerations made in the Impact Assessment are in line with the Commission proposal for the next MFF.

It is assumed that Member States are willing to co-fund. This is a reasonable assumption given the level of attention the topic has received, including the adoption of national strategies in over 10 Member States. ⁽²¹³⁾ This assumption is also based on previous budget allocations by Member States over the course of the current MFF (2021-2027).

Considering the nature of the initiative, effectiveness is tied to the capacity of public authorities, including the Commission, to invest. The funding from the Union is also subject to the specificities of the upcoming Council regulation establishing the Joint Undertakings. The preferred option (PO2) is based on the assumption that the Union will be able to mobilise sufficient funding for an impactful application of the new policy measures foreseen under the proposed Chips Act. Of course, an important change in this revision will be the role of the Union in supporting strategically important manufacturing facilities. This would require at least an order of magnitude larger EU budget for semiconductors in the next MFF. Should these budgets not be realisable, then the impacts described in Section 6.2 will be more subdued.

8.2.3 Total cost benefit overview

The preferred option is expected to generate substantial economic returns across the semiconductor value chain, with EU manufacturers projected to achieve **EUR 6.6–11.5 billion (for total of EUR 40 billion public private funding)**⁽²¹⁴⁾ in additional annual manufacturing revenue from Strategic Projects, while demand-side measures stimulate further design-related activity and crowd in private investment (see Annex 4). Public authorities stand to benefit from a significantly strengthened governance architecture, including, for the first time, direct EU co-financing of industrial deployment via the ECF, alongside new

⁽²¹³⁾ Austria, Czech Republic, Finland, France, Germany, Ireland, Italy, Netherlands, Poland, Portugal, Spain.

⁽²¹⁴⁾ The EUR 40 billion figure is provided for illustrative purposes only.

resilience capabilities that would allow the industry to identify supply chain bottlenecks before the crisis thresholds set out in the Chips Act are reached.

The total costs associated with the preferred option are proportionate and are substantially outweighed by the projected economic benefits, improved supply chain resilience, with SMEs fully exempt from reporting obligations.

Society at large would stand to benefit from improved continuity of essential services during supply disruptions, reduced exposure to geopolitical coercion, the creation of at least **7,300 direct and 36,500 indirect jobs**, and, over time, greater product choice and more competitive pricing for all downstream users of semiconductors. Further information can be found in Annex 3.

8.3 REFIT (simplification and improved efficiency)

The preferred option introduces targeted new obligations but also delivers notable simplification and efficiency gains for businesses and public administrations.

8.3.1 Simplification benefits

The preferred policy option (PO2) delivers simplification by introducing a coordinated EU-level framework in the case of Strategic Projects. With a single project pipeline for large-scale semiconductor investments, duplication of administrative steps and repetitive documentation are prevented. The clarification of the First-of-a-Kind label further simplifies State aid procedures for both Member States and companies. Additionally, the revised Chips Act will delete the concept of a European Chips Infrastructure Consortium (ECIC) for streamlining purposes as it was never used during the implementation of the Chips Act.

Another efficiency gain stems from faster and more predictable permitting procedures. Permitting and design phases for advanced semiconductor facilities in the EU are on average 7.5 months longer than in key competing jurisdictions. Assuming that each year of delay adds around 5% to the total project value, this implies an additional cost of approximately 3.125% of overall investment, corresponding to around EUR 625 million for a representative EUR 20 billion advanced fabrication plant. ⁽²¹⁵⁾ By reducing iterative exchanges with authorities and clarifying permitting pathways, PO2 generates substantial implicit cost savings that outweigh compliance-related costs. Another simplification benefit arises from replacing ad hoc crisis-driven information requests with a structured **Business-to-Business Semiconductor Supply Chain Platform** reducing duplication and improving coordination across Member States. ⁽²¹⁶⁾

8.3.2 Administrative impacts (OIOO perspective)

From a One-In-One-Out perspective, PO2 introduces limited new administrative burdens, largely offset by structural simplification. New “INs” for businesses consist primarily of disclosures of supply chain vulnerabilities, estimated at up to 10 person-days per request,

⁽²¹⁵⁾ Annex 3, Table III (Application of the ‘one in, one out’ approach).

⁽²¹⁶⁾ Annex 3, Table I – Improved visibility of supply chain vulnerabilities.

corresponding to approximately EUR 2,783 per large firm, with total costs of up to EUR 1.34 million per request in a full-coverage scenario. ⁽²¹⁷⁾ These burdens are counterbalanced by “OUTs” in the form of fewer urgent and duplicative crisis-related data calls, streamlined information exchange and reduced internal monitoring effort through partial outsourcing of market-intelligence activities to the Platform. Businesses face a net administrative burden, consisting of onboarding the Platform and disclosures. However, these will be largely offset by the security of supply that this data sharing will enable. Additionally, assessments will only be made on a qualitative basis outside of a formal crisis in the first stage. Overall, PO2 results in a small net administrative burden, which is proportionate, REFIT-compliant and clearly outweighed by the simplification and efficiency gains delivered.

Better alignment of IPF/OEF procedures for projects that receive public funding and meet the requirements reduces administrative burden, shortens timelines, and enables Member States and the Commission to allocate resources more efficiently.

9 HOW WILL ACTUAL IMPACTS BE MONITORED AND EVALUATED?

The Commission will be responsible for monitoring the implementation of the intervention on a regular basis, possibly with the support of external studies, Member States and market data. Furthermore, the Commission will carry out a comprehensive evaluation of the effectiveness, efficiency, coherence, proportionality, and subsidiarity of Chips Act 2. **An evaluation report** presenting the main findings will be submitted to the European Parliament, the Council, the European Economic and Social Committee, and the Committee of the Regions within **four to five years** of the act entering into force. Where appropriate, the Commission may accompany this report with proposals for improving or adapting the Chips Act 2.0.

This review mechanism follows the approach established under the first Chips Act, ensuring continuity, comparability of results, and a long-term perspective on policy results. The Commission, in close cooperation with the Member States, will regularly monitor the implementation and application of the legal provisions, with particular attention to the effectiveness of the adopted measures. Monitoring activities will rely on quantitative and qualitative indicators, drawing from data provided by stakeholders across the semiconductor value chain, Member States, and relevant EU bodies. The overall success of the initiative will be assessed through evidence of strengthened **security of supply**, including progress in relevant measurable aspects such as the EU’s share of global semiconductor production and changes in market concentration. The implementation of Chips Act 2.0 itself and its accompanying measures will also allow for systematic tracking of specific objectives, expected benefits, and related impacts.

9.1 Measurable indicators to monitor the implementation and to report on the progress of the initiative towards the achievement of its objectives

The proposed indicators build on the two new general and specific objectives of the Chips Act 2.0.

⁽²¹⁷⁾ Annex 3, Section II and Table III.

Monitoring indicator for general objectives:

- Total semiconductor related FDI inflows into the EU;
- Skilled workforce in semiconductor and photonics, including workforce trained or reskilled through the competence centres under Pillar I;
- Public support for start-ups and scale ups;
- Scale-up funding via private equity and venture capital.

Monitoring indicators for specific objectives

SO1: Enhance the capacity, security of supply and competitiveness of the EU semiconductor industry across the value chain, including for leading-edge AI chips

The first specific objective seeks to enhance the EU's capacities and security of supply for semiconductors in sectors relevant for the Union's economic security and competitiveness by steering larger and more targeted public and private investments.

Monitoring indicator for SO1:

- EU share of global semiconductor revenues (in EUR) in different segments of the value chain including:
 - Design, IP, EDA
 - Manufacturing
 - Equipment manufacturing
 - OSAT (packaging)
 - Materials / gases
- Top European firms in any value chain segment.
- Operational wafer fabrication capacity in the EU (wspm).

SO2: Develop a strong user market across key industry sectors

The second specific objective is designed to ensure the emergence of a robust and innovative end users' market in the Union ready to adopt new advanced semiconductor technologies, notably for AI chips.

Monitoring indicator for SO2:

- Consumption of chips by key sectors (automotive, energy, health, defence, telecom, AI/data centres/cloud) in value (EUR).

SO3: Increase intelligence capabilities for crisis preparedness and response

Finally, increasing monitoring capabilities should ensure EU's agile, effective, and proactive response prior to a semiconductor crisis. When the EU's economic security is at risk, real-time information and data from companies across the semiconductor supply chain and end-user markets can provide critical insights and enable mitigation or emergency measures at Union or national level.

Monitoring indicator for SO3:

- Coverage by the Business-to-Business Semiconductor Supply Chain Platform (in %) of the Union semiconductor value chain.



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PART 2/3

COMMISSION STAFF WORKING DOCUMENT

IMPACT ASSESSMENT REPORT

Accompanying the document

**Proposal for a Regulation of the European Parliament and of the Council
on a framework of measures for strengthening Europe's semiconductor ecosystem
repealing Regulation (EU) 2023/1782 (Chips Act 2.0)**

{COM(2026) 504 final} - {SEC(2026) 504 final} - {SWD(2026) 505 final}

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ANNEX 1: PROCEDURAL INFORMATION

1. LEAD DG, DECIDE PLANNING/CWP REFERENCES

This Staff Working Paper was prepared by the Directorate-General for Communications Networks, Content and Technology.

The Decide reference of this initiative is PLAN/2025/2008.

This includes the Impact Assessment report as well as, annexed to the report, the Evaluation of the Chips Act.

2. ORGANISATION AND TIMING

The Impact Assessment was prepared by DG CONNECT as the lead Directorate-General.

The Inter-Service Steering Group established for the work streams on online platforms was associated and consulted in the process, under the coordination of the Secretariat-General, including the following services: DG BUDG (DG Budget), DG CLIMA (DG Climate Action), DG COMP (DG Competition), DG DEFIS (DG Defence Industry and Space), DG ECFIN (DG Economic and Financial Affairs), DG EMPL (DG Employment, Social Affairs and Inclusion), DG ENV (DG Environment), DG FISMA (DG for Financial Stability, Financial Services and the Capital Markets Union), DG GROW (DG Internal Market, Industry, Entrepreneurship and SME), DG HERA (DG Health Emergency Preparedness and Response Authority), DG INTPA (DG International Partnerships), JRC (Joint Research Centre), DG MOVE (DG Mobility and Transport), DG RTD (DG Research and Innovation), DG Regio (DG Regional and Urban Policy), DG TAXUD (DG Taxation and Customs Union), EEAS (European External Action Service).

The Secretariat-General and DG CNECT of the European Commission relaunched the Interservice Group for the revision of the Chips Act on the 15th of July 2025. The Group was iteratively consulted on the Impact Assessment of the draft proposal, the Evaluation of the Chips Act and on the key policy measures in the proposed regulation.

3. CONSULTATION OF THE RSB

The Regulatory Scrutiny Board (RSB) hearing took place on 28 January 2026. Following a first negative opinion, the RSB Board gave a positive opinion with reservations on the 30th of March. To address the feedback given by the Regulatory Scrutiny Board, the following changes were made in the Impact Assessment report and its annexes:

Findings of the Board	Main modifications made in the report to address them
(1) The measure to incentivise trusted chips is not sufficiently described to allow for the assessment of impacts.	The measure to incentivise chips in public procurement (policy measure 10) was revised into “ <i>Recommend a security of supply declaration for semiconductors in public</i> ”

	<i>procurement”.</i> Concretely, the revised PM10 would allow public procurement authorities in critical sectors to request from tenderers a supply chain declaration analysing the provenance of semiconductors in the tendered products, outlining their supply chain resilience strategy, in particular with regards to dual sourcing. The declaration would also need to assess the quota of semiconductors supplied from domestic undertakings or equivalent¹. The public procurement authorities may use the supply chain resilience strategy as outlined in the declaration, and the quota of domestic or equivalent semiconductor suppliers, as award criteria along with price. (See further Section 5.2.3.3 and Section 6.2.1.3 of the main document)
(2) The report does not adequately analyse coherence with the existing and forthcoming policy initiatives and instruments. It is not sufficiently clear how interplay will be ensured to achieve synergies between the supply- and demand-side measures.	The interplay between the various measures, in particular the supply side and demand side measures, covering the whole value chain is explained in Sections 5.2, 6.2 and 8.2. Additional elements on coherence with other existing or upcoming policy measures (incl. to the CSA 2 proposal) and instruments were integrated in the report (Section 1.2).
(3) The analysis of the risk of inefficient allocation of resources is not sufficient.	The revised report assesses the costs of individual measures without prejudice to ongoing MFF negotiations. (Section 6 and Section 8; Annex 3 and Annex 4).

¹ See Article 2 of Chips Act 2.0.

ANNEX 2: STAKEHOLDER CONSULTATION (SYNOPSIS REPORT)

1. INTRODUCTION

This annex presents an overview of the five consultation activities: the open public consultation (OPC), call for evidence, surveys, expert interviews, and workshops. In line with the Terms of Reference and the Commission's Better Regulation Guidelines, it summarises findings across the evaluation criteria (effectiveness, efficiency, coherence, EU added value, and relevance), as well as prospective outcomes. This annex presents the stakeholder consultation findings and clarifies how they have been incorporated into the evaluation and policy-making process.

2. OUTLINE OF THE CONSULTATION STRATEGY AND METHODOLOGY

Stakeholder consultation is the structured process through which the Commission and its contractors gather information and perspectives from stakeholders regarding the Chips Act. The consultation strategy defines the scope, identifies the stakeholder groups to be reached, and clarifies the purpose of each activity.

The approach followed the Commission's Better Regulation Guidelines and comprised three main steps:

- Designing the consultation strategy;
- Conducting the consultation activities;
- Informing policymaking through the preparation of our reports.

The consultations aimed to gather stakeholder views and collect data to address the evaluation questions. Findings are presented by consultation method and stakeholder group, and were triangulated with evidence from other data collection and analysis activities.

The consultation tools were designed to be complementary. Surveys and the call for evidence provided broad input, particularly on effectiveness and efficiency, while interviews and workshops with stakeholders (including industry, research organisations, and external experts) supported more in-depth assessment of relevance, coherence, and EU added value. The OPC covered all evaluation criteria and enabled stakeholders and the wider public to share views on the Chips Act's implementation.

Although the study provides an overall evaluation of the Chips Act, the consultation findings are presented with a forward-looking focus, reflecting stakeholder suggestions for improvement. These insights are integrated in the final evaluation report alongside evidence from other methods.

Table 1. Main information on stakeholder consultation activities

Consultation activity	Target groups	Dates
• Open public consultation	- Organisations - Individual respondents	5 September 2025 - 28 November 2025
• Call for evidence	- Organisations - Industry stakeholders - Research institutions - Public authorities - NGOs	5 September 2025 - 28 November 2025
• Survey	- National and regional authorities - Industry users - Supply chain actors - Research and design (R&D) organisations	24 October 2025 - 24 November 2025
• Interviews	- EU industries - Policymakers - Industry representatives - Key investors - Interest groups/alliances - Worker unions	4 November 2025 - 19 November 2025
• Workshops	- Industry representatives - Regional and institutional actors - Research and academic organisations - Supporting ecosystem - European Commission representatives	12 September 2025 - 17 December 2025

3. METHODOLOGICAL ADAPTATIONS AND LIMITATIONS

The consultation strategy was adapted during implementation. Initial stakeholder participation in the OPC and survey was relatively low, so additional targeted consultations were integrated into the consultation plan. Focus groups were replaced by several thematic workshops to allow broader participation. These included workshops with different stakeholder groups. With increased participation in the OPC and survey, the final consultation results reflect **a well-balanced mix of quantitative and qualitative inputs**. Besides, findings were triangulated across multiple sources, with each conclusion based on at least two independent data sources. Section 4 provides a comparison table showing consistency across consultation activities. Finally, the analysis focuses on outputs and early outcomes, reflecting the Act's recent entry into force (September 2023). Self-selection bias was mitigated through diverse methods and outreach to underrepresented groups. Limited financial data for Pillar II facilities (due to ongoing construction and confidentiality) were addressed through cost modelling and qualitative validation.

4. SUMMARISED RESULTS OF THE OPEN PUBLIC CONSULTATION (OPC)

The OPC was conducted over a **12-week period, from 5 September 2025 to 28 November 2025**. The questionnaire consisted of five sections covering respondent identification, views on the functioning of the current Chips Act, perspectives on possible future steps under a potential "Chips Act 2.0", stakeholder-specific questions, and an option to upload supporting documents. The open public consultation was available in all 24 EU official languages. It included both closed-ended and open-ended questions, allowing respondents to elaborate on their views. In total, **105 survey responses and 39 position papers** were received. One response was identified as a duplicate and another as a test submission; both were excluded, resulting in 103 responses included in the analysis.

The **statistical analysis of closed consultation questions** combined high-level aggregation with disaggregated insights by stakeholder group, enabling the identification of emerging trends within specific groups and helping to contextualise broader patterns across responses. To

facilitate the analysis, more granular stakeholder categories were clustered into higher-level groups.

The **qualitative analysis of open-ended responses and position papers** used a hybrid approach, combining Large Language Model (LLM)-driven topic modelling with expert human validation to ensure a structured, consistent, and robust synthesis of stakeholder input across all evaluation criteria.

Two **organised campaigns** with 21 contributions were identified, primarily representing stakeholders from the European semiconductor and electronics ecosystem, including the EuroPractice consortium. Although campaign respondents did not submit identical answers to the closed questions, they repeated key messages across multiple open-ended questions; their inputs are therefore included in the closed-question analysis. The campaigns emphasised that revising the EU Chips Act must sharpen Europe’s strategic focus on semiconductor innovation, industrial deployment, and competitiveness by improving funding tools, reducing bureaucracy, and strengthening collaboration across the value chain.

The OPC was answered predominantly by **organisations** (84%, 87/103), with **individual respondents** comprising 16% (16/103). Most responding organisations were international in scope (74%, 64/87) and primarily large enterprises with ≥ 250 employees (51%, 44/87), although medium (22%, 19/87) and small enterprises (21%, 18/87) were also represented.

Geographically, responses came **mainly from EU Member States** (91%, 94/103), with Germany contributing the most (26), followed by France (16) and Italy (10). Non-EU participation was limited to 9 responses, primarily from the United States (3) and Switzerland (2). Among individual respondents, a clear majority held EU nationality (88%, 14/16).

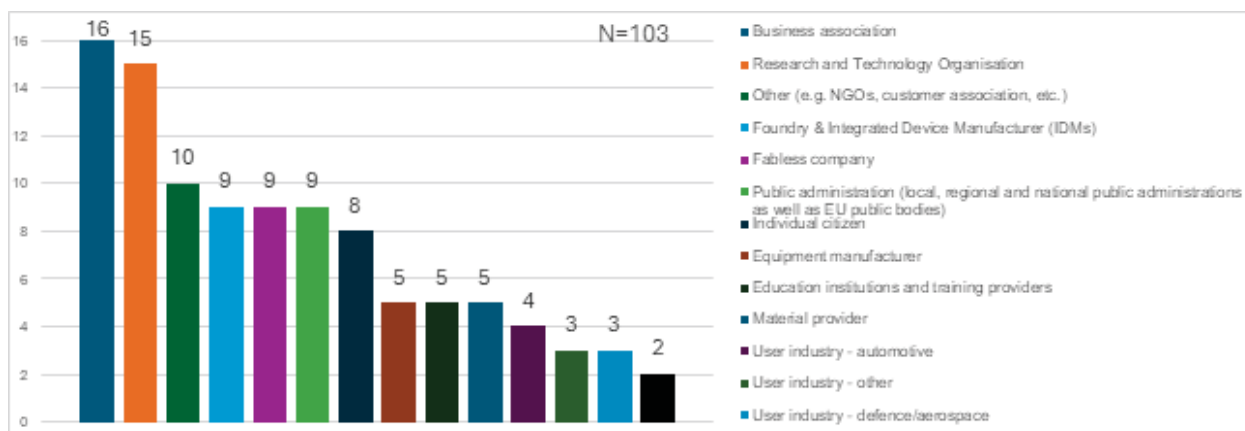


Figure 1. Stakeholder types

Source: Consolidated public consultation of the review of the Chips Act, September-November 2025, Question 2.

4.1. Effectiveness

The consultation results indicate strong positive assessments of **Pillar I (Chips for Europe Initiative)** across all stakeholder groups. Supporting research and innovation activities was the highest-rated objective, while progress on security-by-design principles for cybersecurity protection ranked somewhat lower in comparison. Position papers broadly align with these trends, with stakeholders consistently identifying Pillar I activities, such as pilot lines, competence centres, and start-up support, as having strengthened Europe’s innovation

infrastructure and supported technological capacity building. Concrete examples cited include support for start-ups and local benefits such as job creation.

Regarding **pilot lines** specifically, more than half of respondents (59%, 56/96) considered that they meet their objectives of supporting the transition from ‘lab to fab’, with RTOs/designers (76%, 13/17) and authorities (78%, 7/9 respectively) expressing the strongest positive views, while civil society and supply-chain respondents were more cautious. Answers to open-ended questions suggest that further industrialisation of pilot lines could be supported through state-aid framework reform (GBER revision) and sustained funding support, while end users highlighted the importance of market-driven orientation from the outset. Across sources, stakeholders note that closing the gap between innovation and industrial-scale production remains crucial to achieve high-volume production capabilities.

Competence Centres are broadly viewed as too early to assess fully, though some respondents representing RTOs/designers raised questions about inclusiveness for regional actors and noted operational considerations including budget constraints (civil society and economic stakeholders) and non-unified service costs (public authorities). When asked about other activities that could be covered, most stakeholders suggested waiting until centres become fully operational before expanding their remit.

At the same time, stakeholders express doubt that the 20% market share target is realistic under current conditions. Overall, position papers **characterise the Chips Act as a timely crisis response that created important momentum**, while emphasising that Europe now requires substantially scaled and more comprehensive intervention to achieve meaningful strategic outcomes.

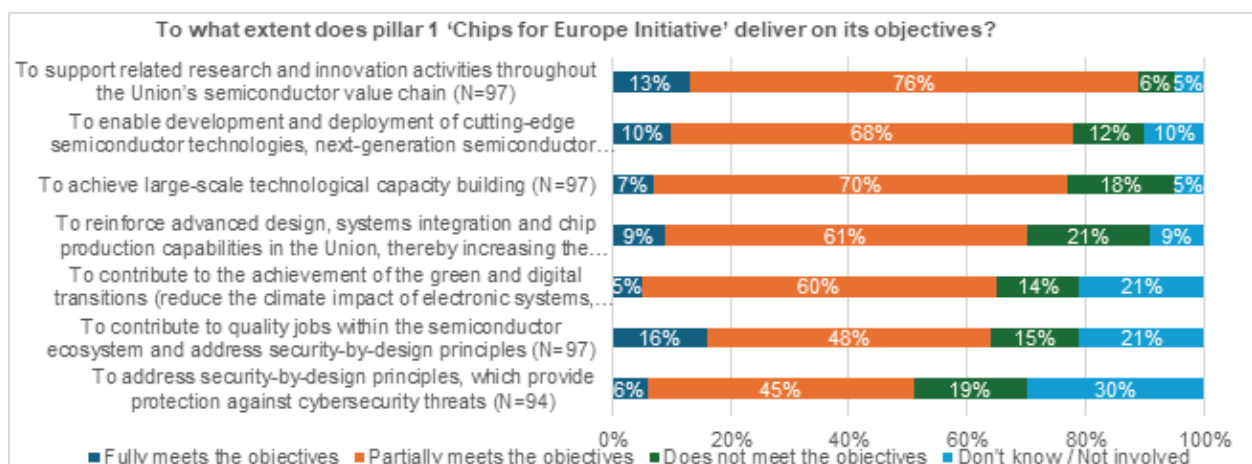


Figure 2. Achievement of Pillar I objectives

Source: Consolidated public consultation of the review of the Chips Act, September-November 2025, Question 6.

Pillar II (Security of supply and resilience) also received broadly positive assessments. Three quarters of respondents (75%, 60/97) considered that this Pillar fully or partially meets its objectives, with supply-chain respondents (70%, 19/27) and end users (67%, 8/12) expressing the strongest positive views, while authorities were more cautious 44% (4/9). A similarly large majority (71%, 69/96) indicated that Pillar II has made the EU a more attractive location for semiconductor manufacturing. Position papers note that while the Chips Act has mobilised substantial investment, questions remain about whether current funding levels are sufficient to keep pace with global competitive dynamics. Stakeholders also identify gaps in the value chain, including Europe’s PCB manufacturing capacity and back-end manufacturing, which are

perceived as undermining front-end investments and contributing to dependencies on non-European suppliers.

Pillar III (Monitoring and crisis response) received comparatively lower assessments. Almost a third of respondents (30%, 29/96) considered that Pillar III fully or partially meets its objectives, with an equal share indicating that objectives are not met. End users and civil society/economic stakeholders expressed the strongest positive views (each 33%, 4/12 and 11/33), while authorities reported the lowest (22%, 2/9). Current uptake of monitoring mechanisms remains limited: two-thirds of respondents (66%, 61/93) reported they had not developed or implemented monitoring systems within their organisations, and a similar proportion (66%, 57/86) indicated they have never reported or received alerts about potential supply chain disruptions. When asked in open-ended questions about suggested additions and changes to Pillar III, there was broad agreement across stakeholders that the Pillar requires further development beyond its current focus on shortage management, with supply-chain stakeholders highlighting practical concerns around information-sharing and export control frameworks.

Regarding chip supply shortages over the past 12-24 months, respondents most commonly reported experiencing shortages in final chips (39%, 22/57) and raw materials (26%, 15/57).

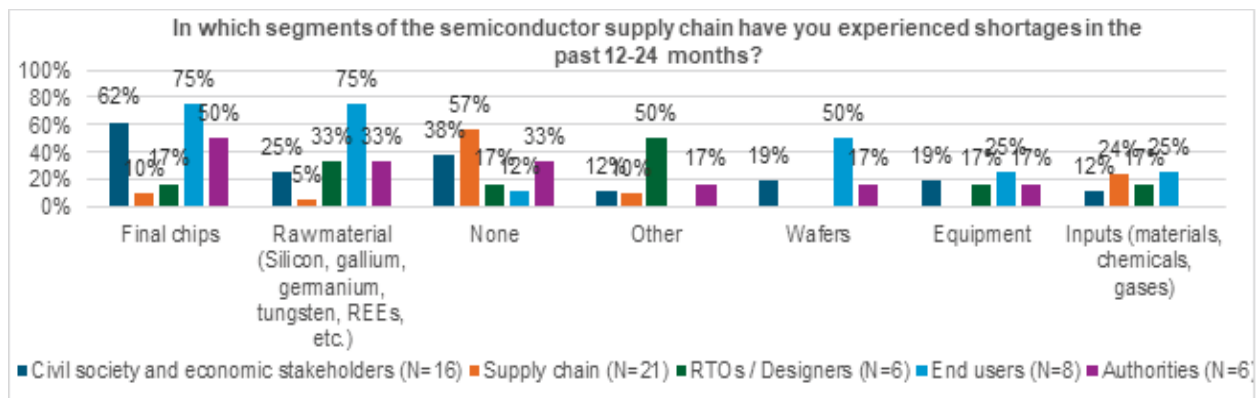


Figure 3. Supply shortages

Source: Consolidated public consultation of the review of the Chips Act, September-November 2025, Question 26.

Looking ahead at the next 2-3 years, a large majority (83%, 68/82) of respondents anticipate further disruptions. Geopolitical risks (82%, 64/78) and new trade barriers (81%, 63/78) emerged as the most frequently cited **threats** across stakeholder groups, followed by logistic bottlenecks (35%, 27/78) and natural hazards (26%, 20/78). Position papers echo these concerns, with stakeholders observing that Europe's relevance as a semiconductor market has declined relative to other regions, and that capacity gaps in advanced manufacturing nodes leave the EU reliant on a narrow base of non-European suppliers.

Respondents most widely supported diversifying trade partners (83%, 71/86) as a **mitigation measure** across all stakeholder groups, followed by investing in innovation for recycling, advanced materials or substitutes (73%, 63/86). Nearly two-thirds (65%, 51/79) considered it useful to introduce protective measures for the Union's semiconductor sector in the event of a crisis.

Communication effectiveness was assessed positively overall. A large majority (86%, 77/89) indicated that the implementation of the Chips Act has been communicated at least adequately within their relevant Member States, with broadly consistent views across stakeholder groups.

4.2. Efficiency

Experiences with implementation mechanisms varied considerably across stakeholder groups. Among fabless companies who engaged with EU-level initiatives, perceptions were mixed, with equal shares finding them not effective or somewhat effective (each 33%, 3/9). Among RTOs, 67% (6/9) reported having been part of one of the five pilot line projects under Pillar I. Most foundry and integrated device manufacturers rated their experience with the first-of-a-kind framework under Pillar II as neutral or satisfactory (each 44%, 4/9), though two-thirds (67%, 6/9) had not applied for integrated production facility or Open EU foundry status.

Position papers and answers to open-ended questions provide further insight into the challenges underlying these mixed experiences. A consistent finding across stakeholder groups is **concern about procedural complexity and slow timelines**. Stakeholders identify state aid approval delays, IPCEI and FOAK process complexity, administrative burden, and inconsistent pilot line access conditions as key efficiency barriers. The length of state aid approval processes is the most prominent concern, with stakeholders noting that timelines of up to two years from submission to grant notification create uncertainty and represent a competitive disadvantage relative to other semiconductor-producing regions. IPCEI is recognised as a valuable instrument, though its efficiency is seen as constrained by approval timelines, administrative complexity, and funding rates that are perceived as less competitive compared to global counterparts. Respondents also noted that Member States retain primary authority over planning and licensing processes, which can affect permit timelines.

Public authority involvement in supporting semiconductor development varies across functions. Among authority respondents, 67% (6/9) indicated they provide specific incentives to the semiconductor value chain, while 44% (4/9) have been involved in facilitating first-of-a-kind facility investments. Two-thirds (67%, 6/9) reported that their authority has developed a semiconductor strategy at national, regional, or local level. All authorities expressed interest in supporting strategic projects in line with the Commission's proposal for a European Competitiveness Fund.

Regarding **coordination and financing**, three quarters of respondents (75%, 64/85) indicated that strategic project selection and set-up should be coordinated at EU level, with strong cross-stakeholder consensus. A large majority of all respondents (87%, 74/85) favoured financing through a combination of funding sources. In their open-text responses, several respondents representing RTOs/designers highlighted the need to align support with market demand, noting that EU awards alone may not guarantee commercial viability. In terms of beneficial incentives for companies, end-user industry respondents particularly favoured financial support for R&D (89%, 8/9), subsidies for building manufacturing facilities (89%, 8/9), and tax incentives for chip production and usage (78%, 7/9).

4.3. Coherence

A large majority of respondents (86%, 58/67) reported that the **Chips Act has contributed to improving governance and coordination between national and regional authorities**, with 9% (6/67) indicating it contributed very well, 16% (11/67) well, and 61% (41/67) adequately. The strongest positive views came from authorities and RTOs/designers, while end users showed more mixed views. Position papers and open-ended responses indicate scope for further strengthening governance arrangements, including through more structured industry involvement in decision-making processes.

The most prominent **internal coherence** concern identified in position papers is the relationship between research and innovation activities under Pillar I and manufacturing capacity under Pillar II. Stakeholders argue that innovation delivers greater value when supported by clear pathways to industrial-scale production. As DIGITALEUROPE noted, “Pillar 1 and Pillar 2 [...] must be more closely integrated. Innovation generated in Pillar 1 only delivers real value when it transitions into industrial-scale manufacturing under Pillar 2”, a view echoed by other business associations such as Eurochambres and ESIA. Beyond internal coherence, respondents call for stronger alignment between the Chips Act and adjacent EU policy instruments, including the Quantum Act, Advanced Materials Act, EuroHPC, and EDIP, to ensure complementarity across policy domains. Stakeholders also identify a need for enhanced coordination across EU, national, and regional governance levels, with regional stakeholders emphasising that success depends on research, companies, pilot lines, centres of excellence, and public policy working closely together.

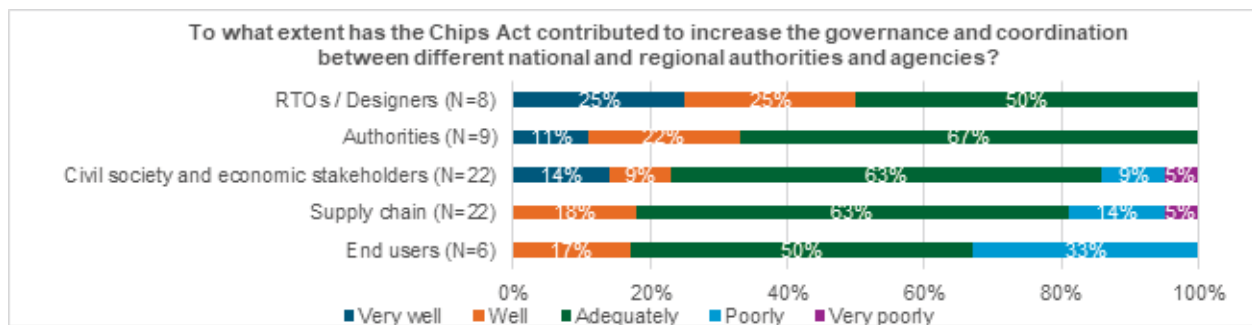


Figure 4. Impact on governance and coordination

Source: Consolidated public consultation of the review of the Chips Act, September-November 2025, Question 31.

Regarding **sustainability**, the majority of respondents (71%, 47/66) reported that their organisation has sustainable practices or policies in place for the semiconductor sector. Supply-chain actors showed the strongest uptake (85%, 17/20), while civil society/economic stakeholders (60%, 12/20) and RTOs/designers (56%, 5/9) showed more varied adoption. Among civil society and economic stakeholders, raw materials extraction was the most widely shared environmental concern (75%, 6/8), followed by high energy consumption, lifecycle assessment capabilities, and water usage. When prioritising concerns related to chips and electronic components, high energy consumption emerged as the top issue (86%, 6/7). In position papers and open-ended questions, some respondents noted potential tensions between environmental regulations and manufacturing requirements, while others observed that sustainability considerations are sometimes deprioritised relative to performance improvements and that incentives may need to target both new and existing equipment. Among business associations, the most frequently cited actions to promote sustainable practices were incentives for green manufacturing and R&D funding for eco-friendly technologies (both 85%, 11/13).

4.4. EU added value

Position papers show strong consensus that EU-level action provides irreplaceable value through coordination mechanisms that should be further strengthened. Stakeholders support a centralised EU-level strategic framework and significant EU budgetary contributions that complement Member State funding. Respondents frame EU coordination as essential for European semiconductor competitiveness, emphasising that it helps minimise fragmentation and enables scale effects that no individual Member State could achieve alone. In response to open-ended questions, authority representatives recommended the European Semiconductor Board as

the primary coordination platform, with investments planned according to European priorities and demand to ensure resilient supply chains.

Views on extending information mandates showed no unanimous position across stakeholder groups. Almost half of respondents (47%, 40/85) supported giving the European Commission or National Competent Authorities a mandate to request information from companies along the semiconductor supply chain to prevent future disruptions, with a similar share (47%, 40/86) supporting mandates to address potential vulnerabilities such as overcapacities or dependencies.

International cooperation received strong support across all stakeholder groups. Collaborative R&D and innovation was the most widely supported action area, consistently ranking at or near the top for every group, while supply chain diversification and security of supply was another cross-cutting priority. Position papers similarly call for strengthened international partnerships with key semiconductor-producing nations, proposing more formalised cooperation mechanisms and risk-based frameworks.

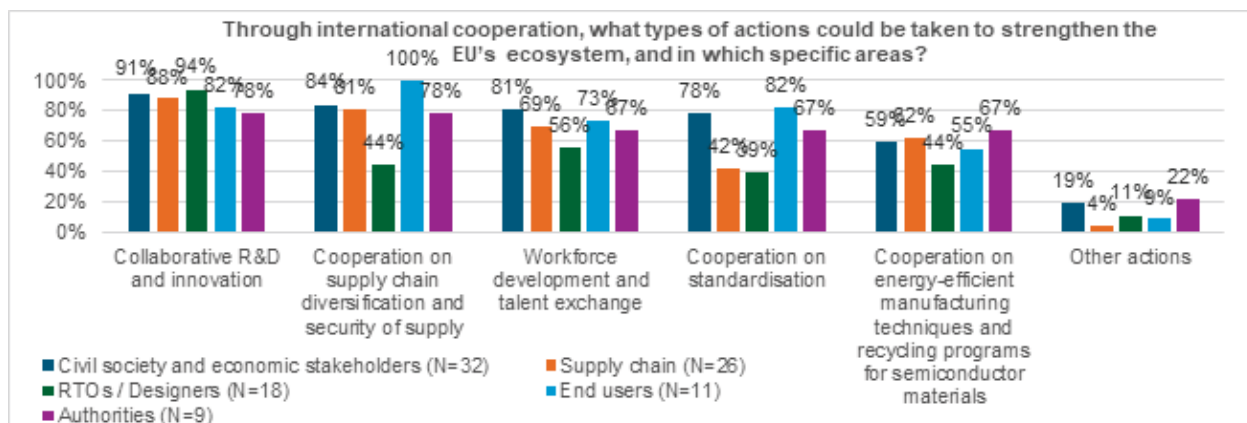


Figure 5. International cooperation actions

Source: Consolidated public consultation of the review of the Chips Act, September-November 2025, Question 63.

All end-user industry representatives (8/8) indicated that the **EU should focus on facilitating technology exchange** in its global semiconductor partnerships, with 88% (7/8) highlighting the importance of building strategic alliances with global leaders, while 75% (6/8) saw value in leading research initiatives. All public authorities (9/9) indicated that they engage in bilateral or multilateral cooperation with third countries in the field of semiconductors, covering areas such as R&D, industrial development, and investment. Among education institutions, half (2/4) indicated that the Chips Act incentivised companies to collaborate with European education institutions and align curricula with labour market needs.

4.5. Relevance

Views on framework adequacy were mixed. One quarter of respondents (25%, 23/94) agreed that the current Chips Act framework provides a sufficiently robust approach to address Europe's supply-side vulnerabilities, while almost half (44%, 41/94) disagreed and one-third (32%, 30/94) expressed a neutral view. RTOs/designers showed the strongest support (62%, 10/16), whereas supply-chain respondents were more cautious, with 56% (14/25) disagreeing. Among authorities, none agreed with the statement, with responses split between neutrality (67%, 6/9) and disagreement (33%, 3/9).

Position papers provide further insight into these reservations. A frequently cited concern is that **the Act's scope places too much emphasis on production capacity targets over alignment with European industrial needs**. As ASML emphasises, “A successful approach to the Chips Act review must not only help develop production capabilities but, more fundamentally, it must create the framework conditions for industry to create [...] an end market for more semiconductors ‘made in the EU’.” Respondents also note that the Act focuses predominantly on front-end chip manufacturing while giving insufficient attention to adjacent value chain segments, particularly printed circuit boards, packaging, and back-end processes. Design capabilities emerge as a prominent theme, with stakeholders arguing that the production-centric approach does not sufficiently recognise the role of chip design in European value creation. Position papers also highlight a disconnect between Chips Act priorities and the needs of key European user industries, particularly automotive, aerospace, defence, and industrial sectors, as well as emerging technology domains such as quantum, photonics, and AI chips.

Among supply-chain respondents, **key factors when selecting a location for semiconductor-related facilities relate to funding access, administrative ease, and skill availability**. Speed and ease of access to public funding was rated very important by 88% (15/17), while clarity of administrative processes and predictability of funding were similarly emphasised. The most frequently identified **barriers to developing an EU AI chip value chain** were lack of manufacturing capability (59%, 55/93), lack of investment instruments (57%, 53/93), skilled workforce shortages (55%, 51/93), and low domestic demand from hyperscalers or AI companies (55%, 51/93). Views varied across stakeholder groups.

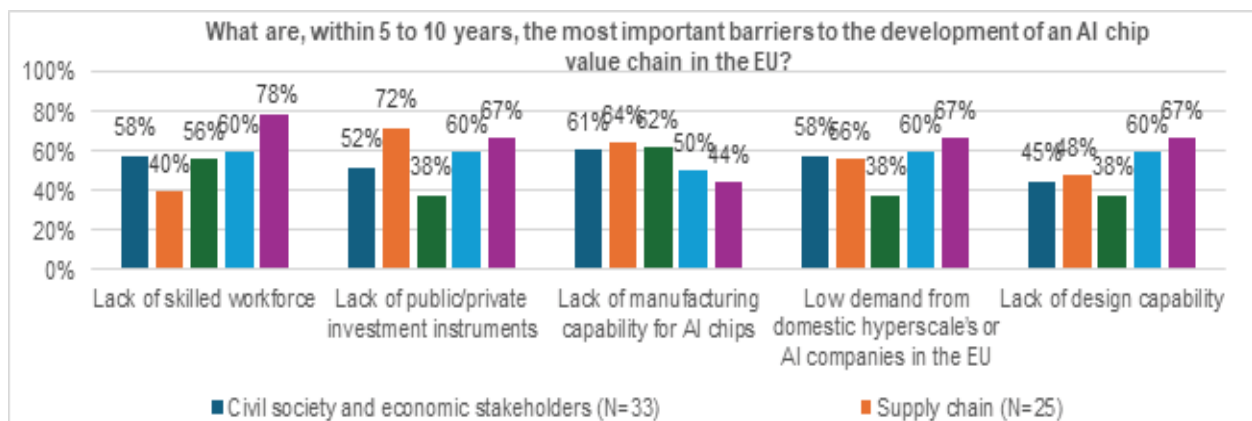


Figure 6. Barriers to AI chip value chain development

Source: Consolidated public consultation of the review of the Chips Act, September-November 2025, Question 42.

Specific obstacles varied by stakeholder type. Fabless companies identified limited access to venture capital and risk finance as the most critical obstacle (78%, 7/9), followed by high cost or limited availability of EDA tools and IP blocks (67%, 6/9). Supply-chain respondents highlighted complex or lengthy permitting procedures and energy costs (each 88%, 15/16). Public authorities unanimously identified access to financing or aid as a key challenge (9/9) to attracting large-scale semiconductor production projects to their region or country, with 78% (7/9) also highlighting skilled labour availability. When asked in open-ended questions what **measures** could mitigate these obstacles, end users emphasised the importance of continuous, proactive Commission dialogue, real-time trade restriction monitoring, early crisis engagement, and complete value chain resilience, extending beyond chip manufacturing. RTOs/designers highlighted EU-level supply observatories with real-time component data and shared strategic reserves for research components. Supply chain stakeholders called for coordinated EU-wide

early-warning systems, harmonised export rules and chips diplomacy with like-minded countries.

Regarding **leadership potential**, respondents most frequently identified semiconductor manufacturing equipment as the segment where the EU has strongest potential to gain or reinforce leadership (79%, 70/89), followed by manufacturing of mainstream chips above 28 nm (62%, 55/89) and packaging, testing, and assembly (61%, 54/89). Fewer respondents (29%, 26/89) saw potential for leadership in advanced chip manufacturing below 10 nm. In terms of **end-user industry prioritisation**, defence/aerospace received strongest support (93%, 83/90), followed by automotive (82%, 75/92), energy (82%, 73/89), and data-centre infrastructure (79%, 73/92).

4.6. Prospective

Respondents expressed strong and consistent support for further Union action across all four action areas. Addressing talent shortages received the highest level of agreement, with 94% of respondents (88 out of 94) agreeing or strongly agreeing that the European semiconductor industry faces serious talent shortages requiring investment in attraction, skilling, reskilling, and training policies; notably, 65% (61 out of 94) strongly agreed, the highest intensity across all statements. The need for EU-level coordination of dispersed national strategies followed closely at 88% (83 out of 94), while lowering barriers for fabless companies and innovative semiconductor firms received 87% agreement. Making Europe a more attractive destination for next-generation chip manufacturing received 84% support (80 out of 95). Across stakeholder groups, there was broad convergence on these priorities, though with variations in intensity (see **Figure 7**).

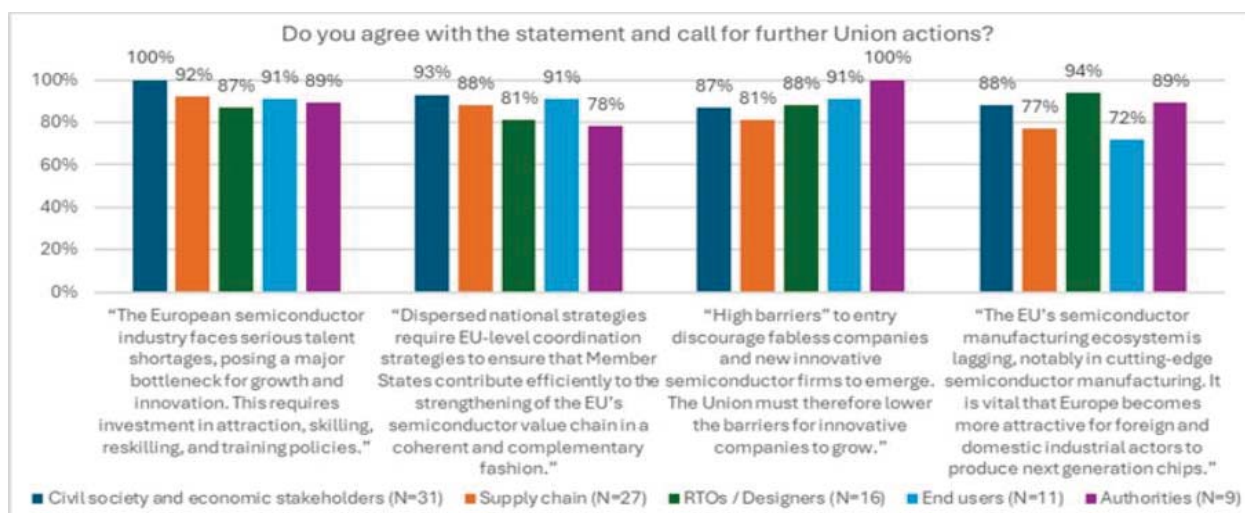


Figure 7. Areas for further Union action (sum of strongly agree + agree)

Source: Consolidated public consultation of the review of the Chips Act, September–November 2025, Question 34.

Position papers provide detailed recommendations for a potential Chips Act 2.0. The core message is that the next phase requires strategic transformation rather than incremental adjustment, moving from a crisis-response instrument to a comprehensive industrial strategy aligned with European demand and competitive positioning.

Design capabilities emerge as one of the most frequently referenced priorities, particularly among supply-chain actors, with proposals for dedicated support to the fabless sector, investment in open-source architectures, and processor development. Stakeholders also call for targeted

support for quantum computing, AI chips, and other emerging technologies. Pilot line expansion and lab-to-fab pathways received particular emphasis from RTOs and user industries, building on the recognised success of Pillar I activities. Stakeholders call for enhanced pilot line infrastructure and clearer pathways from research to industrial production across different technology readiness levels.

Scope expansion beyond front-end chip manufacturing to encompass the full electronics value chain received strong emphasis, particularly from business associations. Respondents underlined the need to widen the FOAK definition under Pillar II to better support the broader semiconductor supply chain and address gaps in PCBs and back-end manufacturing.

Governance and funding reforms feature prominently across stakeholder groups. Proposals include dedicated leadership positions, streamlined procedures through one-stop-shop mechanisms, and strengthened dialogue between policymakers and the European electronics ecosystem. On funding, stakeholders call for structural changes including, consolidated budgets to ensure consistency, dedicated EU budget lines for semiconductors in the next Multiannual Financial Framework and tax incentives to enhance investment attractiveness.

5. SUMMARISED RESULTS OF THE CALL FOR EVIDENCE

The call for evidence was conducted in parallel with the public consultation from **5 September 2025 to 28 November 2025**. Stakeholders were invited to provide open-text responses as well as position papers. In total, **209 responses** were received, including 85 position papers. All inputs were analysed using a hybrid approach combining LLM-driven topic modelling with expert human validation.

The public consultation was answered predominantly by **organisations** (87%, 181/209), with individual citizen respondents comprising 13% (28/209). The largest stakeholder groups were companies/businesses (32%, 66/209), academic/research institutions (26%, 55/209), and business associations (15%, 31/209), followed by NGOs (5%, 10/209), other stakeholders including consumer organisations and trade unions (6%, 12/209), and public authorities (3%, 7/209). Most responding organisations were large enterprises with 250 or more employees (52%, 94/181), though medium (18%, 32/181), small (16%, 29/181), and micro enterprises (14%, 26/181) were also represented.

Geographically, responses came predominantly from **EU Member States** (90%, 188/209), with Germany contributing the highest number (41), followed by France (31), Belgium (21), Spain (19), and Italy (17). Non-EU participation totalled 21 responses, primarily from Switzerland (5), the United Kingdom (5), and the United States (4).

5.1. Effectiveness

Responses and position papers present a nuanced view of the Chips Act's effectiveness. The Act is widely credited with **generating political attention, mobilising substantial investment, and establishing foundational infrastructure**, while stakeholders also identify areas where further progress is needed to achieve intended targets.

On **investment and strategic vulnerabilities**, stakeholders acknowledge substantial investment announcements but question whether current volumes are sufficient to shift Europe's competitive position. Dependence on external suppliers, particularly for advanced nodes, is seen as a continuing area requiring attention. Regarding **specific pillars**, Pillar III monitoring mechanisms

are seen as requiring further development to deliver effective supply chain visibility. For Pillars I and II, stakeholders identify considerations related to technology readiness level coverage and project execution. While Pillar I is credited with tangible achievements, the lab-to-fab transition remains an area for improvement, with respondents calling for stronger mechanisms to translate research excellence into industrial-scale production. Several **cross-cutting enablers** emerge. Respondents stress that infrastructure investments should be matched with sustained human-capital development, with academic institutions underscoring the interdependence between skills, research, and industrial capability. Stakeholders also emphasise that improved accessibility and distribution of support instruments would help maximise the Act's effectiveness, particularly for SMEs and start-ups.

5.2. Efficiency

Responses addressing this criterion primarily focus on **procedural complexity and approval timescales across Chips Act instruments**. Stakeholders across groups identify lengthy approval timelines, administrative burdens, fragmented approaches between EU and national levels, and implementation capacity constraints as areas for improvement.

Approval speed emerges as a prominent concern, with stakeholders noting that European timelines compare unfavourably with other semiconductor-producing regions. These concerns centre particularly on Pillar II instruments, where state aid procedures are seen as lengthy relative to the pace required for timely support, as noted by business associations including DIGITALEUROPE, SEMI Europe, and ESIA. The Important Projects of Common European Interest (IPCEI) mechanism is recognised as important for mobilising large-scale investment, though approval processes are seen as an area for streamlining. **Administrative burden** is closely related. Companies in particular identify multiple sources including complex application procedures and demanding reporting requirements, with smaller companies noting that these pose particular challenges for SMEs and start-ups. For Pillar I, stakeholders call for simpler access mechanisms to the Chips Fund and pilot lines, while for Pillar III, respondents emphasise the need to balance supply chain visibility against reporting burden considerations. **Fragmentation** between EU and national procedures is also identified, with respondents describing parallel processes, inconsistent requirements across Member States, and unclear coordination mechanisms.

5.3. Coherence

Respondents identify coherence as a multi-dimensional criterion spanning internal pillar integration, external policy alignment, and coordination across governance levels – themes that closely mirror those highlighted in the public consultation.

Internally, stakeholders identify scope for stronger alignment between Pillar I innovation activities and Pillar II manufacturing support through dedicated bridging mechanisms to ensure that innovation outputs from pilot lines translate into European manufacturing capabilities. **Externally**, respondents see room for stronger coordination with other EU frameworks such as the AI Act, the Quantum Act, and the Cyber Resilience Act. Stakeholders call for explicit integration between semiconductor policy and broader digital strategies, as well as alignment with defence-industrial policy and economic security frameworks. Coordination across EU, national, and regional governance levels could be strengthened by streamlining funding streams, aligning national approaches, and enhancing central coordination. Reference is made to the European Semiconductor Board as a mechanism to support such alignment. Alignment with **Green Deal objectives** presents both synergies and considerations. Stakeholders recognise

semiconductors as key enablers of the green and digital transitions, viewing the Chips Act as an opportunity to support greater circularity, energy efficiency, and sustainable manufacturing. At the same time, some respondents note that future iterations should address the relationship between environmental and industrial policy objectives.

5.4. EU added value

The key theme across responses is a **strong affirmation that EU-level action delivers benefits unattainable through national efforts alone**. Stakeholders consistently point to scale and critical mass, reduced fragmentation through coordinated action, and shared cross-border infrastructure as core sources of EU added value.

A central element is Europe's ability to **achieve critical mass in investments** that no individual Member State could sustain. Stakeholders emphasise that the semiconductor sector's capital intensity and global competitive dynamics require pooled European resources. Coordination is viewed as equally important, with fragmented national approaches identified as a risk that EU-level action can help mitigate. Stakeholders, particularly academic and research institutions, highlight **shared infrastructure** such as pilot lines and research facilities under Pillar I as concrete examples of EU added value. Distributed manufacturing networks under Pillar III are viewed as requiring EU-level coordination to achieve both economic efficiency and crisis resilience. Citizens and NGOs tend to frame EU added value in terms of **collective resilience and geopolitical positioning**, while public authorities emphasise that EU added value emerges from **connecting regional ecosystems into interregional networks** and leveraging local strengths within a coherent EU framework.

5.5. Relevance

Stakeholders broadly agree that the Act **addresses the overarching challenge of semiconductor resilience and competitiveness but could more closely align solutions with sectoral needs**. Respondents highlight broader questions about whether the Act should shift from self-sufficiency toward indispensability, aligning policy more closely with demand-driven priorities.

Across stakeholder categories, respondents identify an **imbalance between support for leading-edge manufacturing and the needs of mature and mainstream nodes** where European industrial demand is concentrated. Academic and research institutions particularly emphasise that this imbalance "risks weakening Europe's competitive position in the mainstream segments where it already leads" (European University Institute). Stakeholders also identify **value-chain segments** that could benefit from greater attention, including advanced packaging and assembly, printed circuit boards, upstream materials and chemicals, and design capabilities. These observations intersect with Pillar II and the definition of FOAK facilities, with business associations calling for broader FOAK eligibility. Design emerges as the most frequently mentioned area, with stakeholders noting that the current manufacturing emphasis could be complemented by strengthened support for Europe's design ecosystem. Respondents further highlight the **importance of balanced support distribution across stakeholder types**, particularly in addressing barriers faced by SMEs, start-ups, and research institutions.

5.6. Prospective

Respondents provided comprehensive recommendations for a potential Chips Act 2.0, closely linked to the areas for improvement identified under the evaluation criteria and broadly aligned

with themes emerging from the public consultation. A cross-cutting message is the need **for sustained, long-term strategic commitment to achieve European semiconductor objectives.**

On **funding**, stakeholders call for a dedicated EU semiconductor budget at substantially increased scale. Closely related is the recommendation to **expand value-chain scope** beyond front-end manufacturing to include packaging, materials, equipment, and back-end processes, accompanied by a revision of FOAK criteria to reflect this broader definition. **Strengthening European design capabilities** emerges as a key priority, with recommendations focusing on architecture sovereignty, open design platforms, and improved access to design tools and infrastructure. Regarding **implementation**, stakeholders advocate for enhanced pilot lines more closely aligned with industrial scaling requirements, alongside financing mechanisms better suited to SMEs and start-ups. Comprehensive workforce programmes spanning education, training, and talent attraction are emphasised as essential to address skills needs. Strategic international partnerships with trusted partners feature prominently, as does dedicated support for emerging technologies such as quantum, photonics, and AI chips. On **governance**, business associations and public authorities call for strengthened industry-government dialogue and a strengthened European Semiconductor Board to improve strategic coordination.

6. SUMMARISED RESULTS OF THE SURVEY

The survey was administered through Alchemer email campaigns targeting stakeholders identified via desk research and MILD.AI mapping. The initial survey invitation was sent on 24 October 2025, followed by two reminder campaigns: one on November 3rd, a week after initial contact, and a final reminder on 21 November, before survey closure on 24 November 2025. Survey dissemination was further supported by the Austrian Institute of Technology (AIT) and project experts to maximise stakeholder reach across the European semiconductor ecosystem.

The targeted stakeholder survey collected responses from 64 stakeholders. Four tailored questionnaires were designed to capture the specific perspectives of distinct stakeholder groups: national and regional authorities, industry users, supply chain, and research and design organisations. Questions primarily utilised Likert scales (5-point agreement and importance scales) and rating scales, with limited open-ended questions for qualitative feedback. Response options included ‘Don’t know’, ‘Too early to tell’, and ‘Not applicable’ where relevant to ensure data quality and avoid forced responses.

National and Regional Authorities constituted the largest share of respondents (37.5%, 24/64), followed by Research and Design organisations (26.6%, 17/64) and Supply Chain actors (25.0%, 16/64). Industry Users represented the smallest group (10.9%, 7/64).

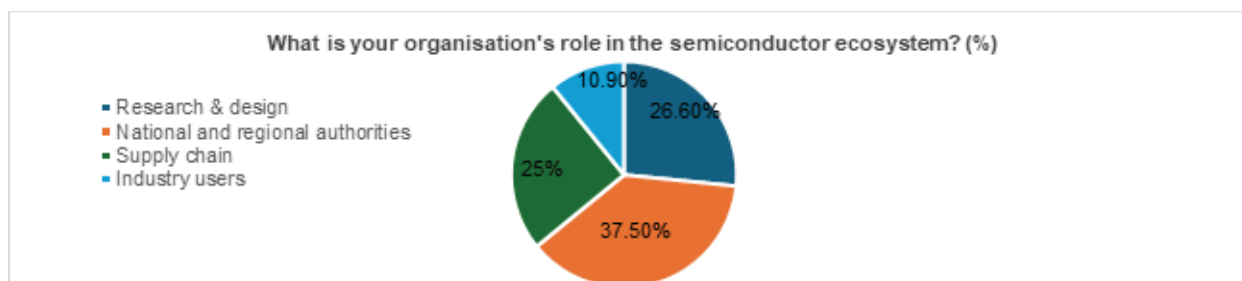


Figure 8. Breakdown of respondent profiles by stakeholder category

Source: Surveys with EU Chips Act stakeholders (research and design organisations N=17, supply chain organisations N=16, industry users N=7, national authorities N=24), conducted by PPMI, October–November 2024).

6.1. Effectiveness

National authorities consistently reported the highest levels of positive effects (75% across most dimensions), which suggests that policy-level coordination benefits are materialising more rapidly than operational effects. RTOs reported the lowest levels of positive effects (35-41%), with 35% reporting ‘no effects’ on several dimensions. This gap warrants further investigation to understand barriers to research organisation engagement.

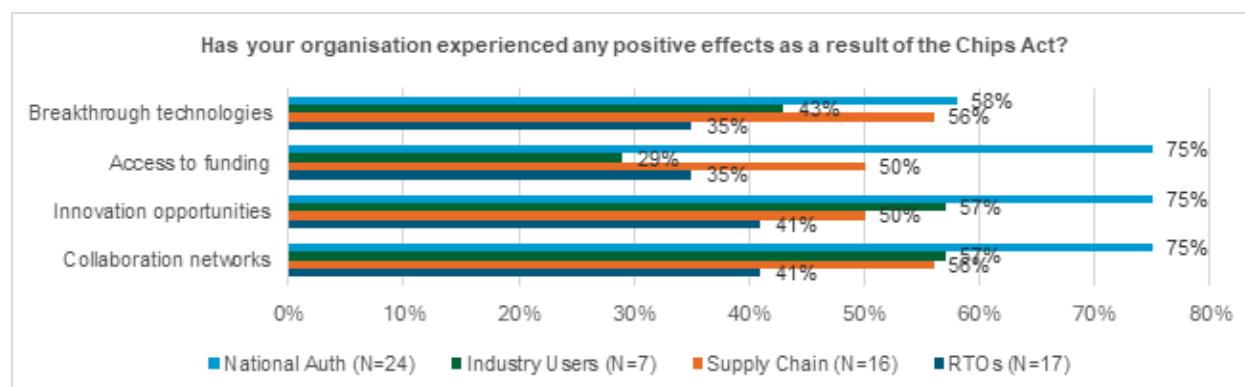


Figure 9. Positive effects experienced (% reporting moderate to very significant effects)

Source: Surveys with EU Chips Act stakeholders (research and design organisations N=17, supply chain organisations N=16, industry users N=7, national authorities N=24), conducted by PPMI, October–November 2024).

Progress assessments varied significantly across the three pillars. Pillar 1 (research-industry link) received the strongest positive assessment, with 58% of National Authorities (14/24) agreeing progress has been made. Pillar 2 (investment and capacity) showed more mixed results (42% agreeing, 10/24), while Pillar 3 (supply chain resilience) received the lowest positive assessment (17% agreeing, 4/24) with 25% (6/24) indicating it was too early to tell. These findings suggest that Pillar 3 mechanisms may require more time to demonstrate observable effects on supply chain resilience.

6.2. Efficiency

National authority responses indicate that **46% (11/24) have encountered significant implementation challenges**, whilst 21% (5/24) reported it was too early to tell and 13% (3/24) indicated no significant challenges. Among those reporting challenges, the most frequently cited were insufficient national co-funding capacity, competing national priorities, and complex EU-national coordination.

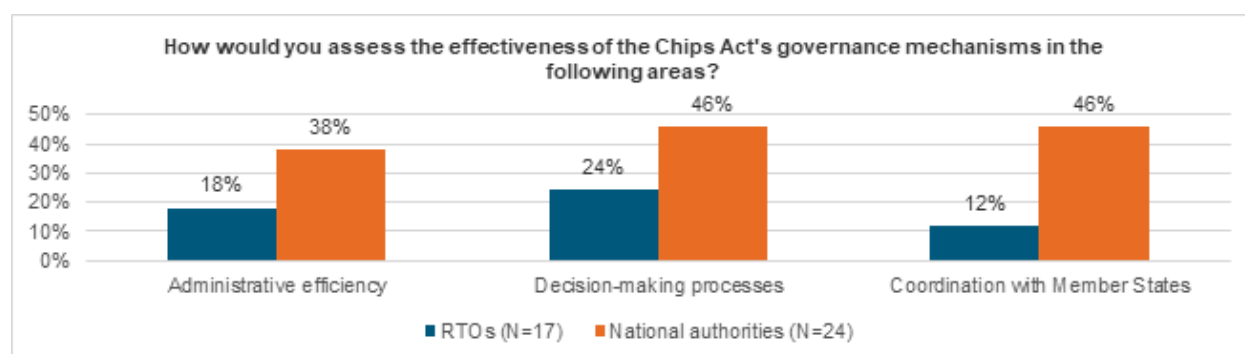


Figure 10. Governance effectiveness assessments (% rating somewhat effective to very effective)

Source: Surveys with EU Chips Act stakeholders (research and design organisations N=17, supply chain organisations N=16, industry users N=7, national authorities N=24), conducted by PPMI, October–November 2024).

A **notable divergence exists between stakeholder groups**: National Authorities assessed governance mechanisms more favourably (38-46% effective) compared to RTOs (12-24%). RTOs showed higher rates of ‘very ineffective’ assessments (18-29%), particularly for administrative efficiency and Member State coordination, which suggests that research organisations face more acute administrative frictions when engaging with Chips Act instruments.

Among RTOs, 47% (8/17) reported facing significant barriers to commercialisation. **Insufficient risk capital and lack of industry partnerships were the most frequently cited barriers**, consistent with the broader concern about the lab-to-fab gap identified in the relevance section.

6.3. Coherence

Regarding external coherence with national strategies, responses from **national authorities indicated mixed alignment**. Of 24 respondents, 33% reported the Chips Act was ‘fully aligned’ with their national semiconductor strategy, 21% ‘somewhat aligned’, and 21% indicated no national strategy exists. **The importance of addressing the misalignment between research priorities and market needs was recognised across all groups**, though with varying intensity. Survey respondents, particularly national authorities, further noted that coordination and investment across the EU, national and regional levels was challenging and more fragmented.

6.4. EU added value

Strengthening the EU’s global position received the highest agreement (68%, 28/41), followed by pooling resources for greater scale (66%, 27/41). This suggests that stakeholders recognise the value of collective European action in the globally competitive semiconductor landscape. However, responses were not uniformly positive: 18-29% of RTOs expressed strong disagreement that these benefits were materialising, indicating a cohort of research organisations that have not yet experienced the expected EU-level synergies.

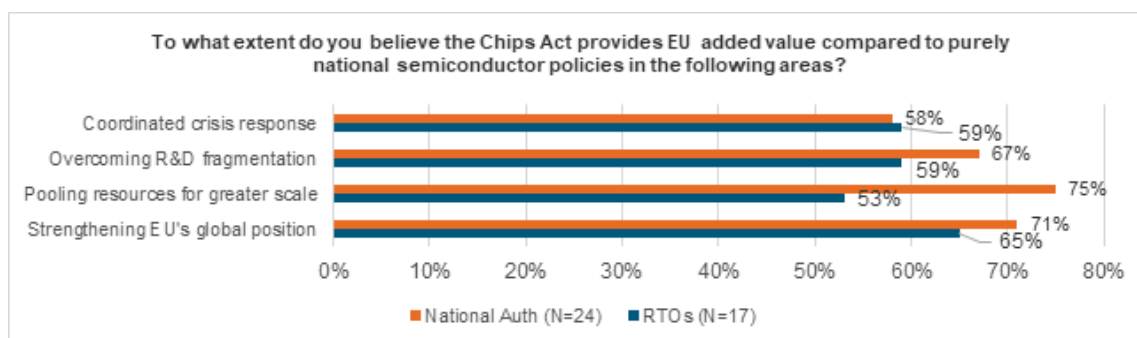


Figure 11. EU added value perceptions (% agreeing or strongly agreeing)

Source: Surveys with EU Chips Act stakeholders (research and design organisations N=17 and national authorities N=24), conducted by PPMI, October–November 2024).

National Authorities consistently assessed EU added value more positively than RTOs, **particularly for pooling resources (75% vs 53%)**. This 22-percentage point gap suggests that the benefits of resource pooling may be more visible at the policy coordination level than at the

research operational level. The relatively similar ratings for coordinated crisis response (59% for RTOs vs 58% for National Authorities) indicate that crisis preparedness benefits are perceived more evenly across stakeholder types.

6.5. Relevance

The survey results demonstrate strong and consistent support for continued EU-level action across all stakeholder groups. Agreement rates on the need for EU-level coordination ranged from 75% (monitoring and crisis response) to 86% (investment and manufacturing capacity), indicating broad endorsement of the subsidiarity rationale underpinning the Act. Supply chain stakeholders demonstrated the strongest support for EU-level coordination in R&D (100%, 16/16) and investment (94%, 15/16), reflecting their direct dependence on ecosystem-wide infrastructure.

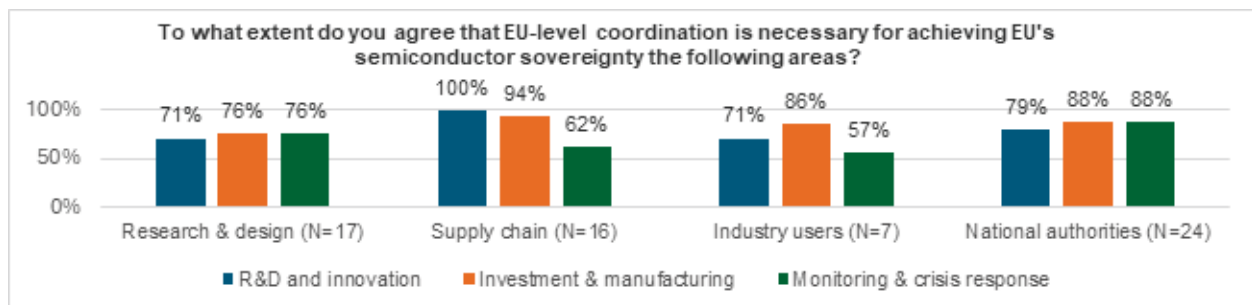


Figure 12. Need for EU-level coordination by policy area (% agreeing or strongly agreeing)

Source: Surveys with EU Chips Act stakeholders (research and design organisations N=17, supply chain organisations N=16, industry users N=7, national authorities N=24), conducted by PPMI, October-November 2024.

However, support for monitoring coordination was comparatively lower among supply chain (62%) and industry users (57%), possibly reflecting concerns about reporting obligations. National authorities showed highest support for monitoring coordination (88%), consistent with their role in crisis response mechanisms and their greater familiarity with Pillar 3 instruments.

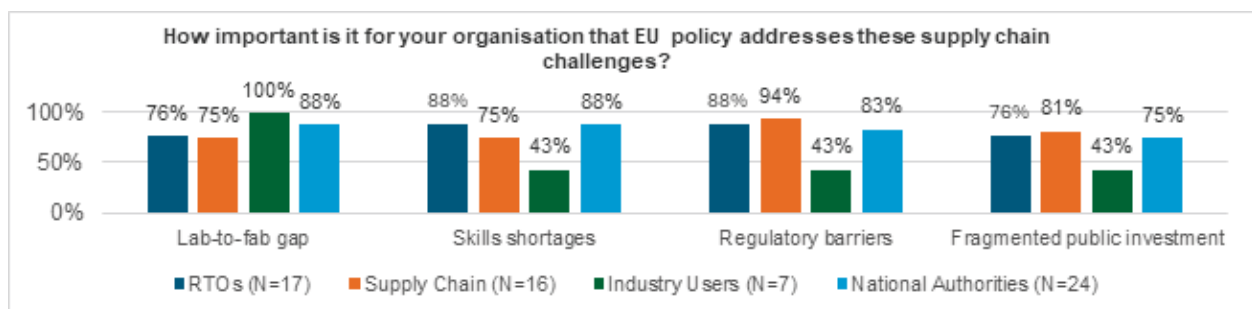


Figure 13. Importance of addressing key challenges (% rating important or very important)

Source: Surveys with EU Chips Act stakeholders (research and design organisations N=17, supply chain organisations N=16, industry users N=7, national authorities N=24), conducted by PPMI, October-November 2024.

Regulatory barriers emerged as the highest-rated challenge overall, with near-unanimous concern from supply chain stakeholders (94%, 15/16). The lab-to-fab gap was unanimously prioritised by industry users (100%, 7/7), whilst RTOs and National Authorities prioritised skills shortages (88% each). These differentiated priorities reflect the varying operational contexts and immediate concerns of each stakeholder group.

6.6. Prospective

Simplified and faster state aid emerged as the top priority (58% ranking first), with particularly strong support from National Authorities (83% ranking first), consistent with their direct experience of notification and approval processes. More direct EU-level funding ranked second (51% ranking first), with strongest support from industry users (80%). Large-scale skills development was also highly prioritised (44% ranking first).

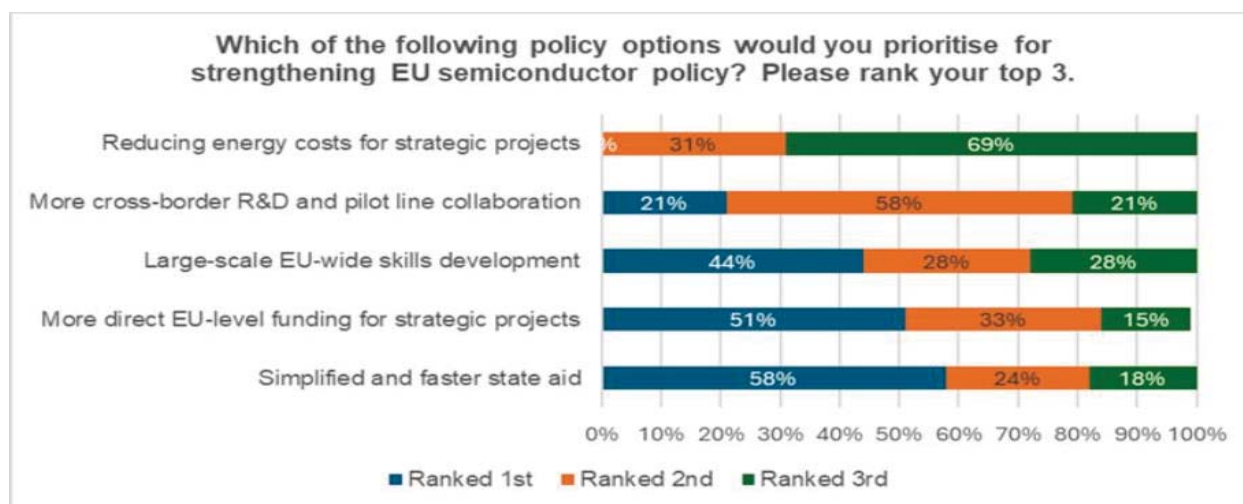


Figure 14. Policy option priorities (% of responses ranking option in top 3)

Source: Surveys with EU Chips Act stakeholders (research and design organisations N=17, supply chain organisations N=16, industry users N=7, national authorities N=24), conducted by PPMI, October–November 2024).

Regarding ambition levels for cutting-edge manufacturing, National Authorities showed diverse views: 29% favoured establishing at least one high-volume leading-edge fab, 21% preferred focusing on pilot lines, 13% supported building multiple leading-edge fabs, and 13% advocated focusing on R&D without new commercial fabs.

7. SUMMARISED RESULTS OF THE EXPERT INTERVIEWS

The interviews were conducted using a semi-structured interview format. The interview guide was developed specifically for this evaluation and was directly aligned with the objectives, pillars, and policy instruments of the Chips Act. This ensured that all discussions systematically addressed themes relevant to the Act while allowing respondents the flexibility to elaborate on issues they considered most significant.

Each interview was fully transcribed and subsequently examined through a structured qualitative analysis process. The analysis focused on identifying recurring themes, points of convergence and divergence, and insights relevant to the evaluation questions. Artificial intelligence tools were used to support the organisation and comparison of the interview material, helping to cluster related content and reveal patterns across stakeholder groups. These AI-assisted steps complemented the manual review of transcripts and improved the consistency and transparency of the analytical process. The material was reviewed iteratively to ensure coherence and completeness.

Respondents represented a broad, strategically selected spectrum of organisations involved in or affected by the European semiconductor ecosystem. The sample included actors from European institutions, industry associations, manufacturing companies, investors, research and innovation

bodies, and supply-chain specialists (**Table 2**). This diversity ensured the inclusion of both supply-side and demand-side viewpoints, as well as short-term operational and long-term strategic considerations. The resulting dataset reflects a balanced mix of technical, economic, policy, and strategic insights relevant to assessing the relevance and implementation of the Chips Act.

Table 2. Interview coding¹

Stakeholder group	Code	Stakeholder group	Code
Public Investor	1	Industry (EMS & PCB)	8
EU Financial Institution	2	Industry Association	9
Private Investor	3	EU Agency / End-User (Space)	10
EU Policymaker (European Commission)	4	Industry (Semiconductor Manufacturer / IDM)	11
Industry Association	5	Policy officer	12
EU Policymaker (European Commission)	6	Trade union	13
EU Implementation Body / Public-Private Partnership	7	Industry Association	14

7.1. Effectiveness

Interviewed stakeholders widely reported that Pillar I instruments had been successful. The EIC’s €300M Chips Fund mandate was described as effective in building a portfolio of deep-tech start-ups and in crowding in private investment by validating risky companies. Stakeholders characterised the Design Platform as a standout success for fabless start-ups, offering easier and cheaper access to design tools. Research-oriented interviewees agreed that Europe remained a global research hub, with IPCEIs and pilot lines supporting innovation along the value chain. First-of-a-kind manufacturing projects and cooperation models such as the TSMC Dresden project (ESMC) were viewed as promising steps towards greater sovereignty and more coordinated European action.

However, perceived **effectiveness dropped sharply at the transition from research to industrialisation and scaling**, creating a pronounced “valley of death” between early-stage innovation and commercialisation. Access to and involvement in pilot lines for start-ups and SMEs was described as unclear and costly and was perceived as a missed opportunity, particularly for equipment and hardware start-ups that needed real testing environments. Stakeholders generally judged Pillar II to be less effective due to weak coordination, the dominance of national budgets (leading to concentration in large Member States), and a lack of clear metrics. They argued that the system mainly supported incremental, rather than disruptive, innovation and that project timelines (3–4 years) were too short for breakthrough technologies that might require seven years or more.

Interviewees identified the investment and market environment as key structural constraints. They claimed that without significantly larger funding, Europe could not expect meaningful independence in advanced CMOS nodes or a competitive position in AI-related hardware. Limited VC and capital markets, the lack of advanced fabs, and the absence of strong European end-users in key sectors such as consumer electronics and AI hardware were said to push start-ups to relocate or raise funds in the US, where both public and private capital moved faster and at much larger scale. While the Chips Act was considered helpful at the seed and early stages, stakeholders argued that it did not yet solve the “valley of death” for follow-on financing.

SME representatives pointed out complex and demanding procedures that made it practically impossible for them to benefit, and some interviewees felt that the Chips Act had not made Europe more attractive for semiconductor start-ups.

Views on supply-chain resilience and governance effects were described as mixed. Interviewees acknowledged that, on paper, the Act had improved sovereignty and triggered new projects, but they also emphasised that Europe still relied heavily on Asian, especially Taiwanese, suppliers and that current investment volumes were viewed as “cosmetic” compared to Asia’s.

Stakeholders involved in Pillar III reported that data collection had shown voluntary mechanisms could work technically, but effectiveness had been undermined because the information gathered was not meaningfully used, which they said damaged trust and future cooperation.

Finally, some stakeholders argued that supply-side support alone was insufficient. In their view, **effectiveness required stronger demand-side measures** (e.g., “buy European” clauses in public procurement for initiatives such as the Pilot Lines, AI Factories, and EuroHPC) to counter the tendency for purchases to come predominantly from US or Japanese suppliers.

7.2. Efficiency

Stakeholders reported that the Chips Act was seen as strategically important but at times operationally challenging. They generally argued that some instruments were not well aligned with the capital intensity and timelines of semiconductors, and that governance across funding streams and administrative levels could be difficult to navigate. Several companies reported duplicated procedures for the same project, which increased costs and slowed decisions, while smaller players often relied on consultants to manage similar application requirements.

Interviewees pointed to the design and sequencing of funding instruments as a key issue. Existing innovation and scale-up tools were described as insufficiently tailored to the cost structure of chip development. **Grants were often too small for major steps such as a tape-out, while the next-tier instruments required higher technological maturity than many firms had reached.** This contributed to a “valley of death” between programmes and, in scale-up support, to difficulties meeting requirements for significant prior investment commitments. Stakeholders argued that more flexible ticket sizes, smoother transitions across technology readiness levels and clearer rules for co-investment with trusted non-EU partners would improve alignment with sector needs.

Procedures were frequently described as slower and more burdensome than in competing regions. Validation and approval for first-of-a-kind investments could take many months, and the gap between political announcements and the first calls was occasionally long. Interviewees also noted repeated documentation requests, digital platforms that did not always function as intended and limited administrative capacity. Stakeholders also highlighted limited transparency on application status, criteria and decision-making, which made planning difficult. They noted the absence of an EU-level overview of firms and investment activity, reducing visibility for effective policy steering. These experiences indicated, in their view, room for simplification, clearer timelines and more consistent once-only submission practices.

Finally, several stakeholders commented that the Act had been assembled under time pressure with limited early industry input, resulting in instruments layered onto administrative systems not fully adapted to semiconductor needs. Decisions to fund many parallel technology areas, such as in quantum, were viewed as spreading resources thinly. Interviewees also noted that for

the most financially robust global semiconductor firms, bottlenecks related less to subsidies than to broader framework conditions such as predictable permitting, skilled labour availability and competitive operating costs.

7.3. Coherence

Stakeholders generally indicated that coherence had been a recurring challenge in the implementation of the Chips Act, both within the EU policy system and across Member States. They noted that internal coherence between innovation funding instruments and top-down policy design had sometimes been limited. Bottom-up work with start-ups was seen as insufficiently connected to the design or adjustment of large-scale instruments. Interviewees reported that operational services collected valuable insights from start-ups, but these were not always fed back into policymaking.

Stakeholders also observed that coherence across instruments and programmes had been uneven. Although synergies in principle existed between frontier research, proof-of-concept funding, transition mechanisms, and later-stage innovation support, interviewees suggested that these links tended to depend on individual initiative rather than structured coordination. **The intended pathway from research to pilot lines and then to production was not widely perceived as an integrated continuum.** The first pillar was viewed as largely research-driven, with limited mechanisms to support the translation of results into industrial innovation or manufacturing scale-up.

Interviewees further noted that coordination across Member States had sometimes been fragmented. **National and regional semiconductor initiatives were often developed independently**, without a clear framework to bring them together into a more strategic European approach. Governance structures intended to facilitate coordination were described as offering limited visibility into other countries' activities, which stakeholders felt could hinder mutual learning and risk duplication. According to several interviewees, parts of the value chain, such as electronic manufacturing services and PCB industries, were receiving comparatively less attention.

Stakeholders also pointed to areas where **legal and policy scope had been unclear** or not fully aligned with other regulatory instruments. Definitions such as what constituted first-of-a-kind were considered difficult to interpret, and some critical segments (e.g., materials suppliers, testing, metrology equipment) were not always clearly addressed. Interviewees also noted potential tensions with other frameworks, including foreign subsidy rules. Environmental and energy-efficiency considerations, prominent in State aid rules, were not seen as strongly integrated into the Chips Act.

Finally, stakeholders described **data collection and monitoring as an area where coherence could be strengthened.** Multiple Commission services, Member States, and private actors carried out parallel semiconductor-related data exercises, sometimes overlapping and targeting the same firms. Interviewees reported a lack of a shared framework or one-stop-shop, which they felt increased administrative burden and reduced transparency. They also saw limited evidence that collected data was systematically pooled or used to support coordinated policy development, noting that effective monitoring, particularly under the third pillar, would require both legal provisions and sufficient institutional capacity.

7.4. EU added value

Stakeholders generally indicated that European funding instruments had played a crucial role for deep-tech start-ups in semiconductors and related fields. Many interviewees believed that companies supported through Union programmes would have struggled to survive on national or private funding alone, especially at very early and capital-intensive stages. European-level public investment, combined with national support, was described as “genuinely additional”, enabling rounds and growth that many Member States could not have achieved independently.

Interviewees noted important signalling and ecosystem effects too. The Chips Act was seen as demonstrating institutional commitment, helping build investor trust and a more visible European semiconductor community. Events and portfolio efforts were viewed as contributing to **“a recognisable European semiconductor ecosystem”** rather than a set of disconnected national efforts.

On regulation and coordination, stakeholders argued that the EU offered value that Member States could not replicate alone. The state aid framework linked to the Chips Act and IPCEI experience was perceived as creating “a common playing field”, giving Europe clearer rules for competing in global subsidy environments, even though most investment came from national budgets.

The joint undertaking structure was viewed as another source of added value through its matching-fund model. Interviewees saw this “money-doubling mechanism” that encouraged national mobilisation. At the same time, they noted that the Act continued to rely heavily on national fiscal capacity, limiting the extent to which EU-level funding could reduce disparities between larger and smaller Member States. Stakeholders also highlighted added value in market intelligence. They reported that only an EU-level effort could generate comprehensive cross-border data on semiconductor use and revenues, which companies valued as a neutral reference point. Yet, they stressed that this advantage depended on such information being visibly used in policy design; otherwise, the case for centralised monitoring weakened.

Interviewees also mentioned several limits. Slow funding roll-out, shaped by the Multiannual Financial Framework and procedural complexity, was perceived as reducing the Act’s competitiveness relative to faster support schemes elsewhere. Stakeholders additionally noted that full semiconductor autonomy was unrealistic. **They saw the EU’s most feasible contribution as reinforcing existing industrial strengths, attracting inward investment, and supporting competitive European firms within global supply chains** rather than pursuing full localisation.

7.5. Relevance

Stakeholders indicated that the European Chips Act addressed several important needs within Europe’s semiconductor ecosystem, though assessments of its overall relevance varied. Many noted that its initial focus did not fully reflect Europe’s structural strengths, long-term vulnerabilities, or the realities of global markets. While the Act provided a framework for investment and technological development, **interviewees stressed the need to refine priorities, strengthen demand-side integration, and better align with industrial capabilities and geopolitical constraints.**

Several stakeholders observed that early instruments overlooked **emerging needs, particularly the strategic roles of fabless design companies**. End-user industries and parts of the supply chain, such as electronic manufacturing services, printed circuit boards, packaging, testing, metrology tools, and raw materials, were not adequately considered, creating uncertainty for investors and leaving European strengths underexploited.

A recurring theme was **the need to focus on areas of competitive advantage**, including lithography and other production equipment, photonics, power electronics, sensors, and imaging technologies. Interviewees suggested that political emphasis on the most advanced manufacturing nodes was unlikely to be realistic without significantly larger budgets. They recommended building on existing ecosystems and concentrating on niches where Europe can lead. Long-term relevance was also linked to AI hardware and related technologies, where innovations risked remaining underutilised without strategies ensuring domestic deployment. Ignoring these areas could leave Europe economically marginalised.

Stakeholders highlighted that monitoring and intelligence functions required clearer design. Effective data collection needed to be tied to specific policy purposes, with aggregated intelligence shared back to contributors to inform assessments and foster long-term cooperation. Interviewees emphasised the importance of integrating industrial policy across the full electronics value chain. Declines in European printed circuit board manufacturing, for instance, were seen as threatening commercial sectors as well as space and defence autonomy, underscoring the need for sustained support to maintain critical suppliers.

7.6. Prospective

Interviewees suggested that the future of **the Chips Act would require a strategic refocus**. Some argued that Europe should concentrate on its real strengths, such as equipment, photonics, sensors, power electronics, and specific AI-related hardware, while providing better support for fabless design and the full electronics value chain. Monitoring and data collection were expected to evolve into a more purposeful intelligence function, with information clearly linked to policy choices, shared with contributors, and used to guide priorities and risk assessments.

Looking ahead, stakeholders called for more flexible and faster funding tools to bridge the “valley of death” from research to industrial scale-up, alongside simpler procedures and clearer access for start-ups and SMEs. They also highlighted the need for smoother pathways across technology readiness levels, and clearer rules for co-investment with trusted non-EU partners. At the same time, they anticipated a stronger EU role in coordinating national initiatives, aligning the Chips Act with other regulatory frameworks, and complementing supply-side subsidies with demand-side measures such as strategic public procurement.

A distinctive perspective emphasised that before pursuing ambitious expansion, Europe should secure existing facilities, as remaining backend capacity faces significant pressure. Recommendations included integrating social conditions (job creation quality, health and safety standards, collective bargaining requirements) and environmental criteria (PFAS substitution, renewable energy incentives) to position Europe as a leader in sustainable semiconductor manufacturing.

Stakeholders emphasised that **Europe should not aim for full semiconductor autonomy but a realistic position**: reinforcing existing strengths, attracting foreign investment, supporting competitive European application companies, and increasing agile EU-level funding to remain relevant in AI chips and advanced computing.

8. SUMMARISED RESULTS OF THE WORKSHOPS

Sixteen thematic evaluation workshops (**Table 3**) were conducted between September and December 2025 with the participation of diverse stakeholders across the European semiconductor ecosystem. Structured summary reports were developed for each of the workshops, including sections 1) Summary of Stakeholders' Perspectives; 2) Key messages per evaluation criteria; and 3) Prospective Reflections for Chips Act 2.0. These summaries have been analysed and compared across the workshops.

Table 3. Workshop coding

Workshop title	Code	Workshop title	Code
Health	1	Automotives	10
Telecoms	2	PCB & EMS	11
RTOs & Academia	3	SMEs & Start-ups	12
ESRA & Regional clusters	4	Industrial Alliance on Processors and Semiconductor Technologies Plenary	13
Technology, Innovation and Skills	5	PAB Workshop	14
Defence & Space	6	PMB Workshop	15
Supply chains	7	Semiconductor equipment and its components	16
Advanced Chips Design for Data Centres	8	Stakeholder's validation workshop	17
Materials	9		

This diverse participation ensured comprehensive coverage of the semiconductor value chain and other stakeholders. They included:

- **Industry representatives:** Major telecoms and industrial equipment manufacturers (Ericsson, Nokia, Philips, Siemens), manufacturer of semiconductors and equipment (ASM, ASML, ST Microelectronics, Cologne Chip), fabless companies, design service providers and other firms (e.g., cloud providers).
- **Regional and institutional actors:** Regional authorities from Saxony, Catalonia, and Finland; industrial clusters (Silicon Europe, MESAP); competence centres; and implementation practitioners managing major projects like Saxony's TSMC facility.
- **Research and academic organisations:** Research Technology Organisations (RTOs) including IMEC, Fraunhofer, CSEM, and CRT/LETI; universities (TU Graz, University of Delft); and academic consortia involved in pilot lines and research projects.
- **Supporting ecosystem:** Organisations dealing with education (European Chips Skills Academy, EIT Digital, aCCcess), material suppliers, manufacturing technology suppliers, investors, and national talent initiatives.
- **European Commission:** Representatives from DG CNECT, DG DEFIS, DG SANTE, DG RTD, and the Joint Research Centre participated to provide policy context and gather feedback.

8.1. Effectiveness

Across the workshops, stakeholders recognised that the Chips Act had **mobilised significant investment and accelerated progress in design, pilot-line development and early manufacturing capacity**, yet they also emphasised that **critical structural gaps persisted** across the value chain. Many noted that Europe still depended heavily on non-EU suppliers, and recent disruptions in the medical, industrial and telecoms sectors illustrated the **ongoing**

vulnerability of supply chains. Participants also warned that component obsolescence, particularly of specialised FPGAs, posed rising risks for sectors requiring long validation cycles.

Stakeholders broadly agreed that **Europe lacked viable high-performance manufacturing options**, especially for AI, HPC and advanced automotive applications. With nearly all cloud-grade chips sourced from Asia, concentration risks remained extremely high. Several workshops highlighted that the absence of a sufficiently large and coordinated European demand base limited incentives for large-scale investment in cutting-edge capacity.

SME access emerged as a consistent concern. While many welcomed the ambition of pilot lines, design platforms and competence centres, stakeholders reported barriers related to cost, administrative complexity, and timing. Pilot-line access was still unaffordable for early-stage innovators, the design platform remained oriented toward firms already active in microelectronics, and in several Member States competence centres had only recently become operational, limiting early benefits for SMEs and start-ups. A lack of effectiveness was also noted by equipment manufacturers who pointed out that their business model would require higher R&D support, not investment incentives.

A cross-cutting theme was the lack of demand aggregation, especially in sectors relying on customised or low-volume chips (health technologies, telecoms, data centres, automotive, PCB/EMS). Participants described this as a fundamental structural weakness: fragmented demand prevented economies of scale and slowed the transition from “lab to fab”, limiting Europe’s ability to industrialise emerging technologies.

Workshops also noted that **skills shortages remained a major bottleneck**, with current initiatives seen as insufficient relative to projected shortages of 70,000-80,000 professionals. Acute gaps were reported in analogue design, system architecture, advanced packaging and testing, profiles essential for scaling many of the technologies supported under the Act.

Finally, **stakeholders stressed that back-end and supporting ecosystem capabilities**, notably packaging, testing, materials, and PCBs/EMS, **remained underdeveloped and insufficiently addressed** by the Chips Act. Several workshops argued that progress in front-end capacity would not translate into ecosystem resilience unless downstream and adjacent segments were strengthened in parallel, particularly for strategic sectors such as defence, automotive and industrial automation.

8.2. Efficiency

Across the workshops, stakeholders emphasised that suggested that while the Chips Act created valuable instruments, **administrative processes were at times perceived as slow, complex, and misaligned with industry timelines**. Participants highlighted long funding cycles, multi-stage application procedures, and lengthy State-aid approvals as recurring sources of inefficiency. Timing mismatches were frequently cited – industry projects often required multi-year lead times, while some public-funding deadlines operated on six-month windows, creating uncertainty and deterring participation. Stakeholders across sectors therefore prioritised reduced administrative burden, clearer guidance, and streamlined multi-instrument processes as key conditions for improving efficiency.

Another broad theme was **fragmentation across parallel EU and national initiatives**. Workshops pointed to multiple programmes operating with limited coordination, leading to duplication, inconsistent cost models, and unclear complementarities. Participants expressed a

preference for a more unified and predictable framework, with several arguing that the Chips Act would function more efficiently if structured as a **single, coordinated programme with clearer interfaces between instruments** rather than a collection of separately governed schemes. Gaps in day-to-day coordination between entities offering similar expertise—such as competence centres, research infrastructures, and national innovation agencies—were also reported as reducing the overall efficiency of investment.

Some workshops raised concerns regarding the **tension between efficiency and geographical cohesion**. While many stakeholders acknowledged that semiconductor manufacturing benefits from concentration in strong industrial clusters, regional authorities emphasised that they played a critical role in training talent, supporting SMEs, and anchoring local innovation ecosystems. Participants noted that overly centralised investment risks overlooking regional capabilities and slowing implementation, underscoring the need for better multilevel coordination rather than simply broader dispersion of funds.

Mobilising **private capital, particularly European venture capital, was repeatedly identified as a structural bottleneck**. Stakeholders argued that despite the availability of public funding, many semiconductor and deep-tech companies faced difficulties raising private investment at scale. Pension-fund rules and conservative investment mandates were frequently mentioned constraints, alongside the limited depth of European VC markets compared to the United States. As a result, participants stressed that the binding constraint for scale-up was often not public-funding volume but insufficient private-capital mobilisation, which reduced Europe's ability to translate R&I outputs into industrial impact.

8.3. Coherence

Workshop discussions suggested that stakeholders saw the main coherence gap in the Chips Act's **imbalance between its strong emphasis on manufacturing capacity and comparatively weaker support for design ecosystems, downstream integration, and demand-creation mechanisms**. Participants across sectors argued that these elements needed to evolve together for the strategy to be coherent, yet this alignment had not fully materialised. Although seen as setting a great foundation, intended synergies across the three pillars were seen as only partially realised, due to fragmented funding streams, misaligned timelines, and weak operational linkage between Pillars I and II, especially in the transition from pilot-line validation to industrial deployment.

A cross-cutting theme from multiple workshops was the scale mismatch between European demand and the investment requirements of semiconductor manufacturing. Even where European technology alternatives existed, participants noted that providers struggled to achieve cost competitiveness because the scale of demand was insufficient. Sectors such as telecommunications, automotive, industrial automation, and medical technologies individually lacked the volume to justify major fabs, and participants across several workshops stressed that scale cannot be reached without coordinated, aggregated demand. This structural constraint was linked to cases where European components were technically available but not adopted widely due to higher cost and fragmented purchasing.

Stakeholders also pointed to regulatory and policy incoherence affecting implementation. Tensions emerged between ambitions for greater use of European technology and EU state-aid and procurement rules that restricted preferential treatment. Materials and equipment suppliers noted path dependencies that made it difficult for European pilot lines to adopt EU-produced chemicals or tools, as certification systems were aligned with non-EU inputs. Emerging

environmental regulations, particularly PFAS restrictions, were also described as misaligned with Europe's manufacturing ambitions, given the absence of economically viable substitutes for certain fabrication processes.

Participants highlighted fragmentation across EU instruments, including Chips JU, Horizon Europe, EIC, IPCEIs, and InvestEU. While individually valuable, these initiatives were perceived as lacking a unifying architecture, creating duplication of administrative effort and insufficiently coordinated investment logic. IPCEIs were viewed as coherent with the Act at a strategic level but still favouring large incumbents, with limited mechanisms to ensure collaboration with smaller innovators. Some challenges were also noted as stemming from **temporal misalignment**. Stakeholders noted that multi-year project cycles and programme start dates were out of sync with industry time-to-market pressures, with initiatives planned for 2026 already perceived as too late for emerging technological windows. Similarly, semiconductor skills pipelines required decade-long investment horizons, yet relevant programmes operated on shorter budgetary cycles, limiting structural impact.

8.4. EU added value

Across the workshops, participants broadly agreed that **EU-level coordination was essential** for achieving outcomes that individual Member States could not deliver alone. Stakeholders highlighted that only the EU could coordinate dispersed national strategies, facilitate cross-border collaboration, and create economies of scale needed for shared infrastructures such as pilot lines, competence centres, and the European Chips Design Platform. If implemented effectively, these platforms were seen as providing globally distinctive EU added value, particularly by enabling SMEs and start-ups to access design tools and advanced prototyping environments that no single country could sustain.

EU-level action was also viewed as necessary for advancing strategic autonomy, not through full self-sufficiency, which participants widely considered unrealistic, but **by reinforcing Europe's strongest technological niches**. Workshops consistently pointed to European advantages in areas such as manufacturing equipment including advanced packaging tools and lithography, to photonics, silicon photonics, power electronics, sensors, and energy-efficient design. Participants emphasised that strengthening these capabilities, combined with targeted international partnerships, could create mutual dependencies where global supply chains rely on European technologies. This was seen as an EU-level task, as no Member State could negotiate such strategic partnerships alone.

Stakeholders also noted EU added value in **coordinating shared investments, particularly through Chips JU and IPCEI mechanisms**. Participants observed that these programmes enabled joint funding and collaboration across borders, giving smaller Member States access to research infrastructures and reducing duplication of national efforts. For many SMEs, universities, and RTOs, the EU framework offered opportunities that national schemes could not provide.

However, workshops also highlighted several areas where EU added value remained largely unrealised. Fragmented decision-making and parallel national initiatives continued to dilute Europe's collective leverage. Participants stressed that while Europe possessed substantial potential demand, the absence of EU mechanisms for demand aggregation prevented this from translating into coordinated procurement or industrial scale. In sectors such as health, telecommunications, and data centres, regulatory fragmentation, such as the lack of a unified

European counterpart to the FDA, pushed innovators to seek approval in the US first, weakening Europe's bargaining position and market cohesion.

Stakeholders also viewed **labour mobility and talent attraction** as a major unrealised opportunity for EU added value. Despite widespread skills shortages, there was no unified European framework for cross-border mobility, qualification recognition, or work permits for international talent. Participants argued that only EU-level action could meaningfully reduce these barriers and support semiconductor workforce development at the scale required.

8.5. Relevance

Across the workshops, **stakeholders broadly agreed that the Chips Act addressed several of the EU's most pressing semiconductor needs**, particularly the scarcity of mature-node manufacturing capacity, the fragmentation of design infrastructure, and the lack of coordinated investment in critical technologies. Participants consistently emphasised that Europe's most strategically important sectors, including automotive, health, defence, space, and telecommunications, continued to rely predominantly on mature and specialised technologies, making the Act's focus on securing and expanding such capacity highly relevant. Defence and space relied on radiation-tolerant 7-12 nm nodes; automotive applications required long-lifecycle components; and healthcare depended on parts requiring multi-decade availability, which standard global semiconductor lifecycles do not support. **Participants therefore viewed the Chips Act as filling a gap that individual Member States could not address alone.**

At the same time, workshops highlighted that several structural needs remained only partially reflected in the Act's design, especially as new vulnerabilities were arising. Many sectors stressed that **relevance depended not only on front-end capacity** but on strengthening packaging, testing, assembly, and PCB/EMS capabilities, which were described as Europe's most acute bottlenecks. Stakeholders across telecoms, automotive, and materials workshops argued that without these back-end and integration capabilities, the Chips Act risked reinforcing Europe's dependence on non-EU suppliers even as wafer-fabrication capacity expanded.

Another recurring theme concerned the **Lab-to-Fab gap, which stakeholders described as not merely an implementation issue but a design-relevance challenge**. Pilot lines were judged valuable for TRL 5-6 development but insufficiently connected to pathways for high-volume manufacturing. Universities and RTOs pointed to wafer-size mismatches, limited access to industrial equipment, and weak technology-transfer channels, all of which limited the relevance of pilot-line investments for early-stage innovation ecosystems.

SMEs repeatedly noted that the Chips Act's architecture was not fully aligned with their needs, despite the central role SMEs play in design, IP development, and manufacturing technology supply. Barriers included cost-prohibitive pilot-line access, consortium structures that favoured incumbents, and an absence of mechanisms to test equipment within industrial fabrication environments. For fabless companies and design start-ups, the Act was seen as insufficiently tailored to address Europe's limited availability of EDA tools, high design costs, and lack of early-stage risk capital – factors that were identified as core relevance gaps.

Workshops also underscored that Europe's design ecosystem and architectural IP capabilities represented a more fundamental sovereignty constraint than manufacturing alone. Stakeholders emphasised that relevance would depend on strengthening software-heavy chip design, system integration, and access to state-of-the-art EDA tools. Telecommunications and data-centre actors, for instance, stressed that controlling architectural design flows and system-

level integration was just as important as building fabs, yet this dimension was underrepresented in the Chips Act's current scope.

Finally, **skills needs emerged as a cross-cutting relevance issue**. Participants across design, R&I, manufacturing, packaging, automotive, telecoms, and materials workshops reported shortages in applied engineering, analogue design, advanced packaging, and system integration skills. Some stakeholders argued the Chips Act's skills measures were insufficiently aligned with where shortages were most acute and did not yet match the pace of technological change in AI, chiplet architectures, and power electronics.

8.6. Prospective

Across the workshops, stakeholders underscored that any future iteration of the Chips Act should move beyond a predominantly supply-driven focus toward a more systemic, integrated, value-chain approach. Participants emphasised the need for a framework that supports not only front-end manufacturing but also design ecosystems, advanced packaging, testing and system integration, which remain essential bottlenecks for Europe's competitiveness.

Stakeholders also pointed to a series of structural reforms. A recurrent theme was the need for dedicated mechanisms for SMEs and fabless companies, including accessible pilot-line pathways, equipment-testing environments, lighter consortium requirements, and dedicated equipment development infrastructure with confidentiality protections, R&D tax credits and TRL 7-9 fast-track funding, and equipment sector representation in governance structures.

Another widely supported proposal was the introduction of demand-aggregation frameworks, enabling coordinated procurement across high-impact sectors such as defence, telecommunications, automotive, health and space. Participants suggested that publicly funded projects could embed demand-side instruments to strengthen the position of European suppliers. They also stressed the need for faster, more flexible funding instruments, streamlined administration, and longer funding horizons aligned with the 10–15 year timescales typical of semiconductor innovation. Predictable, multi-year funding was repeatedly described as critical for enabling companies to plan ahead and scale confidently.

Beyond procedural reforms, workshops identified several new technological and strategic priorities for a next phase of the Act. These included targeted support for advanced manufacturing capabilities, such as sub-2 nm processes and 3D/heterogeneous packaging, to reduce reliance on Taiwan and respond to the rapid rise in AI-driven demand. At the same time, participants stressed that expanding leading-edge capacity should not come at the expense of mature nodes, which remain indispensable for automotive, health, industrial and defence sectors.

To strengthen Europe's long-term sovereignty in design, stakeholders proposed investments in reusable IP libraries, open design clouds, and European EDA tools, arguing that architectural and system-level control is as strategically important as manufacturing. Persistent talent shortages also prompted calls for common European curricula beginning in primary and secondary schools with teacher involvement, mobility schemes, and streamlined international recruitment pathways. Workshop discussions also highlighted the importance of purposeful international partnerships, particularly a more formalised high-level cooperation framework with Taiwan, alongside selective strategic collaborations with Japan, South Korea and other trusted partners in areas where Europe is unlikely to develop full domestic capacity in the near term.

9. COMPARISON OF THE RESULTS OF CONSULTATION ACTIVITIES

The table presents the key results per consultation activity, organised by evaluation criteria, and by the level of consistency, complementarity, and contradiction of the results across consultation activities. Overall, there was a high convergence in the results of different consultation activities, in particular, over the need to align the Chips Act with emerging vulnerabilities, speeding-up and simplifying procedures, and the need to foster SME participation and design activities. Dissent, if any, emerged over the priorities of the Chips Act.

Evaluation criterion	Open public consultation and call for evidence	Survey	Interviews	Workshops	Consistency	Complementarity	Contradiction
Effectiveness	Pillar I received strong positive assessments, with a majority considering pilot lines meet their objectives. Pillar II was viewed positively by three quarters of respondents, who considered it has made the EU a more attractive location for semiconductor manufacturing. However, stakeholders question whether investment volumes are sufficient to shift Europe's competitive position and highlight structural vulnerabilities in PCBs and back-end manufacturing. Pillar III received notably lower only around a third considering objectives met; two-thirds of respondents	National authorities report highest positive effects (75% across most dimensions); RTOs report lowest (35-41%), with 35% reporting "no effects" on several dimensions. Progress varies by pillar: Pillar 1 (research-industry link) strongest at 58%; Pillar 2 (investment/capacity) mixed at 42%; Pillar 3 (supply chain resilience) weakest at only 17%, with 25% of respondents stating it too early to tell.	Pillar I is widely viewed as successful. However, effectiveness is lacking in the commercialisation of knowledge. Pilot line access for start-ups and SMEs is unclear, costly, and a missed opportunity. First-of-a-kind manufacturing projects are promising steps, but overall Pillar II suffers from weak coordination, national budget dominance, and lack of clear metrics. Effects of the Chips Act on supply chain resilience are mixed. The Act has triggered new projects, but Europe still relies heavily on Asian, especially Taiwanese, suppliers, with current investment volumes "cosmetic" compared	Workshop participants confirmed that the Chips Act delivered its main outputs. However, critical gaps remain, and large dependencies persist. Europe lacks production capacities for high-performance chip; early 100% of chips for data centres are manufactured in Taiwan. SME participation in the Chips Act remains weak. The Design Platform came only late and excludes electronics companies wishing to integrate chips; pilot line access remains cost prohibitive. Talent programmes operate at insufficient scale. Vulnerabilities persist in packaging, testing, and commodity components, with	High	High	Low

Evaluation criterion	Open public consultation and call for evidence	Survey	Interviews	Workshops	Consistency	Complementarity	Contradiction
	had not developed monitoring systems or engaged with disruption alerts. A large majority anticipate further supply disruptions, citing geopolitical risks and trade barriers as primary threats. The lab-to-fab gap remains a key barrier, and the 20% market share target is widely seen as unrealistic. SME and start-up accessibility to support instruments requires improvement.		to Asia's. Pillar 3 data collection showed voluntary mechanisms can work technically, but effectiveness was undermined because information was not meaningfully used, damaging trust. Supply-side support alone is insufficient.	PCB and packaging firms remaining outside the Act's scope.			
Efficiency	Experiences with implementation mechanisms varied considerably, with mixed perceptions among fabless companies and most foundries not having applied for facility status. Procedural complexity and slow timelines are dominant concerns; state aid approval delays are characterised as a competitive disadvantage. IPCEI is valued but undermined by	46% of national authorities encountered significant implementation challenges; 21% said too early to tell. Most frequent challenges: insufficient national co-funding capacity, competing national priorities, complex EU-national coordination, and skills/workforce limitations. Notable governance effectiveness gap: national authorities rate relevant	The Chips Act was assembled under time pressure which may explain some of its shortcomings. Stakeholders describe instruments too rigid for semiconductor capital intensity and timelines, fragmented governance across funding streams and administration levels, and procedures that are slow, untransparent, and administratively heavy. Companies face duplicated, overlapping	Processes are too slow (two years between application and funding), and favour very large projects create systematic inefficiencies. Programme coordination between DGs and the EU and national level could be improved, causing duplication and missed synergies. The most critical bottleneck is mobilising European venture capital.	High	High	Low

Evaluation criterion	Open public consultation and call for evidence	Survey	Interviews	Workshops	Consistency	Complementarity	Contradiction
	lengthy processes and less competitive funding rates. Three quarters of respondents support EU-level coordination for strategic project selection, and favour combined funding sources. Administrative burdens pose barriers, in particular for SMEs and start-ups. Fragmentation between EU and national procedures (parallel processes, inconsistent requirements, and unclear coordination) are perceived as impeding delivery.	mechanisms 38-46% effective vs RTOs only 12-24%. RTOs show higher “very ineffective” assessments (18-29%), particularly for administrative efficiency and Member State coordination. 47% of RTOs face commercialisation barriers, with insufficient risk capital and lack of industry partnerships being the most cited elements.	procedures for the same project. Complicated governance forces newer or smaller players to rely on expensive consultants. validation can take ten to twelve months versus roughly half that time or weeks in competitor countries. Time between announcement and first call has been around one year. Documentation must be submitted multiple times, digital platforms do not function as intended, and understaffed bodies are overwhelmed. Limited visibility on application progress, evaluation criteria, and decision-making makes planning difficult. Data collected from industry is perceived as one-way exercise.				

Evaluation criterion	Open public consultation and call for evidence	Survey	Interviews	Workshops	Consistency	Complementarity	Contradiction
Coherence	A large majority reported the Chips Act has contributed to improving governance and coordination between national and regional authorities. However, internal coherence gaps persist between Pillar I innovation and Pillar II manufacturing support, with stakeholders calling for bridging mechanisms. External alignment with adjacent EU frameworks (AI Act, Quantum Act, Cyber Resilience Act, defence policy) requires strengthening. Multi-level coordination across EU, national, and regional governance led through streamlined funding streams. Most respondents reported sustainable practices in place, but tensions exist between environmental regulations and semiconductor manufacturing	Mixed national strategy alignment: only 33% fully aligned with Chips Act, 21% somewhat aligned, 21% reported no national strategy exists. Significant clarity gap between high-level objectives (70% clear) and application procedures (only 31% clear). Industry users reported 0% clarity on application procedure.	Coherence across instruments and programmes could be improved. Potential synergies between frontier research, proof-of-concept funding, and later-stage support function mainly because individual researchers and programme managers push them forward, not through formal coordination mechanisms. The intended continuum from R&D to pilot lines to large-scale production is not perceived as a real, functioning pathway. Another challenge is that coordination across member states is fragmented. National and regional initiatives are developed in isolation with no clear framework for aggregating efforts into strategically coherent European action. Uncertainty around definitions (first-of-a-kind), exclusion or unclear treatment of critical	The fundamental incoherence lies in expanding manufacturing capacity while underinvesting in design ecosystems and back-end manufacturing. A recurring problem is that European alternatives exist but cannot achieve cost-competitiveness due to lack of scale, yet cannot achieve scale without initial demand. “Buy European” procurement clashes with state-aid restrictions; material suppliers report pilot lines using Asian chemicals despite European alternatives; PFAS restrictions conflict with fabrication equipment needs.	High	High	Low

Evaluation criterion	Open public consultation and call for evidence	Survey	Interviews	Workshops	Consistency	Complementarity	Contradiction
	requirements.		segments (materials suppliers, testing, metrology equipment) are obstacles to investment.				
EU added value	Strong consensus that EU-level action delivers benefits unattainable through national efforts alone, particularly scale, critical mass, and reduced fragmentation. Shared infrastructure under Pillar I is cited as a concrete example. The European Semiconductor Board is highlighted as a key coordination platform to prevent subsidy races. Views on extending information mandates were divided, with around half supporting expanded reporting. International cooperation received strong support across all stakeholder groups, with collaborative R&D and supply chain diversification as top	Strengthening EU global position received highest agreement (68%); pooling resources second (66%). National authorities were consistently more positive than RTOs, particularly on resource pooling (75% vs 53%), suggesting benefits were more visible at policy level than research operational level. Crisis response benefits were perceived more evenly across groups (RTOs 59%, National authorities 58%). However, 18-29% of RTOs strongly disagree that EU-level benefits are materialising.	The Chips Act sends a strong message of EU commitment, creating trust among investors and industry. By providing a framework for large-scale investments in semiconductor production and R&D, it fills a role Member States cannot perform and adds momentum by encouraging Member States to mobilise national resources. Only European-level efforts can collect comprehensive market intelligence across sectors and borders. Slow funding roll-out reduces attractiveness compared to more agile schemes in other regions. The state aid framework is seen as too restrictive to allow Europe to participate in global	The EU's distinctive contribution lies in coordinating across member states. The EU level is also relevant because strategic autonomy cannot be achieved at member states level. The EU also provides a collective voice for negotiating strategic partnerships. Shared infrastructure provides valuable access through pilot lines, competence centres, and EU-level consortia, with complementary IPCEI and Chips JU funding. However, the EU's greatest potential remains largely unrealised. Fragmentation undermines competitiveness; absence of mechanisms for aggregated procurement prevents leveraging market	High	High	Low

Evaluation criterion	Open public consultation and call for evidence	Survey	Interviews	Workshops	Consistency	Complementarity	Contradiction
	priorities; all public authorities reported engaging in bilateral or multilateral cooperation with third countries.		subsidy competition more effectively.	size; absence of unified work permit approach creates competitive disadvantages in talent attraction.			
Relevance	Views on framework adequacy were mixed: only one quarter agreed the current framework sufficiently addresses supply-side vulnerabilities, while almost half disagreed. The Act's scope is seen as too narrow, with excessive focus on production capacity over alignment with European industrial needs. Stakeholders identify an imbalance between leading-edge manufacturing support and mature nodes where demand is concentrated. Value-chain gaps in PCBs, packaging, back-end processes, and design s are under-addressed. For location decisions, funding access, administrative simplicity, and skilled	Strong consensus on EU-level coordination: 86% for investment/ manufacturing, 81% for R&D, 75% for monitoring. Supply chain stakeholders were the most supportive (100% for R&D, 94% for investment). Lower support for monitoring among supply chain (62%) and industry users (57%), possibly reflecting concerns about reporting obligations. Lab-to-fab gap emerged as highest priority (83%); unanimous among industry users (100%). Skills shortages (80%), supply chain disruptions (78%), and energy costs (77%) widely Recognised. Regulatory barriers	The Chips Act addresses important needs, but its initial focus did not sufficiently reflect Europe's structural strengths, long-term vulnerabilities, or global semiconductor market realities. Moreover, the Act lacked attention to emerging needs, particularly fabless design companies' strategic roles, and did not adequately consider end-user industries or the broader supply chain, creating uncertainty for investors and leaving European strengths underexploited. A recurring theme in the interviews is the need to focus on Europe's competitive advantages. The political emphasis on competing at the most	The Chips Act is relevant, in particular because of its investments in mature node production and in R&D. Stakeholders emphasised the need to move from chip-centric focus to systemic approach including packaging, testing, and assembly. The Lab-to-Fab Gap persists, with pilot lines reaching TRL6 but lacking pathways to high-volume production. Critical across all sectors.	High	High	Low

Evaluation criterion	Open public consultation and call for evidence	Survey	Interviews	Workshops	Consistency	Complementarity	Contradiction
	workforce availability emerged as most important factors. Semiconductor equipment and mainstream chip manufacturing were identified as strongest areas for EU leadership potential, with defence/aerospace and automotive as priority end-user sectors.	particularly concern supply chain actors (94%). RTOs and National Authorities both prioritised skills shortages (88% each).	advanced manufacturing nodes is unrealistic without far larger budgets.				

ANNEX 3: WHO IS AFFECTED AND HOW?

1. PRACTICAL IMPLICATIONS OF THE INITIATIVE

The proposed initiative would establish a regulatory framework to ensure the functioning of the internal market for semiconductors, secure the competitiveness of the sector, and strengthen the resilience of the semiconductor supply chain across the Union.

The measures concern a few principal stakeholder groups: the semiconductor industry, research organisations and public authorities. On the industry side, the initiative covers a broad cross-section of the semiconductor value chain, including IDMs, fabless companies, design houses, equipment manufacturers, and suppliers, as well as industrial users in sectors such as automotive, telecom, healthcare, energy, industrial robotics, defence, and security. Research organisations refers to the wider research and innovation ecosystem including Research and Technology Organisations (RTOs), academia, and scientific associations. Public authorities encompass national competent authorities in Member States and regions and the European Commission.

Benefits to industry and research organisations

Industry and research organisations stand to benefit from enhanced regulatory predictability through a clarified FoAK framework, accelerated permitting procedures, and the establishment of a Chips Fund 2.0 targeting start-ups and scale-ups. These measures are designed to support capacity expansion by large firms while facilitating technology diffusion from the world of research to SMEs and the broader industry thus bridging the lab-to-fab gap. The introduction of Strategic Projects and targeted demand-side measures would reduce investment risk for advanced facilities, stimulate demand for specialised inputs, and improve access to design and production capabilities. Proposed information-gathering measures would improve supply chain visibility across the value chain.

Furthermore, an example EUR 40 billion investment in Strategic Projects is estimated to generate EUR 6.6–11.5 billion in additional annual revenue for EU semiconductor manufacturers. (see further detail in Annex 4).

Demand-side measures are estimated to generate approximately EUR 0.35–0.46 billion in additional design-related demand for EU fabless firms in the AI Gigafactory context, assuming around 5% capture of the design value envelope, with further dynamic effects through scaling and learning. Innovation procurement (PM9) provides SMEs and start-ups with anchor customers, early revenues, and reference deployments: each euro of public demand is estimated to generate persistent revenue effects of up to EUR 0.5 and to crowd in approximately EUR 0.2 of private investment.

The proposed Business-to-Business Semiconductor Supply Chain Platform (PM5) delivers aggregated supply chain intelligence that would otherwise be prohibitively costly for individual firms to gather independently. Faster permitting (PM3) reduces delay-related capital costs by an estimated EUR 625 million for a representative EUR 20 billion fab.

Beyond direct financial returns, end-users would benefit from enhanced Union-level preparedness, particularly during emergency situations, through improved availability of crisis-prone semiconductors and more robust supply chain coordination mechanisms.

Costs and compliance burdens

Certain measures - particularly those aimed at supporting supply chain resilience - will also give rise to compliance costs. Large firms face one-off onboarding costs for the Platform (PM5) of approximately EUR 100,000 per firm, with recurrent annual costs of EUR 50,000. Across the 483 large firms in the EU semiconductor value chain, this corresponds to approximately a EUR 48 million one-off cost and EUR 24 million per year.

Information requests (PM6) are estimated at up to 10 person-days per firm per request, equivalent to EUR 2,782 per firm and up to EUR 1.34 million sector-wide per crisis request.

Project reporting under PM8 and PM2 runs at 1–2% of project value per year; procurement participation under PM9 at approximately 1.05% of contract value; and certification costs under PM10 are incremental and largely absorbed within existing schemes.

SMEs are fully exempt from reporting obligations, mitigating the risk of disproportionate administrative burdens on smaller actors. Proposed information-gathering measures may nonetheless result in additional obligations for SMEs unless proportionate mitigation mechanisms are applied in practice.

Taken together, the costs associated with these measures are substantially outweighed by the economic benefits brought by improved supply chain resilience.

Impacts on public authorities

For public authorities, Chips Act 2.0 clarifies the scope of permissible public support measures and ensures that the current framework is compatible with the co-financing of Strategic Projects from the Union budget. These changes are designed to foster more complementary and strategically oriented investments across the Union. Member States would also benefit from a strengthened Union-level crisis monitoring and preparedness mechanism, underpinned by a dedicated governance structure to ensure coordination within the single market. National public authorities are, however, expected to incur administrative and adjustment costs associated with assessing applications for support measures.

At EU level, implementation of the preferred option requires a one-off investment of approximately EUR 70 million to develop the Business-to-Business Semiconductor Supply Chain Platform (PM5), alongside staffing of 19 FTEs (additional and redeployment) to administer Strategic Projects, operate the Platform, oversee information requirements, and manage innovation procurement. Here, total annual administrative costs for the Union are approximately EUR 3 686 000².

The proposed framework would, for the first time, allow the EU budget to directly co-fund industrial-scale semiconductor manufacturing, design, and supply chain resilience activities, unlocking a coordinated, cross-border investment pipeline that goes beyond the reach of the current framework.

² Full Time Equivalents (FTEs) were established based on internal Commission analysis. The hourly wage for Member States and businesses was estimated at EUR 29.4 /h. The European Commission costs per FTE are EUR 194 000/year.

Enhanced coordination of public support through Strategic Projects would promote deeper integration across design, manufacturing, and advanced packaging activities. Critically, access to supply chain information outside of a crisis context would allow the Commission to identify specific bottlenecks, dependencies, or disruptions before they reach crisis activation thresholds, thereby shifting focus towards proactive anticipation and mitigation measures. The aforementioned Platform and mandatory information tools (PM5, PM6) would give the Commission an early-warning and crisis-response capability that currently does not exist. At the same time, appropriate safeguards would be applied throughout to ensure strict protection of business-confidential information, proportionality of requests, and full compliance with EU data protection and competition rules.

For Member States, recurrent costs for accelerating permitting (PM3) and validation of mandatory information submissions (PM5, PM6) are moderate and largely absorbable within existing administrative structures.

Impacts on society

Society at large stands to benefit from wider availability of supply of both leading-edge and mainstream semiconductor technologies. Improved Union-level crisis preparedness would benefit consumers and citizens directly, including through better continuity of essential services such as healthcare, energy, communications, and defence during supply disruptions. Reduced reliance on concentrated third-country supply chains lowers the Union's exposure to geopolitical coercion and supply weaponisation. Domestic sourcing criteria under PM10 reduce the risk of embedded vulnerabilities in critical systems. Citizens would also benefit as workers, with the creation of new high-skilled positions and increased labour mobility. Over time, a stronger EU semiconductor ecosystem is expected to contribute to greater product choice, higher quality, and more competitive pricing for all downstream users of semiconductor-enabled goods. No direct costs to citizens are anticipated.

Methodology

The assessment of impacts draws on multiple data sources, including the targeted stakeholder consultation, comprising interviews and surveys, the open public consultation, the Call for Evidence, and desk research. Where possible, impacts have been quantified on the basis of available assessments or modelling. Where dedicated modelling was not feasible due to data or tooling constraints, a qualitative assessment was carried out drawing on existing studies and stakeholder input. Further details on the methodological approach, including detailed tables and estimates, are provided in Annex 4.

2. SUMMARY OF COSTS AND BENEFITS

I. Overview of Benefits (total for all provisions) – Preferred Option		
Description	Amount	Comments
Direct benefits		
Structural expansion and rebalancing of the EU semiconductor industrial base	Qualitative and quantitative; high strategic significance EUR 6.6-11.5 billion additional annual manufacturing revenue; up to EUR 7-9 billion potential design revenues	Assuming EUR 15 billion in public support, PO2 increases EU semiconductor manufacturing capacity through Strategic Projects, generating an estimated EUR 6.6–11.5 billion in additional annual revenue depending on the technology mix. Furthermore, capacity expansion is estimated at approximately 108,000 to 222,000 wafers per

		month. In addition, expanded manufacturing capacity generates recurring fiscal returns for Member States. Applying a value-added ratio of 34% and an average fiscal capture rate of 16.5%, annual direct tax revenues are estimated at EUR 380-662 million once full operational capacity is reached. In parallel, demand-side measures such as innovation procurement may in the short-term generate approximately EUR 0.35–0.46 billion in additional design-related demand for EU-based fabless semiconductor firms, with further indirect benefits through learning effects, scaling and improved investment conditions. <i>Main beneficiaries: EU industry (fabless firms, foundries, end using industry), Member States.</i>
Enhanced investment viability and capital efficiency for large-scale semiconductor projects	Quantitative and qualitative; high significance Indicative avoided delay costs of ~EUR 600–650 million per EUR 20 billion fab	Under PO2, EU co-funding, alignment of FoaK/IPF/OEF procedures, fast-track permitting and demand-side measures jointly improve the bankability of large-scale semiconductor projects. EU co-funding lowers the effective cost of capital, and shortens time to break even. Demand-side instruments such as innovation-oriented public procurement increase revenue predictability. Empirical evidence suggests that each euro of public demand can generate persistent revenue effects of up to EUR 0.5 and crowd in approximately EUR 0.2 of additional private investment. Streamlined and faster permitting further reduces delay-related capital costs. Permitting and design phases in the EU are on average around 7.5 months longer than in leading Asian jurisdictions. Assuming that each year of delay increases total project costs by approximately 5%, this corresponds to an additional cost of around 3.1% of total investment, or approximately EUR 625 million for a representative EUR 20 billion advanced fabrication plant. Earlier and more predictable utilisation of new facilities enhances financial viability, particularly for specialised and application-specific production lines. <i>Main beneficiaries: EU Industry (semiconductor investors), Member States, regional authorities.</i>
Enhanced supply chain resilience and crisis preparedness	Qualitative; high economic significance Up to EUR 1.53 trillion in downstream production value exposed in worst-case disruption scenario	PO2 strengthens monitoring, demand stability and crisis coordination through the Business-to-Business Semiconductor Supply Chain Platform. Improved visibility of structural vulnerabilities enables earlier risk detection and coordinated response, reducing the likelihood and duration of supply bottlenecks. In 2023, motor vehicles and transport equipment (EUR 934 billion) and machinery and equipment (EUR 600 billion) together generated over EUR 1.53 trillion in production value. In the absence of coordinated monitoring and mitigation, this output remains exposed to semiconductor

		supply shocks. PO2 safeguards the functioning of the Single Market during crises by supporting the free flow and availability of semiconductors needed by critical supply chains. <i>Main beneficiaries: End user industries, Member States.</i>
Strengthened EU economic security, resilience and crisis management capacity	Qualitative; high strategic and societal significance	By promoting dual semiconductor sourcing from domestic undertakings, PO2 reduces the risk of embedded vulnerabilities, malicious interference and geopolitical coercion in critical systems. This enhances the integrity of defence, telecommunications, healthcare, energy and digital infrastructure. Reduced reliance on externally concentrated supply chains lowers exposure to supply weaponisation and strengthens the EU's strategic autonomy in vital technologies for competitiveness, security and defence. . In severe disruption scenarios, improved semiconductor availability may contribute to protecting public safety and mitigating life-threatening risks. <i>Main beneficiaries: citizens, public authorities, end user industries (e.g. defence and telecom sectors), and EU industry in general.</i>
Strengthened semiconductor EU innovation ecosystem and accelerated industrial deployment	Qualitative; medium-high significance	PO2 enhances R&D and innovation outputs through expanded pilot lines, a strengthened Chips Fund, and R&D components embedded within Strategic Projects. Increased co-location of research and manufacturing improves knowledge transfer, scale-up capacity and innovation intensity across the value chain. Innovation-oriented public procurement further stimulates technological development. Empirical evidence (see Annex 4 Section 6) suggests that firms participating in such procurement experience 10–20 percentage point higher probabilities of product innovation and approximately 6 percentage point higher probabilities of process innovation compared to otherwise similar firms. Shorter and more secure design-to-fabrication cycles within the EU reduce lead times, improve protection of sensitive intellectual property and increase customer trust. This particularly benefits SMEs and start-ups seeking to scale innovative semiconductor solutions. <i>Main beneficiaries: universities, RTOs, EU Industry (SMEs, start-ups, semiconductor firms).</i>
Structural expansion and rebalancing of the EU semiconductor industrial base	Qualitative and quantitative; high strategic significance EUR 6.6–11.5 billion additional annual manufacturing revenue; up to EUR 7–9 billion potential design revenues	PO2 increases EU semiconductor manufacturing capacity through Strategic Projects, generating an estimated EUR 6.6–11.5 billion in additional annual revenue depending on the technology mix. With EUR 15 billion in public support, capacity expansion is estimated at approximately 108,000 to 222,000 wafers per month, in comparison, under the baseline conditions additional capacity of 321,500 wafers

		per month is announced to date (projections till 2030). In addition, expanded manufacturing capacity generates recurring fiscal returns for Member States. Applying a value-added ratio of 34% and an average fiscal capture rate of 16.5%, annual direct tax revenues are estimated at EUR 380–662 million should the aforementioned projects be realised. <i>Main beneficiaries: EU industry (fabless firms, foundries, end using industry), Member States.</i>
Enhanced investment viability and capital efficiency for large-scale semiconductor projects	Quantitative and qualitative; high significance Indicative avoided delay costs of ~EUR 600–650 million per EUR 20 billion fab	Under PO2, EU co-funding, alignment of FOAK/IPF/OEF procedures, fast-track permitting and demand-side measures jointly improve the bankability of large semiconductor projects. EU co-funding lowers the effective cost of capital, stabilises expected utilisation rates and shortens time to break even. Demand-side instruments such as innovation-oriented public procurement increase revenue predictability. Empirical evidence suggests that each euro of public demand can generate persistent revenue effects of up to EUR 0.5 and crowd in approximately EUR 0.2 of additional private investment. Streamlined and faster permitting further reduces delay-related capital costs. Permitting and design phases in the EU are on average around 7.5 months longer than in leading Asian jurisdictions. Assuming that each year of delay increases total project costs by approximately 5%, this corresponds to an additional cost of around 3.1% of total investment, or approximately EUR 625 million for a representative EUR 20 billion advanced fabrication plant. <i>Main beneficiaries: EU Industry (semiconductor investors), Member States, regional authorities.</i>
Indirect benefits		
Job creation across the semiconductor value chain	Around 4,700 to 7,300 direct jobs Approximately 10,000 to 36,500 indirect and induced jobs	Employment grows due to construction, operation of new fabs, supply chain expansion, and design-centred SME activity. Stabilised supply reduces disruption-related job losses in dependent industries Strategic Projects are estimated to create around 4,700 to 7,300 direct jobs, depending on the technology mix ⁽³⁾. Applying conservative employment multipliers consistent with open and globalised value chains, this corresponds to approximately 10,000 to 36,500 indirect and induced jobs. Higher employment outcomes are associated with capacity expansion following the current wafer mix, while leading-edge manufacturing delivers fewer but more capital- and skill-intensive direct jobs. <i>Main beneficiaries: workers, regional labour markets.</i>

⁽³⁾ Assuming public support of EUR 15 billion from the Union and Member States

Broader economic spillovers	Qualitative and quantitative; medium–high significance	Investment in semiconductor capacity generates wider spillovers across the value chain, including for equipment manufacturers, materials suppliers, engineering services and other specialised suppliers. Regional economies benefit from clustering effects, technology diffusion and increased productivity in downstream sectors. Over time, these spillovers contribute to sustained value creation and tax revenues beyond the directly supported projects. <i>Main beneficiaries: Member States, upstream and downstream industries.</i>
Administrative cost savings related to the ‘one in, one out’ approach		
Administrative cost savings due to the Strategic Projects (simplification effects)	Qualitative (administrative efficiency gain)	Semiconductor firms and national authorities benefit from reduced duplication of administrative steps when compared to fragmented national processes under the baseline. Strategic Projects create a coordinated EU-level project pipeline, simplifying interactions and streamlining procedural handling for a select number of projects that qualify as Strategic Projects. <i>Main beneficiaries: EU industry, public authorities.</i>
Administrative cost savings due to faster and more predictable permitting processes	Qualitative (reduced administrative effort)	Firms benefit from fewer iterative exchanges with permitting authorities and clearer procedural timelines. While not removing obligations, PO2 reduces the time and administrative workload associated with managing complex investment dossiers. <i>Main beneficiaries: EU industry, public authorities.</i>
Administrative cost savings due to reduced ad hoc crisis information requests	Qualitative (reduction of repeated, urgent data calls)	Through the Business-to-Business Semiconductor Supply Chain Platform, companies and national authorities face fewer uncoordinated, last-minute requests. The structured, recurrent mechanism replaces fragmented information demands that currently generate high administrative burden. <i>Main beneficiaries: EU industry, public authorities.</i>

II. Overview of costs – Preferred option							
		Citizens/Consumers		Businesses		Administrations	
		One-off	Recurrent	One-off	Recurrent	One-off	Recurrent
Action (a)	Direct adjustment costs	None	None	None	None	Administrative capacity upgrades for accelerated permitting (PM3) - Expected to be largely absorbed within existing structures - Includes: temporary staff reinforcement, digitalisation of permitting procedures, streamlining and planning workflows. Establishment of governance and procedural systems for Strategic Projects (PM8) - Costs related to the development of selection procedures, evaluation criteria, monitoring frameworks, reporting templates etc.. Platform development and initial IT infrastructure (PM5) - EUR 70 million for	EU-level/Member State co-funding for Strategic Projects (PM8) Requires Union and Member States contributions of at least EUR 15 billion to co-fund Strategic Projects of importance to Europe's technological sovereignty, including leading-edge fabs, packaging hubs, design facilities and supply chain resilience investments.

						platform setup and development which includes the development and deployment of the platform and IT infrastructure, security infrastructure and interoperability tools.	
	Direct administrative costs (to the 'one in, one out' approach)	None	None	Technical IT integration with the Business-to-Business Platform (PM5) - Voluntary cost for large companies themselves would be ~€ 100K for the initial year ⁽⁴⁾ Administrative onboarding and integration with the Platform (PM5) Voluntary low-medium cost of circa 3 person-days which are required to establish compliance with new regulatory obligations. Involves account creation,	Mandatory disclosures of supply chain vulnerabilities based on qualitative assessment (PM6) Approximately 10 person-days are required for large firms for reporting ⁽⁵⁾. Which can be translated into EUR 2782, per year ⁽⁶⁾ In the case of anticipated crisis and assuming all companies are requested to submit data the total effort might cost up to EUR 1.34 million per request across the entire value chain in Europe. Annual Platform operational	None	Processing and validating mandatory information submissions (PM5, PM6) - Moderate costs to sustain the capacity of the Commission and national competent authorities to review, classify, and validate firm-level vulnerability data on a continuous basis. Administrative coordination under the Platform (PM5). - Low-medium cost for regular coordination between Member States and the Commission to manage queries, update procedures, and issue formal information

⁽⁴⁾ Estimation from the Supply chain Working Group of the Industrial Alliance on Processors and Semiconductor Technologies

⁽⁵⁾ [Reporting obligations](#)

⁽⁶⁾ Assuming an annual salary of a supply chain analyst of EUR 60k.

				internal procedural setup, and alignment of data formats.	participation costs (PM5) - The cost for the large companies themselves would be ~€ 50K for the yearly operations.⁽⁷⁾ - The cost covers ongoing data sharing; system maintenance; and internal monitoring alignment. Administrative reporting linked to Strategic Projects and FoaK (PM8, PM2) 1–3 FTE/year, corresponding to 1-2% of the project value⁽⁸⁾. Here, cost includes monitoring reports, compliance documentation, EU-level coordination reporting Administrative participation costs under innovation		requests. Administrative reporting and coordination for Strategic Projects (PM8) 12 FTEs at EU level to supervise Strategic Projects which covers administrative (non-fiscal) tasks such as monitoring, reporting, compliance checks, and cross-border coordination linked to Strategic Projects (11). - Total costs: EUR 2 328 000 Increased administrative burden from demand-side instruments (PM9) Medium cost to the EU and other administrations for the administration of innovation procurement, early-stage offtake programmes and Chip Innovation Partnerships requires additional staffing and contracting capacity.

⁽⁷⁾ Estimation from the Supply chain Working Group of the Industrial Alliance on Processors and Semiconductor Technologies

⁽⁸⁾ The administrative burden observed in Horizon Europe projects (typically estimated at 6–10% of project budgets) is used as a reference point; this roughly corresponds to approximately 0.5–1 full-time equivalent (FTE) of administrative effort per project per year. IPCEI reporting and compliance obligations are assumed to require approximately two to three times higher effort than Horizon Europe projects, reflecting additional State aid requirements, dual reporting to national and EU authorities, and longer monitoring periods. This implies an estimated administrative effort in the order of 1–3 FTE per year for a typical IPCEI participant. When scaled to the substantially larger investment volumes of IPCEI projects, this level of effort corresponds to only a small fraction of total project budgets (typically around or below 1–2%). These figures should be interpreted as indicative.

					procurement (PM9) Approx. 1.05% of contract value ⁽⁹⁾, ⁽¹⁰⁾ which includes: bid preparation, compliance documentation.		Operating the Business-to-Business Platform (PM5) - EU-level cost of 6 FTEs for monitoring, analysis and crisis preparedness functions; handling the RFI's; additional IT maintenance and security costs. - Total costs: EUR 1 164 000
	Direct regulatory fees and charges	None	None	None	None	None	None
	Direct enforcement costs	None	None	None	Adaptation of production processes to meet technological and resilience requirements in Strategic Projects (PM8) Costs likely to be negligible as the Strategic Projects' designation is only for projects meeting the criteria at the moment of application. .		Oversight of mandatory information requirements (PM5, PM6). Approximately 2 FTEs for the Commission and Member States to review compliance, validate data, flag inconsistencies.

⁽¹¹⁾In the current Chips JU, 18 FTEs supervise a budget of around EUR 4.175 billion EU funding.

⁽⁹⁾ PwC, London Economics, & Ecorys. (2011). Public procurement in Europe: Cost and effectiveness. European Commission, Directorate-General for Enterprise and Industry.

⁽¹⁰⁾ Rodionova, Y., Balaeva, O., Yakovlev, A., & Esaulov, D. (2018). Public procurement transaction costs: A country-level assessment. Public Sector Studies, 20(4), 66–81.

	Indirect costs	Opportunity cost of public money being directed elsewhere	None	Opportunity cost of capital allocation Firms may decide to redirect investment away from other activities to invest in Strategic Projects.	Increased competition for skilled labour Strategic Projects intensify demand for technicians, engineers, and specialised operators, increasing hiring and wage pressures.	None	Long-term fiscal exposure from Strategic Projects (PM8) - High costs which, despite being classified as investment expenditure, generate significant fiscal pressure. Transitional dual-system administrative burden (PM5, PM6) - Low-medium (and diminishing) cost. Until the Platform and governance system reach maturity, public administrations handle both legacy crisis tools and new mechanisms.

III. Application of the ‘one in, one out’ approach – Preferred option(s)			
[M€]	One-off (annualised total net present value over the relevant period)	Recurrent (nominal values per year)	Total
Industry and enterprises			
New administrative burdens (INs)		Mandatory disclosures of supply chain vulnerabilities. Medium-low cost expected, estimated at up to 10 person-days/year for large firms (benchmarked to costs of reporting) per request. Can be translated into EUR 2783 cost per request ⁽¹²⁾.	The additional administrative costs for businesses likely will not exceed 0.1 FTE.
Removed administrative burdens (OUTs)		Simplification from Strategic Projects - Reduced duplication of administrative steps during initial project preparation. - Clearer EU-level project pipeline reduces time spent identifying relevant authorities and procedures. Faster and more predictable permitting procedures - Fewer iterative exchanges with	

⁽¹²⁾ Assuming an annual salary of a supply chain analyst of EUR 60k.

		permitting authorities. Assuming that delays add around 5% of total project value per year, a 7.5-month delay (about 0.625 years) translates into a cost penalty of approximately 3.1% of project value. In Taiwan, these phases typically take between 6 and 13 months, whereas in the EU they usually require 16 to 18 months ⁽¹³⁾. This implies that permitting and design in the EU are approximately 3 to 10 months longer than in Taiwan. Using midpoint estimates, ⁽¹⁴⁾ the average amounts to roughly 7.5 months additional time. As set out in Annex 3, and the assumption that each year of delay adds around 5 % of total project value ⁽¹⁵⁾, this implies an additional cost equivalent to 3.125 % of overall investment. For a representative EUR 20 billion advanced semiconductor fabrication plant, this corresponds to roughly EUR 625 million in additional expenditure • Smoother administrative handling of investment dossiers throughout project lifecycle. Fewer ad hoc crisis-related information requests • Companies no longer need to respond to urgent, unstructured, duplicative	

⁽¹³⁾ Figure 16 - Average duration of projects for building wafer fabs (Source: Exyte, 2025)

⁽¹⁴⁾ Around 9.5 months for Taiwan and 17 months for the EU

⁽¹⁵⁾ <https://www.csis.org/analysis/streamlining-permitting-process-fab-construction>

		requests from multiple authorities during disruptions. Partial outsourcing of market-intelligence activities	
Net administrative burdens*	One-off cost for onboarding and integration with the Business-to-Business Supply Chain Platform is not offset by any one-off benefits.	Small net administrative burden, as mandatory disclosures are largely offset by simplification gains (permitting, crisis data calls, reduced monitoring needs).	
Adjustment costs**		- Companies no longer need to respond to urgent, unstructured, duplicative requests from multiple authorities during disruptions. - Firms (especially SMEs) rely on aggregated insights from the Business-to-Business Platform, reducing time spent on internal analysis and monitoring tasks.	
Public administrations (European Commission and Member States)			
New administrative burdens (INs)	None	Processing and validating mandatory information submissions. - Moderate cost for national competent authorities who must review, classify, and validate firm-level vulnerability data on a continuous basis. Recurrent administrative coordination under the Platform.. - Low to moderate costs for public	

		authorities due to regular coordination between Member States and the Commission to manage queries, update procedures, and issue formal information requests. Administrative reporting and coordination for Strategic Projects - Moderate costs covering administrative (non-fiscal) tasks such as monitoring, reporting, compliance checks, and cross-border coordination linked to Strategic Projects. Increased administrative burden from demand-side instruments. Moderate cost for the Commission in the administration of innovation procurement, early-stage offtake programmes requires additional staffing and contracting capacity.	
Removed administrative burdens (OUTs)	None	Simplification due to Strategic Projects - Reduced duplication of administrative steps during initial project preparation Reduced ad hoc crisis information requests - Member States receive a steady stream of structured, standardised data and fewer emergency data calls need to be issued to industry. National competent authorities benefit from centralised	Administrations would incur a moderate recurrent cost from processing mandatory information, coordinating the Platform, fulfilling Strategic Project reporting tasks, and administering demand-side instruments.

		information flows, reducing the need to run parallel national reporting channels. The shared EU governance framework lowers duplication across Member States, especially for cross-border projects. Streamlined information exchange among Member States • Centralised Platform removes the need for parallel national reporting channels. • Less duplication in sharing and validating supply chain intelligence across borders. More predictable permitting processes • Clearer permitting pathways reduce back-and-forth between national authorities and firms.	
Net administrative burdens*	None	Moderate net burden, partly offset by structural simplifications.	
Adjustment costs**			
Total administrative burdens***			

(*) *Net administrative burdens = INs – OUTs;*

(**) *Adjustment costs falling under the scope of the OIOO approach are the same as reported in Table 2 above. Non-annualised values;*

(***) *Total administrative burdens = Net administrative burdens for businesses + net administrative burdens for citizens*

3. RELEVANT SUSTAINABLE DEVELOPMENT GOALS

IV. Overview of relevant Sustainable Development Goals – Preferred Option(s)		
Relevant SDG	Expected progress towards the Goal	Comments
SDG 4: Quality education	Chips Act 2.0 will result in an increase in training opportunities for enhancing digital skills, particularly those related to semiconductor technologies, thus contributing to quality education and lifelong learning.	
SDG 8: Decent work and economic growth	Chips Act 2.0 would contribute to the sustainable development goal of decent work and economic growth by ensuring a well-functioning Single Market in times of crisis and therefore mitigate severe economic repercussions through loss of business opportunities and crisis-related redundancies. It is expected that this initiative will result in an increase in employment due to the spurring of additional chip design and manufacturing capacities in the EU and the increase in SMEs and startups thanks to a renewed Chips Fund.	
SDG 9: Industry, innovation and infrastructure	Chips Act 2.0 is expected to increase the number of semiconductor facilities and support the development of next generation semiconductor technologies in Europe.	

ANNEX 4: ANALYTICAL METHODS

1. MODELLING ECONOMIC IMPACTS

1.1. EU semiconductor market size estimation

1.1.1. Establishing a starting point for BAU scenario

This section establishes the baseline for the market size of Europe's semiconductor industry by quantifying the total **revenue generated** by firms headquartered **within the EU27 in 2023**. The analysis draws on the IDC 2030 Semiconductor Market and Global Value Chain Study, which provides harmonised data across the principal value chain segments and global regions. In this section we focus only on devices, for overall value chain analysis refer to the sections below.

The IDC dataset reports industry revenues at market (transaction) prices. Consequently, the figures represent the economic activity of semiconductor firms based in the EU27. Within this device-focused perspective (chip-level), **Europe generated EUR 50.52 billion in semiconductor device revenues in 2023**. This mostly reflects the activity of Europe's major integrated device manufacturers (IDMs), including Infineon, NXP and STMicroelectronics, whose portfolios span automotive, industrial, power and application-specific devices.

To provide further granularity, Table 1 presents the device-level composition of semiconductor revenues in the EU27 in 2023. This breakdown will serve as the basis for modelling differential growth dynamics, as each device type follows a distinct global demand and pricing trajectory.

Table 1. EU27 semiconductor revenue by device category, 2023 (EUR million and % share). *Source: IDC 2030 study reporting.*

Device category	2023 revenue (EUR million)	Share of total EU semiconductor revenue (%) (¹⁶)
Application-specific (ASIC, ASSP, etc.)	14 871	29.4
Micro-components (MCUs, MPUs, DSPs)	12 691	25.1
Discretes, sensors, actuators	12 239	24.2
Analogue	6 441	12.7
Optoelectronics	2 611	5.2
Memory	1 460	2.9
Logic	204	0.4
Total	50 518	100.0

The device-level composition confirms that Europe's semiconductor industry is dominated by mainstream semiconductors, i.e. in the application-specific devices, micro component, and analogue market segments. Together these 3 categories account for nearly 80% of total semiconductor manufacturing revenue in Europe. These areas align closely with Europe's

(¹⁶) Includes revenues generated in production capacity outside the EU by European semiconductor firms.

comparative advantages in automotive, industrial, and power electronics. **Memory and logic represent marginal shares (below 4% combined)**, whereas globally these two market segments represent the bulk of revenue growth in the coming decade, driven by artificial intelligence.

This product structure is critical for later-stage modelling, as different device types exhibit distinct price elasticity, innovation cycles, and capital intensity. For instance:

- Analogue and power devices have stable long-run demand linked to electrification and automotive transition, but lower revenue growth per wafer.
- Micro-components and application-specific devices capture system-level integration gains and drive mid-range revenue growth.
- Logic and memory, while minor in EU output, tend to experience high global price volatility and cyclical dynamics that are more visible in the more mature and commoditised segments, particularly older-generation logic and memory.

1.1.2. Modelling the BAU scenario

The modelling draws primarily on IDC's **2023–2030 forecast series**,⁽¹⁷⁾ which captures verified investment pipelines, corporate announcements, and regional growth expectations. The dataset reflects both global market recovery after the 2022 downturn and strong European capital formation driven by public subsidies and private investment in new fabs and equipment capacity.

According to IDC, **EU27 device revenues are expected to reach EUR 85.073 billion by 2030**, corresponding to a compound annual growth rate (**CAGR**) of **7.7 %** over the period 2023–2030. This IDC forecast forms the baseline from which the post-2030 device projections are developed. This is **below the global CAGR of 8.75% and well below the US CAGR of 10.6%**.

This lagging growth rate is understandable when considering that Europe does not have significant players in AI which is the key driver of growth in the broader industry. ⁽¹⁸⁾ Furthermore, European companies do not benefit from the price-setting capacity of foundries active in the 7nm and below process nodes typical of AI chips. ⁽¹⁹⁾

This AI boom is not volume-driven, unlike past cycles, but price-driven, fuelled by steep increases in average selling prices (ASPs) for AI devices ⁽²⁰⁾. **Industry growth therefore reflects two dynamics**: one driven by AI logic and AI memory inflation, and another covering mature nodes, automotive, and analogue devices which is growing more slowly

Europe's semiconductor industry is largely absent from AI-intensive segments. Its industrial base is concentrated in analogue, power, microcontroller, and application-specific semiconductors, which are vital for automotive, energy, and industrial systems but do not benefit

⁽¹⁷⁾ IDC, Semiconductors market data by feature size, sector and region, CNECT/2022/MVP/0084 – Second Interim Report

⁽¹⁸⁾ IBS Global Semiconductor Industry Service, May 2025

⁽¹⁹⁾ Future Horizons - The Global Semiconductor Monthly Report December 2025

⁽²⁰⁾ EE Times Europe (2025), "The Recovery Base Is Fragile, Future Horizons' Penn Says", 15 April 2025, available at <https://www.eetimes.eu/the-recovery-base-is-fragile-future-horizons-penn-says/>.

from AI-driven ASP inflation. In fact, the automotive and industrial applications end-market represent 70% of the EU's semiconductor revenues. ⁽²¹⁾

Therefore, the figure by IDC on the EU's growth is in line with the **expectation that Europe's revenue trajectory will lag global averages beyond 2030** for structural reasons i.e. Europe's specialisation lies in mature nodes, notably analogue, power, and automotive semiconductors. These generate lower value added and grow more slowly in value than advanced logic and memory, where both demand and average selling prices are structurally higher. With AI-related products potentially reaching around 70 % of the global market by 2030, this divergence implies that Europe's growth could lag the global average more markedly.

Given these structural conditions, Europe's semiconductor device revenues under the BAU scenario are expected to grow in line with global foundry demand for mature and mid-range technology nodes.

Projections from IBS (International Business Strategies) indicate that, between 2030 and 2035, foundry revenues at technology nodes of 40 nm and above are expected to grow at annual rates ranging from negative 1.5 % to positive 7.5 % growth, depending on the node size, with most mature nodes clustering around at least 5 % (Table 2). This shows a clear divide in market growth for both advanced technology and mature nodes.

Table 2. Global Foundry market growth by technology node. *Source: IBS Analysis of Global Foundry Market, December 2025.*

Node	Growth rate around 2030–2035 (%)
45/40 nm	~6.25 – 6.72
65 nm	~5.46 – 7.54
90 nm	~(1.5) negative growth
130 nm	~5.60 – 5.78
180 nm	~5.29 – 5.59
250 nm	~6.27 – 6.67

Reflecting the EU's current wafer mix, which remains concentrated in these mature nodes and has limited exposure to leading-edge (the AI-driven market segments), **the BAU projection applies an average long-run revenue growth rate of approximately 5% per year for EU27 semiconductor device revenues over 2030–2035.** This rate lies below the global average but is consistent with the projected growth dynamics of the technology nodes most relevant to the European manufacturing base.

Table 3. Assumptions for the revenue growth model. *Source: Compiled by the authors.*

Parameter	Global market	Europe (BAU)	Comment
2030–2035 CAGR	~9 % (including all node sizes) ⁽²²⁾	5%	Adjusted for limited exposure to AI-driven growth and mature

⁽²¹⁾ IDC, Semiconductors market data by feature size, sector and region, CNECT/2022/MVP/0084 – Second Interim Report

⁽²²⁾ IBS, Global Semiconductor Industry Service, Analysis of Foundry Market, December 2025.

			product mix
Growth driver	AI logic, HBM, accelerators	Automotive, power, industrial semiconductors	ASP divergence
Relative global share	Concentration in Asia and US	Stable at 8–9 % ⁽²³⁾	No structural capacity shift expected
Key risks	AI-cycle volatility, trade barriers, CAPEX constraints	Energy prices, project delays, limited AI participation	Structural, not cyclical

Using the IDC 2030 device value of **EUR 85.073 billion**, the following projections are obtained:

- 5% CAGR → $85.1 \times (1.05)^5 \approx 85.1 \times 1.276 \approx \text{EUR } 108.6 \text{ billion}$

Therefore, under the BAU, EU27 device revenues increase from EUR 85.1 billion in 2030 to approximately EUR 108.6 billion in 2035. Furthermore, over the full 2023–2035 period, the EU27 semiconductor device segment is therefore projected to grow from EUR 50.5 billion to around EUR 108.6 billion. This corresponds to a cumulative increase of roughly 115 % and an implied **average annual growth rate of approximately 6.6%**. This shows a deceleration of the European revenue growth, from the period 2025-2030 (7.7%) to the period 2030-2035 (5%), where the importance of AI and leading-edge manufacturing will become more prominent.

1.2. EU Semiconductor manufacturing capacity estimation

1.2.1. Establishing a starting point for BAU scenario

The below estimate reflects **Europe's physical potential to manufacture semiconductor wafers in front-end fabs**, but it does not indicate how much is actually produced, nor the revenue or value chain contributions of other semiconductor segments.

Data anchors

Global installed capacity, 2023: 29.6 million wpm (wafers per month – 200 mm-equivalent).
Source: SEMI World Fab Forecast release of 2 January 2024 ⁽²⁴⁾202 ⁽²⁵⁾. The IDC report also states that all manufacturing currently located in the EU is at mature nodes ($\geq 40 \text{ nm}$) and that no advanced or leading-edge manufacturing is available in the region.

The EU27 share (8.1 %) ⁽²⁶⁾ is applied to SEMI's global installed capacity:

$$29.6 \text{ million wspm} \times 0.081 = 2.40 \text{ million wpm (200 mm-equivalent)}$$

IDC expresses all manufacturing capacity in **300mm-equivalent** units.

Wafer-size normalisation follows surface-area ratios:

⁽²³⁾ Europe's recent revenue share has shown short-term volatility due to downturns in automotive and industrial semiconductors, although its medium-term structural share typically remains within the 10–12 % range.

⁽²⁴⁾ **SEMI (2024).** *Global Semiconductor Capacity Projected to Reach Record-High 30 Million Wafers per Month in 2024*, SEMI Reports. Press release, 2 January 2024. SEMI, Milpitas, CA. Available at: <https://www.semi.org/en/news-media-press-releases/semi-press-releases/global-semiconductor-capacity-projected-to-reach-record-high-30-million-wafers-per-month-in-2024-semi-reports> [Accessed: October 2, 2025].

⁽²⁵⁾ IDC, Semiconductors market data by feature size, sector and region, CNECT/2022/MVP/0084 – Second Interim Report

⁽²⁶⁾ IDC, Semiconductors market data by feature size, sector and region, CNECT/2022/MVP/0084 – Second Interim Report

- Surface area of a 200 mm wafer: $\pi \times 100^2$
- Surface area of a 300 mm wafer: $\pi \times 150^2$
- Surface Ratio: 200 mm / 300 mm wafer = $4/9 \approx 0.444$

Therefore: 2.40 million wspm $\times 0.444 \approx$ **1.07 million wpm (300mm-equivalent)**

1.2.2. Modelling the BAU scenario

The BAU scenario is anchored in a documented 2023 baseline and projected forward on that basis. Capacity projections are drawn from the IDC Semiconductor Fab database, which provides estimates of global and EU27 production capacity expressed in 300mm (12") wafer starts per month equivalents. As the dataset extends only to 2030, projections to 2035, the end of the next MFF, are derived by applying global production trends to the EU context..

Pipeline used in BAU

The construction of the BAU scenario relies on projections from the IDC Semiconductor Fab database. The figures in the table below reflect new projects that have already been announced (see Table 4).

Table 4. Projected new fab capacity resulting from the announced projects. *Source: IDC Semiconductor Fab database.*

Product Type	2023	2024	2025	2026	2027	2028	2029	2030	Total
MEMs								14,000	14,000
Analog/Mixed Signal			6,700		48,000				54,700
Discrete (incl. power)			50,000	20,000	48,000			28,900	146,900
Foundry					9,200				9,200
Logic	35,000			21,700		40,000			96,700
EU27 total	35,000	0	56,700	41,700	105,200	40,000	0	42,900	321,500

Based on announced and already committed semiconductor manufacturing projects in Europe, **the EU's installed wafer fabrication capacity is projected to rise from approximately 1.07 million wafers per month (12-inch, 300 mm equivalent) in 2023 to over 1.39 million by 2030.** This represents an overall increase of about 30%, **corresponding to an average annual growth rate of 3.9%** in capacity. These figures cover only projects that are publicly announced and sufficiently advanced to be included in the business-as-usual (BAU) scenario. They do not take into account potential future investments or investments currently under scrutiny for State aid. The estimate therefore provides a conservative baseline for Europe's manufacturing capacity under existing commitments.

The fastest market expansion is anticipated in leading-edge segments, where EU-headquartered players have limited presence. In this segment, growth in manufacturing capacity is expected to be more limited in Europe than in other world regions. Furthermore, any such increase is likely to serve an IDM model rather than operate as an open foundry.

In line with these findings, this BAU model assumes that all announced and already funded projects determine Europe's capacity growth up to 2030, which is already represented in the IDC

projections data. After 2030, capacity increases are assumed to result from incremental brownfield expansion, tool upgrades, and new projects yet to be announced. To represent this trend, and in line with the manufacturing vs. revenue growth over the period 2023-2030 summarised in the previous paragraph, scenarios of organic growth factors of +2 %, +3 %, and +4 % per year are envisaged from 2031 onwards to the 2030 installed capacity level of 1 391 500 wafers per month (300 mm equivalent), in order to determine the manufacturing capacity by 2035 (Table 5).

Table 5. Projection of Europe’s manufacturing capacity following the organic growth assumption.

Source: prepared by the authors.

Year	Known project path	+2 % p.a.	+3 % p.a.	+4 % p.a.
2031	1,391,500	1,419,330	1,433,245	1,447,160
2032	1,391,500	1,447,717	1,476,242	1,505,046
2033	1,391,500	1,476,671	1,520,530	1,565,248
2034	1,391,500	1,506,204	1,566,146	1,627,858
2035	1,391,500	1,536,328	1,613,130	1,692,973

The projection based on announced and committed projects indicates an installed manufacturing capacity of about 1.39 million wafers per month (300 mm equivalent) by 2030, representing an overall increase of approximately 30 % compared with 2023.

When an organic growth factor of +2–4 % per year is applied from 2030 onwards to capture incremental brownfield expansions and future, as yet unannounced, projects, the model yields 2035 capacity range of roughly 1.54–1.69 million wafers per month. This corresponds to an additional 10–22 % increase beyond the level implied by the current investment pipeline.

Hence, given all the above assumptions hold, under the business-as-usual (BAU) scenario, Europe’s installed semiconductor manufacturing capacity is expected to reach at least 1.39 million wafers per month by 2030, and between 1.54 and 1.69 million by 2035.

1.3. EU positioning in the global value chain and EU value chain strength and resilience

The integrated circuit (IC) or chip is, in broad terms, an amalgamation of transistors, which can serve as either an electronically controlled switch or as a signal amplifier to perform a given function. Since the invention of the IC in the 1950s, a central driver of the semiconductor industry is the continuous push to increase the number of transistors that can be integrated onto a single chip, either through the classical approach of transistor miniaturisation or more recently through innovative packaging techniques such as chiplet architectures or three-dimensional integration.

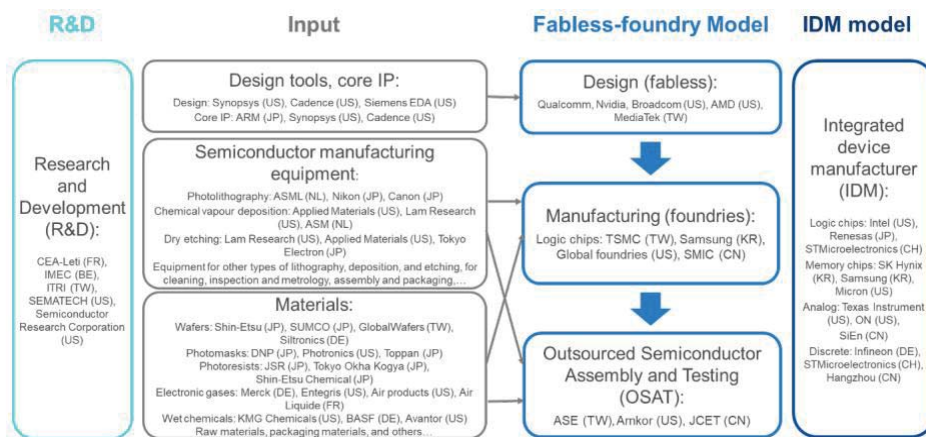
This trend has been made possible by the division of the industry into highly specialised segments along the value chain, ranging from design and equipment manufacturing to fabrication, packaging and testing. No single region controls all stages and firms operate through complex, internationally dispersed networks that maximise expertise, efficiency and scale within complementary but independent production stages. In fact, the semiconductor industry is a direct

result of globalisation, with a chip travelling over 50,000 km and crossing international borders over 70 times before reaching the end-customer ⁽²⁷⁾. While globalisation and interdependence have enabled rapid innovation, they have also created structural vulnerabilities, as disruptions in any segment or geography can ripple across the entire ecosystem.

Figure 14 shows the many stages of semiconductor production, that go from manufacturing equipment, Intellectual Property (IP) to Electronic Design Automation (EDA) tools to raw materials to the design and manufacturing of semiconductors including final assembly, test and packaging.

The EU's position in the semiconductor value chain is strongest in upstream segments, particularly in manufacturing **equipment** and advanced **materials**. In lithography, ASML and its key suppliers, including Zeiss and Trumpf, form a globally indispensable cluster. The Union also hosts major players in back-end equipment such as Besi, EV Group, and SÜSS MicroTec, and is home to leading producers of specialty chemicals including BASF, Merck, and Solvay, alongside substrate manufacturers such as Siltronic and Soitec. The EU's **research** landscape further reinforces these strengths with institutions such as IMEC, CEA-Leti, Fraunhofer, VTT, Tyndall, and SAL contributing to advanced expertise across multiple semiconductor technology domains.

Figure 14 - Semiconductor supply chain and leader companies by segment ⁽²⁸⁾



Source: JRC rearrangement based on the top firms listed in CSET (2021) on 2019 market share data; top manufacturers of wafers and fabless are from Statista¹⁰ 2023; R&D listing is based on reported R&D centres in SIA (2016).

The EU also maintains a solid base of **integrated device manufacturers** (IDMs) that design and fabricate their own chips. Key firms include STMicroelectronics, Infineon, and NXP, followed by Bosch, ams-Osram, and Elmos. Although the EU accounted for around 8% of global wafer-fabrication capacity in 2023, its production is concentrated in relatively **mature nodes** for power electronics, microcontrollers, sensors, and other application-specific chips serving sectors such as automotive, industrial automation, and consumer appliances rather than in **leading-edge nodes**. The latter can be found in applications such as smartphones, high-performance

⁽²⁷⁾ [Chip Production's Ecological Footprint: Mapping Climate and Environmental Impact](#)

⁽²⁸⁾ Cerutti, I. and Nardo, M., Semiconductors in the EU, Publications Office of the European Union, Luxembourg, 2023, doi:10.2760/038299, JRC133850.

computing, AI applications, 5G/6G infrastructure, or data centres. These advanced chips are almost all manufactured in Taiwan (for logic chips) and Korea (memory chips) ⁽²⁹⁾. Since 2025, the US has secured its own leading-edge production capacity ⁽³⁰⁾, with Japan expected to follow soon ⁽³¹⁾. This is primarily because leading-edge chips are concentrated in applications such as smartphones, high-performance computing, and data centres, sectors in which the EU has a relatively limited industrial footprint. Currently, **foundries** fabricating at the leading edge are largely based in Taiwan and South Korea, with the US ramping up its capacity. The EU has limited leading-edge capacity with Intel in Leixlip, Ireland, that is currently reserved for Intel's internal purposes and is not serving as an open foundry.

What remains limited in the EU is a comprehensive **chip design ecosystem** that includes both fabless design firms and large-scale foundries. Fabless companies, which design chips but outsource their manufacturing, generate roughly half of global chip revenues, yet the EU accounts for less than 1% of fabless revenues. The leading **software tools** and **IP** blocks needed to design chips are of US origin. The EU, lacking globally leading fabless “design houses” comparable to the major players in the US and Asia, misses the dense combination of big design firms and open foundries that underpins advanced chips leadership elsewhere.

As a result, the semiconductor value chain remains highly concentrated across a few global regions, and the EU's role, while critical upstream, depends on external partners for several downstream and high-volume manufacturing stages, including for AI chips. The US and several East Asian economies retain leading positions in chip design and leading-edge digital chip manufacturing, while Taiwan and South Korea account for the majority of global leading-edge wafer fabrication capacity. Japan remains a key supplier of essential materials and precision components. Assembly, packaging, and testing activities are largely concentrated in China and Southeast Asia, where significant high-volume back-end capacity has developed.

OECD (2025) ⁽³²⁾ explains that the semiconductor (chips) value chain can be broadly structured into **three principal stages: design, wafer fabrication, and assembly, testing, and packaging (ATP)**. Each stage relies on specific inputs including wafers, manufacturing equipment, and specialised materials provided by dedicated suppliers, and all are characterised by a strong dependence on **research and development (R&D)** to sustain technological progress and competitiveness. The three stages can be further described as:

- **Chip design** is *skill- and research-intensive*, and increasingly capital-intensive, due to the significant cost of electronic design automation (EDA) tools, intellectual property (IP) blocks, verification environments and prototype testing. The complexity of state-of-the-art designs requires substantial upfront investment and contributes to high barriers to entry.
- **Wafer fabrication** (front-end manufacturing) is *capital-intensive*, requiring advanced equipment, cleanroom facilities, and economies of scale. It is also rooted in decades of accumulated experience and high R&D expenditure, which explains why the sector is

⁽²⁹⁾ https://www.oecd.org/content/dam/oecd/en/publications/reports/2025/12/the-chip-landscape_27ef5d87/02dbd028-en.pdf

⁽³⁰⁾ [TSMC begins producing 4-nanometer chips in Arizona, Raimondo says | Reuters](#)

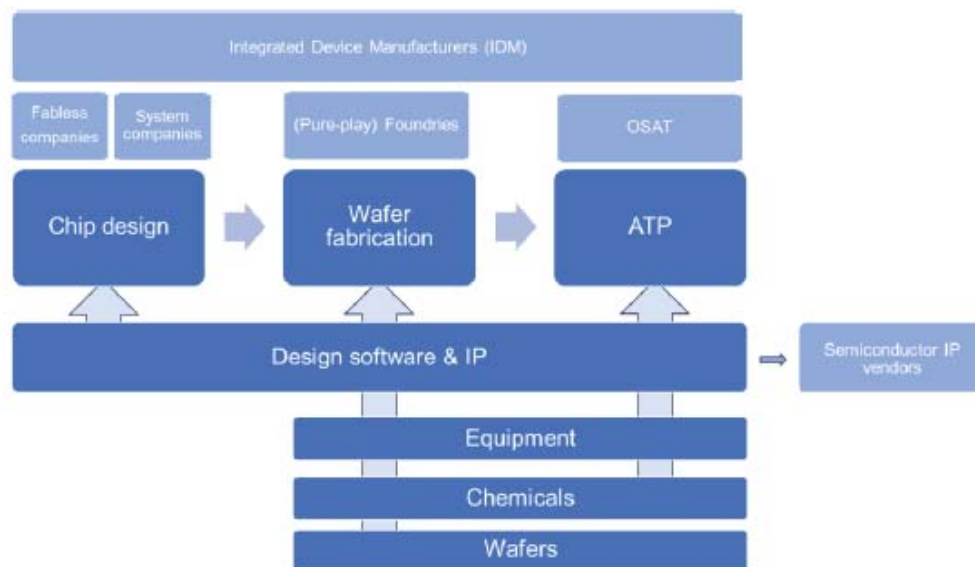
⁽³¹⁾ [Rapidus Achieves Significant Milestone at its State-of-the-Art Foundry with Prototyping of Leading-Edge 2nm GAA Transistors First prototypes successfully demonstrate electrical characteristics as the company continues to hit targets leading up to 2027 mass-production - Rapidus株式会社](#)

⁽³²⁾ OECD. (2025). *Mapping the semiconductor value chain: Working towards identifying dependencies and vulnerabilities* (OECD Science, Technology and Industry Policy Papers No. 182). OECD Publishing.

highly concentrated and why catching up is particularly difficult for late entrants. Sustaining competitiveness at leading-edge process nodes requires continuous innovation, with firms such as Intel illustrating the challenges associated with keeping pace with rapid innovation cycles.

- **Assembly, Test, and Packaging (ATP)** (back-end manufacturing) is *labour-intensive* and less automated, providing lower added value compared to the first two stages. However, advances in heterogeneous integration and 2.5D/3D packaging have turned ATP into an important source of differentiation in performance, energy efficiency and miniaturisation. Moreover, advanced packaging requires close integration between front-end and back-end processes, reinforcing interdependencies across the value chain.

Figure 15. The Illustration of the chips value chain. *Source: OECD, 2025.*



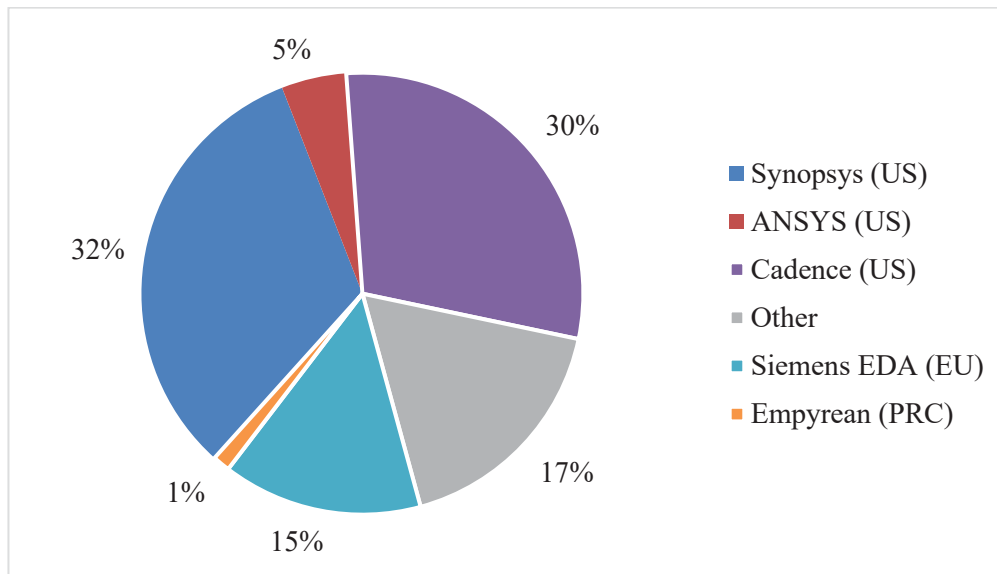
Note: The light blue boxes indicate the different business models.

As illustrated in the figure above, the principal value chain stages are supported by upstream segments such as chemicals and raw materials, wafers and substrates, and semiconductor manufacturing equipment. The produced and packaged chips are then ready for downstream integration and end-use applications.

1.3.1. Detailed analysis of semiconductor value chain

1.3.1.1 Electronic Design Automation

Figure 16. EDA vendors market share 2024 Source: IDC



Electronic Design Automation (EDA) tools are the software tools used to design chips. The EDA Market is dominated by three vendors i.e. Synopsys (US), Cadence (US), and Siemens EDA (EU). Data from 2024 shows that together they hold a market share north of 75%, the acquisition of Ansys by Synopsys in 2025 takes this up to 80%.⁽³³⁾

Design automation software is not delivered as a single application but as an integrated suite of specialised tools that, taken together, constitute the end-to-end “design flow” required to develop an integrated circuit. This flow spans multiple stages and abstraction levels, including (i) front-end design and verification (RTL development, simulation, formal verification, and static checks), (ii) synthesis (translation of RTL into a gate-level netlist under timing, power and area constraints), (iii) physical implementation (floorplanning, placement, clock-tree synthesis, routing, and iterative optimisation), and (iv) sign-off analysis and physical verification (static timing analysis with extracted parasitics across Process, Voltage, Temperature (PVT) corners, signal-integrity analysis, power-integrity and reliability checks such as IR drop and electromigration, and rule-deck-based ‘Design Rule Check’/‘Layout versus Schematic’). The outputs of each stage are used as inputs to subsequent stages; as a result, effective operation depends on consistent constraints, compatible data models, and tight interoperability across tools. In practice, the design process is iterative rather than linear, with repeated loops between implementation and sign-off to resolve violations and converge on manufacturable results.

In practice, as attested by their market share, the three vendors exert total dominance over the Western semiconductor design tool market since the **remaining 20% is primarily** held by Empyrean Technology that is a China based EDA vendor. Empyrean targets Chinese companies

⁽³³⁾ Market share also considers revenues generated from simulation software.

and is still catching up to the big three. Considering its Chinese ownership it also presents clear economic security risks and is not a viable substitute for the three main vendors.

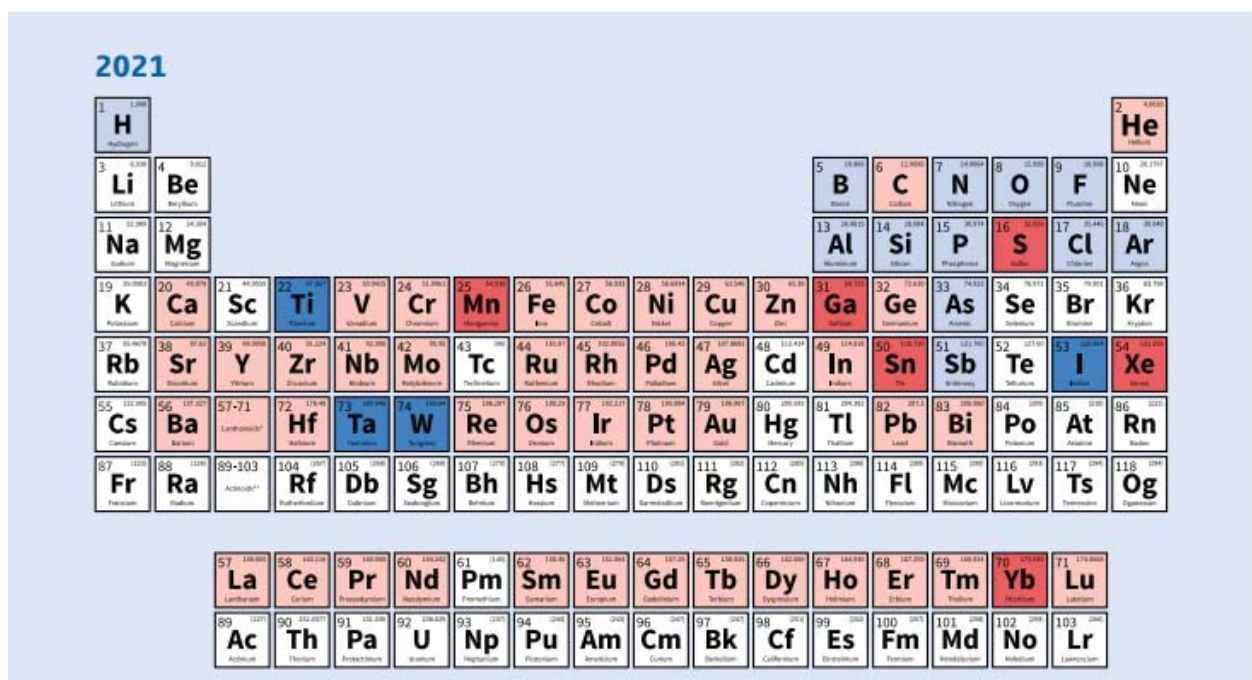
The rest of the market share is **split amongst smaller companies that cannot offer a complete suite of tools** for the development of chips, many of whom aspire to eventually be acquired by one of the big three. Some open-source alternatives are emerging, although these are not suitable for serious commercial chip designs and may only be reliably used for very mature technologies.

1.3.1.2 Materials

1.3.1.2.1 Critical raw materials

The raw materials required for semiconductor manufacturing span almost the entire periodic table and range from silicon, which is relatively abundant, to rare earth elements. According to analysis by ZVEI, over the last thirty years the number of elements used in the semiconductor industry has quadrupled. ⁽³⁴⁾

Figure 17. Elements used in the semiconductor industry, where coloured elements denote use. Source: ZVEI⁽³⁵⁾.



Key examples here include gallium (Ga) and germanium (Ge). These are metals that are not found naturally. They are instead formed, usually as a by-product of the refineries of other metals. Ge is formed as by-product of zinc and Ga is a by-product of processing bauxite and zinc ores.

⁽³⁴⁾ [Semiconductor-Strategy-for-Germany-and-Europe.pdf](#)

⁽³⁵⁾ [Semiconductor-Strategy-for-Germany-and-Europe | ZVEI](#) Light blue indicates elements in use in the 1980s; Dark blue indicates elements in use in the 1990s; Light red indicates elements in use in the 2000s; Dark red indicates elements in use in the 2010s.

35% of the gallium used in the EU is being refined in Germany, however raw gallium originates from China, which holds 94% of the world's production. ⁽³⁶⁾

For **Gallium (Ga)** it is known that about 70% of the material imported to the EU is used to produce integrated circuits, 25% for lighting applications (mostly LED technology) and the rest for photovoltaic technology. In the US the shares of Ga consumption are similar (74% for ICs, the rest for LEDs and specific solar cells). However, increasingly Gallium is also being used in power electronics.

For **Germanium (Ge)** the main producer is China with 79% of world production followed by United States (16%) and United Kingdom (3%). The main uses of Germanium in the EU are infrared optics 52%, optical fibres 23% and satellite solar cells 12%. Ge supply appears to be less of an issue as diversification of sources is simpler compared to Gallium.

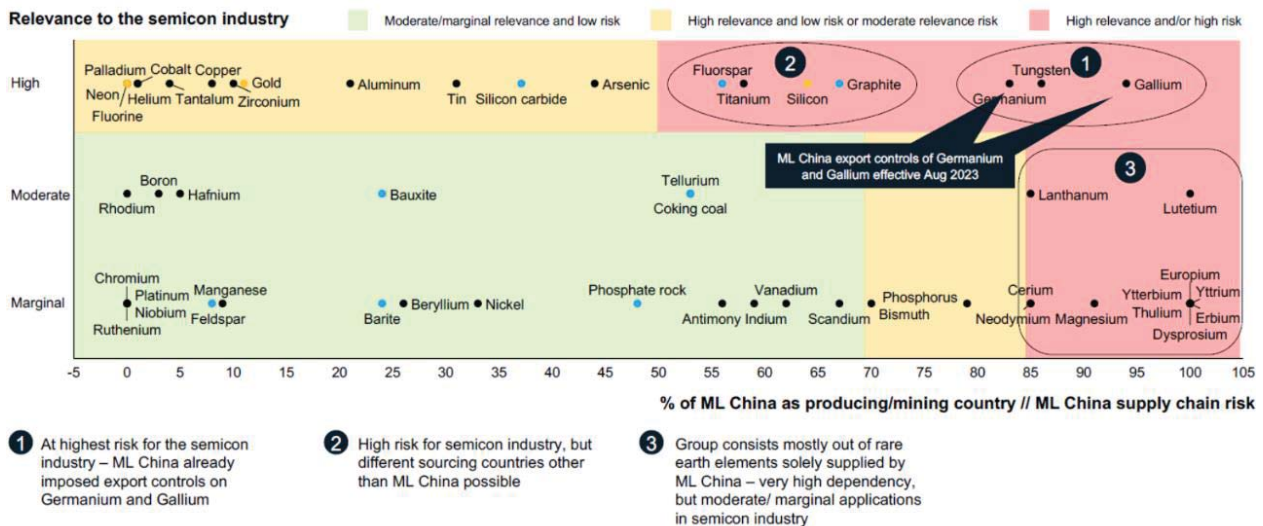
Gallium is used in the industry mainly to make **compound semiconductors**, crucial for RF, power and optoelectronics. Gallium Arsenide (GaAs) and Indium Gallium Arsenide (InGaAs) are some of the most widely used and researched III-V compound semiconductors. For example, **Gallium arsenide (GaAs)** is used for **high-frequency RF chips**, especially power amplifiers and low-noise components in wireless communications. **Gallium nitride (GaN)** is used for **high-power and high-voltage devices**, including power conversion (e.g., chargers, data-centre power supplies) and RF power devices (e.g., telecom infrastructure). Importantly, **GaN** is a potential substitute for **Silicon Carbide (SiC)** in next generation power devices. **Gallium-based optoelectronics** is used in **LEDs and laser diodes**, since these materials emit light efficiently.

Germanium is used in semiconductors mainly in three areas. For example, **SiGe (silicon–germanium) chips** are widely used for **high-frequency analogue/RF** (e.g., telecoms, radar, automotive sensing) since it improves transistor performance. Germanium is also crucial for **silicon photonics** and is used for **on-chip photodetectors** for fibre-optic wavelengths. Additionally, this compound has been used as growth material for transistors contacts since at least the 28nm technology node and as channel material for the 5nm node ⁽³⁷⁾, making it a strategically critical element in leading edge technologies. Europe's Umicore is a large player in both Germanium and Gallium refining and recycling.

⁽³⁶⁾ Cerutti, I., & Nardo, M. (2023). *Semiconductors in the EU: State of play, future trends and vulnerabilities of the semiconductor supply chain* (JRC133850, EUR 31625 EN). Luxembourg: Publications Office of the European Union. <https://doi.org/10.2760/038299>

⁽³⁷⁾ The channel is the “active” part of a transistor and this was the first time a channel was not made in pure Silicon. <https://fuse.wikichip.org/news/3398/tsmc-details-5-nm/>

Figure 18. Critical raw materials in the semiconductor industry. Source: McKinsey



The examples of gallium and germanium are crucial since Chinese dominance over these materials have resulted in the introduction of export controls on gallium and germanium (and related compounds) from 1 August 2023, ⁽³⁸⁾ requiring exporters to obtain licences. The measure is widely understood to be part of ongoing geopolitical rivalries and trade confrontation and is viewed as a response to the tightening of restrictions on China's access to advanced semiconductor manufacturing equipment and know-how, including lithography-related controls. These export controls have resulted in prices for these raw materials to increase by around 20%. ⁽³⁹⁾

1.3.1.2.2 Compound semiconductor Substrates/Epiwafers

The compound semiconductor substrate supply chain is **highly concentrated and regionally segmented**, with leading players clustered in a small number of countries and individual firms specialising by material type.

The Yole Intelligence mapping of leading players worldwide in compound semiconductor substrates highlights that **Europe's visible footprint in substrates is relatively narrow**, with **Freiberger Compound Materials (EU)** identified for **GaAs** and **InP** substrate, both elements crucial for the photonics industry. A larger share of the global supplier base sits in **the United States** (e.g., **Wolfspeed**, **Coherent/II-VI**, **SK siltron CSS**, **AXT**) and **East Asia**, including **Japan** (e.g., **Sumitomo Electric**, **Resonac**, **SiCrystal (ROHM group)**, **JX Nippon Mining & Metals**), **China** (e.g., **SICC**, **Tankeblue**, **Vital**), and **Taiwan** (e.g., **GlobalWafers**, **Hermes-Epitek**). ⁽⁴⁰⁾

However, Europe's exposure in SiC substrates is partially mitigated by the growing vertical integration of certain IDMs. In particular, **STMicroelectronics is building in-house SiC substrate capacity in Catania (Italy)** within its vertically integrated "Silicon Carbide Campus", supported by a **EUR 2 billion Italian state-aid measure approved under the EU Chips Act**

⁽³⁸⁾ Yole, Status of the Compound Semiconductor Industry 2024

⁽³⁹⁾ Yole, Status of the Compound Semiconductor Industry 2024

⁽⁴⁰⁾ Yole, Status of the Compound Semiconductor Industry 2024

framework. In addition, **onsemi is expanding SiC-related capacity at Rožnov (Czechia)**, backed by a **€450 million Czech state-aid measure likewise approved in line with the objectives of the Chips Act.** ⁽⁴¹⁾

Therefore, while Europe does not have significant substrate suppliers, it has significant substrate manufacturing capability as part of vertically integrated IDMs.

The **epiwafer segment** sits immediately downstream of substrates. Here, suppliers take a base **substrate** (e.g., SiC, GaAs, InP, GaN-on-SiC) and grow **epitaxial layers** that determine device performance. This step is a critical dependency point since epitaxy is highly process-sensitive and qualification-heavy, making supplier switching slow and costly.

Based on Yole Intelligence's mapping of leading epiwafer players, the **EU's identifiable merchant epiwafer footprint** includes **Soitec (France)** and **Azur Space (Germany)**, alongside smaller specialised actors (e.g., **Allos** for uLED GaN-related activity). In contrast, a substantial portion of global capability is concentrated outside the EU, particularly in **Japan** (e.g., Sumitomo Electric and other major materials houses), **Taiwan** (a dense epiwafer ecosystem spanning several III–V platforms), **the United States** (e.g. Wolfspeed), and **China** (Enkris Semiconductor, Epiworld), with suppliers covering **SiC**, **GaN** variants (GaN-on-Si, GaN-on-SiC, GaN-on-sapphire), and **GaAs/InP** platforms. ⁽⁴²⁾

1.3.1.3 Ultra-high-purity process gases and chemicals

1.3.1.3.1 Gases

Europe's semiconductor manufacturing ecosystem depends on a broad set of ultra-high-purity process gases and precursors that enable thin-film deposition, patterning (etch), doping, chamber cleaning, and surface/interface treatments, including lithography-support gases used for scanner/track purging and post-lithography resist processing. While several baseline gases remain manufactured within Europe, the EU is structurally dependent on external supply for many of the most critical electronics specialty gases. This dependency is significant because semiconductor production is serial and qualification-bound: the absence of a single qualified molecule at the required purity, packaging, and delivery specification can halt an entire process module and disrupt the operations of a whole fab.

1.3.1.3.1.1 Gases manufactured within Europe and principal functions

European production continues to cover a subset of widely used enabling gases, primarily supporting deposition, etch, and process conditioning. These include ammonia (NH₃) for nitride deposition and nitridation; chlorine (Cl₂) and hydrogen chloride (HCl) for etch, cleaning, and epitaxy process control; nitrous oxide (N₂O) and nitric oxide (NO) for oxide/oxynitride formation and interface engineering; and sulphur hexafluoride (SF₆) for silicon etch (including isotropic and MEMS applications). In addition, certain hydrocarbons (CH₄, C₂H₄, C₃H₈, C₃H₆) are used as carbon sources for specialised films (e.g., hardmasks and carbon-doped layers), while CO and SO₂ may appear in niche plasma or surface-chemistry contexts. Overall, domestic availability exists for several important gases; however, these are often comparatively

⁽⁴¹⁾ [Commission approves €450 million Czech State aid for Onsemi's new semiconductor manufacturing facility](#)

⁽⁴²⁾ Yole, Status of the Compound Semiconductor Industry 2024

standardised and, in many cases, less distinctive for advanced-node capability than gases for dopants, high-value deposition precursors, and critical etch/clean.

1.3.1.3.1.2 Gases predominantly sourced from outside Europe and principal functions

Europe's most material external dependencies are concentrated on molecules that are tightly coupled to transistor formation, materials integration, and equipment availability:

- Dopant gases and diffusion sources: arsine (AsH_3), phosphine (PH_3), diborane (B_2H_6) and related boron chemistries (BBr_3 , BF_3), as well as POCl_3 , underpin formation of n-type and p-type regions and diffusion processes. ⁽⁴³⁾ These inputs are not readily substitutable; alternative sourcing typically requires extensive requalification and may present yield and reliability risk.
- Deposition precursors: silane (SiH_4), ⁽⁴⁴⁾ disilane (Si_2H_6), chlorosilanes (DCS/TCS) and SiCl_4 , tetraethyl orthosilicate (TEOS), trimethylsilane (TMS), germane (GeH_4) and WF_6 enable deposition of key silicon, dielectric, SiGe/Ge, and tungsten films. Disruption can halt deposition modules and create cascading effects on work-in-progress wafers and cycle time.
- Etch and chamber-clean gases: HF (oxide removal), HBr (anisotropic silicon/polysilicon etch), NF_3 (remote plasma cleaning), F_2/ClF_3 (aggressive cleaning/fluorination), and multiple fluorocarbon/PFC/HFC gases (e.g., CF_4 , CHF_3 , C_2F_6 , C_3F_8 , C_4F_8 , C_4F_6 , C_5F_8 , CH_3F , CH_2F_2) are essential for pattern transfer, selectivity/profile control, and maintaining tool uptime.
- Reliability/passivation inputs: deuterium (D_2) supports selected passivation and anneal processes; substitutability constraints may manifest through yield or reliability qualification impacts even where immediate production continues.

Furthermore, when considering the upstream sources of these gases, more than 50% of the Union's electronics speciality gases are heavily dependent on China.

1.3.1.3.1.3 Structural characteristics of the dependency

These dependencies are amplified by: (i) the serial nature of wafer fabrication (a blocked step halts downstream processing); (ii) qualification constraints (purity, impurity profile, packaging, and delivery stability are part of the specification);⁽⁴⁵⁾ and (iii) limited substitutability, particularly for dopants and advanced deposition precursors;

External dependence for dopants, critical deposition precursors, and etch/clean chemistries, combined with qualification-bound production, creates a high risk profile. Even where Europe retains domestic production of several baseline gases, disruption affecting externally sourced molecules on the critical path is likely to result in discontinued outcomes: module stoppages, tool

⁽⁴³⁾ [Chemicals Used in the Electronics Industry | OECD](#)

⁽⁴⁴⁾ [Silane | Air Liquide](#)

⁽⁴⁵⁾ For semiconductor process gases, the applicable specification extends well beyond a nominal purity value (for example, 99.9999%). In practice, device manufacturers and equipment suppliers jointly qualify the gas as an integrated package, encompassing its detailed impurity profile, cylinder and valve materials, packaging configuration, and the performance of the associated delivery hardware. Any change in supplier, production site, or even cylinder type typically necessitates requalification, a process that can require several weeks to months and entails significant engineering effort and test-wafer consumption.

downtime, cycle-time extension, and potential yield degradation, with cascading effects across the European semiconductor value chain and downstream industrial users.

1.3.1.3.2 Chemicals

Semiconductor fabs rely on ultra-high-purity chemicals at every step, including cleaning acids (hydrofluoric acid, hydrochloric acid, sulphuric acid), bases (ammonium hydroxide), oxidisers (hydrogen peroxide), solvents (isopropyl alcohol), etch and deposition chemistries, and Chemical-Mechanical Planarisation (CMP) slurries used to polish wafers between layers. These inputs must meet tight purity specifications and are qualified to specific tools and recipes, therefore shortages or quality issues can halt production and are not quickly solved by switching supplier.

This section will focus on photoresists since these chemicals are a pronounced dependency. This is due to the fact that the supply base for high-end resists is very concentrated and switching costs are higher, with requalification often required and limited near-term alternatives are available once a process is determined. Polysilicon and precursor chemicals will also be considered.

1.3.1.3.2.1 Photoresist

Photoresist is a critical input to semiconductor photolithography. It is the chemically active film that receives the circuit pattern during lithographic exposure (DUV/EUV), enabling selective development, etching, and subsequent pattern transfer to the wafer. While lithography tools and masks are high-profile assets, photoresist performance directly governs pattern quality, throughput, and ultimately yield. Any sustained disruption in photoresist supply can therefore halt wafer output in fabs.

This dependency is amplified by stringent performance and integration requirements. Photoresists must be highly sensitive at the relevant wavelength to support acceptable scanner throughput, form uniform films with strong adhesion, and remain mechanically and chemically stable through downstream steps (etch, cleans, stripping). These materials are typically co-developed and qualified with fabs for specific process windows, tool settings, and patterning stacks. Once qualified for high-volume manufacturing, changing resist formulations or suppliers can trigger lengthy requalification and yield risk, creating high switching costs and practical vendor lock-in.

The supply base is highly concentrated, with Japanese suppliers holding an estimated ~90% share, notably JSR and Tokyo Ohka Kogyo (TOK).⁽⁴⁶⁾ This market structure increases systemic exposure to disruptions affecting a small set of producers (manufacturing incidents, quality excursions, logistics interruptions) and heightens sensitivity to policy or geopolitical events. The 2019 Japan–South Korea export licensing changes affecting certain semiconductor chemicals, including EUV photoresist, illustrate how regulatory actions can translate into near-term supply uncertainty for dependent manufacturing regions.⁽⁴⁷⁾ Even where alternative sourcing exists, substitution is constrained by qualification timelines and by extreme purity requirements, where trace contamination can produce unacceptable defect rates and shipment rejections.

⁽⁴⁶⁾ [Japan - Semiconductors | U.S. International Trade Administration](#)

⁽⁴⁷⁾ [The South Korea-Japan Trade Dispute in Context: Semiconductor Manufacturing, Chemicals, and Concentrated Supply Chains | U.S. International Trade Commission](#)

Although strategically significant, as attested by the acquisition of JSR by Japan's state-backed fund JIC, ⁽⁴⁸⁾ the photoresist sector is comparatively small and specialised, requiring sustained R&D and high-purity manufacturing capabilities. This combination of high technical barriers, concentrated incumbency, and tight fab integration suggests persistent dependency risk, particularly for leading-edge nodes and EUV processes.

1.3.1.3.2.2 Polysilicon

High-purity polysilicon serves as feedstock for production of silicon wafers. Stringent purity requirements exist in order to ensure that resultant wafers have no deformities or impurities that would inhibit the function and performance of fabricated chips.

Today's polysilicon market is bifurcated. The vast majority (>90%) is manufactured to support relatively lower purity photovoltaic (PV) applications. The PV segment is dominated by Chinese suppliers.

That contrasts with electronic- or semiconductor-grade (EG) polysilicon, which has been historically produced outside of China at a more even supply-demand balance. In the EG segment, Germany's Wacker Chemie ("Wacker") is a market leader, alongside other key players from the U.S., Japan, and South Korea.

Additionally, the input material required to produce both PV and EG polysilicon is metallurgical-grade silicon (MG-Si), for which global supply is heavily dependent on China.

1.3.1.3.2.3 Precursors

Precursors are complex molecules used in Atomic Layer Deposition (ALD) and Chemical Vapor Deposition (CVD), which enable the atomic-scale precision essential for fabricating transistors, interconnects, and memory structures in advanced chips. They represent one of the most knowledge-intensive, high-value segments of the semiconductor materials chain, and their production requires deep expertise in molecular design, purification, and process integration.

The global precursor market, though modest in size at around USD 1.7 billion in annual revenues in 2024, is strategically critical and growing rapidly. The market is projected to exceed USD 2.5 billion by 2029, a 47% increase from 2024,⁽⁴⁹⁾ driven by demand for advanced logic and 3D memory chips, and by the use of new materials such as cobalt, ruthenium, molybdenum, and ferroelectric high-k dielectrics. Metal and metal oxide precursors account for most of this growth, while dielectric and low-k materials are projected to remain large and stable segments.

The EU holds a globally leading position in the precursor market through its chemical champions Merck (Germany) and Air Liquide (France). These two companies together command over half of global market share in advanced precursors. Their strengths lie in chemical synthesis, purification, and integration with process equipment and fabs. Supporting firms such as BASF (Germany), Solvay (Belgium), Evonik (Germany), Umicore (Belgium) and DOCK Chemicals (Germany) complement this leadership through the development of specialised chemistries and R&D collaboration. These capabilities, backed by Europe's strong research ecosystem, make the region a cornerstone of global innovation in ALD and CVD

⁽⁴⁸⁾ [Japan-backed fund to buy chip materials maker JSR for \\$6.4 billion | Reuters](#)

⁽⁴⁹⁾ [The Outlook For The Precursor Market Remains Strong | Semiconductor Digest](#)

materials. On the other hand, Chinese firms such as Huate Gas, Nata Opto, and Jingrui are rapidly scaling capacity.

1.3.1.4 Manufactured inputs

1.3.1.4.1 Front-end manufacturing

1.3.1.4.1.1 Masks

Photomasks are **design-specific and critical input** to wafer fabrication: each product and process node requires a dedicated mask set, and delays in mask availability can directly gate tape-out schedules and production ramps. The supply base is structurally split between **captive production** (masks made in-house by leading foundries/IDMs) and the **merchant market** (external mask shops). Market analysis indicates that captive production increased from **35% - 65% of the global photomask market** between **2008 and 2020**, implying that firms without captive capability are increasingly reliant on a relatively smaller merchant capacity pool, which can tighten during upcycles. ⁽⁵⁰⁾

In the merchant segment, key suppliers include **Tekscend Photomask (Japan)**, **Dai Nippon Printing, DNP (Japan)**, **Photronics (United States)**, **SK-Electronics (Japan)**, and **Taiwan Mask Corporation, TMC (Taiwan)**. While no E headquartered companies are in this market, Tekscend has a production facility in Dresden that supplies leading-edge photomasks including for EUV lithography.

Upstream of mask shops, supply is further concentrated in **EUV mask blanks**, where a recent market summary reports that the top two manufacturers, **AGC (Japan)** and **HOYA (Japan)**, account for **around 93%** of the market, creating an additional dependency that can propagate into mask availability even where mask-making capacity exists. ⁽⁵¹⁾

1.3.1.4.2 Advanced packaging

1.3.1.4.2.1 T-Glass

Nittobo's **T-glass** is a specialised glass cloth used in the **package substrates** that support and connect advanced chips (the "carrier" that links the silicon to the rest of the device). Its purpose is to improve **dimensional stability under heat**, which helps reduce substrate warpage and supports manufacturing yields and reliability in large, high-power packages.⁽⁵²⁾ Nittobo explicitly positions this material as crucial for **semiconductor package substrates** used in **high-performance CPUs** and **AI semiconductors**, and also links it to **communications ASICs and switches**, making it relevant to data-centre compute and high-speed networking supply chains. ⁽⁵³⁾ From a resilience perspective, the key impact driver is **market concentration**: industry reporting places Nittobo at **around 90% market share** in the relevant semiconductor-materials glass fibre cloth segment (often referenced specifically as low-CTE/T-glass), indicating limited

⁽⁵⁰⁾ [EUV mask technologies: evolution and ecosystem for devices](#)

⁽⁵¹⁾ [ASML Holding Before Q4 Earnings: How Should Investors Play the Stock?](#)

⁽⁵²⁾ [A Critical AI Niche Is Dominated by One Little-Known Japanese Company - WSJ](#)

⁽⁵³⁾ <https://www.nittobo.co.jp/eng/business/electronicmaterials/index.htm>

redundancy and a heightened risk of bottlenecks if capacity, logistics, or qualification timelines are disrupted. ⁽⁵⁴⁾

1.3.1.4.2.2 Dielectric polymer film

When it comes to dielectric polymer film, a key insulating material used in CPUs and GPUs, 95% of supply is dependent on one manufacturer in Japan, Ajinomoto, with its Ajinomoto Build-up Film (ABF). ⁽⁵⁵⁾ This film is used in **build-up package substrates** that sit between the silicon die (e.g., CPU/GPU) and the printed circuit board, enabling the dense multilayer wiring and microvia structures needed to route signals from nanometre-scale on-chip circuitry to millimetre-scale system interconnects. ⁽⁵⁶⁾

1.3.1.5 Manufacturing equipment ⁽⁵⁷⁾

The manufacturing process for a chip is equipment intensive and as is the case across the semiconductor value chain, the equipment ecosystem is fragmented and highly specialised. For the purpose of simplicity, this analysis will group the equipment market in two - front-end and back-end manufacturing.

Front-end manufacturing (FEOL/BEOL wafer fabrication) comprises the processes used to form semiconductor devices and interconnect structures on a silicon wafer, including transistor formation, dielectric and metal layer deposition, patterning, etching, and planarisation. **Back-end manufacturing** (assembly, packaging, and test) comprises post-fabrication operations that separate the wafer into individual dies and integrate each die into a package, including die attach, electrical interconnection (e.g., wire bond or flip-chip), encapsulation, thermal/mechanical integration, and final electrical test.

1.3.1.5.1 Front end equipment

When it comes to front-end equipment, the EU's most significant lever is **lithography (approx. 92%)**. This is a strong position in a critical process step, but it is also highly concentrated in one segment. In contrast, **front-end wafer-fab equipment as a whole** is led by the **United States** with a market share of approximately 40%, followed by **Japan** at approximately 28% and **Korea** at 24%, with the EU remaining in **single digits**.⁽⁵⁸⁾ This distribution indicates that Europe's influence over upstream manufacturing capacity is not commensurate with its lithography strength.

1.3.1.5.1.1 Deposition

Deposition equipment comprises chemical vapour deposition (CVD) and plasma-enhanced CVD for dielectrics and spacers, physical vapour deposition (PVD, sputter) for metals and liners, atomic layer deposition (ALD) for ultra-thin conformal films (including high-k and barriers),

⁽⁵⁴⁾ <https://www.digitimes.com/news/a20260204PD225/nittobo-nikkei-2028-launch-materials.html>

⁽⁵⁵⁾ [Ajinomoto pledges to invest millions to produce material that's vital to semiconductor packaging | TechRadar](#)

⁽⁵⁶⁾ [Ajinomoto Build-up Film \(ABF\) | Innovation Story | Innovation | The Ajinomoto Group Global Website - Eat Well. Live Well.](#)

⁽⁵⁷⁾ Bonnet, P., Ciani, A., Molnar, J., & Nardo, M. (2025). EU's strengths and weaknesses in the global semiconductor sector (JRC141323, EUR 40253). Luxembourg: Publications Office of the European Union. <https://doi.org/10.2760/6302476>

⁽⁵⁸⁾ Bonnet, P., Ciani, A., Molnar, J., & Nardo, M. (2025). EU's strengths and weaknesses in the global semiconductor sector (JRC141323, EUR 40253). Luxembourg: Publications Office of the European Union. <https://doi.org/10.2760/6302476>

and, in advanced FEOL, epitaxy reactors for selective Si/SiGe growth. Here, the leading vendors are primarily non-European, notably Applied Materials (US), Tokyo Electron (JP) and LAM (US), with a significant European position in ALD through ASM (NL).

In 2023, the deposition equipment market totalled USD 23.1bn in sales and was dominated by Applied Materials (US) at 54% market share and Lam Research (US) at 14%, Tokyo Electron at 13% and ASM (NL) at 10% representing the most significant EU position in this sub-segment.⁽⁵⁹⁾

1.3.1.5.1.2 Lithography

Lithography is the manufacturing step that transfers a circuit pattern onto a silicon wafer. A photomask contains the pattern for one layer. The wafer is coated with a light-sensitive film (photoresist), then a lithography tool projects light through the reticle to expose the resist. The wafer is developed so parts of the resist are removed, leaving a temporary patterned layer that acts as a stencil.

Lithography combines the exposure tool (i.e. optical exposure) with resist processing (coater/developer tracks) to transfer mask patterns into photoresist, which subsequently guides etch or implant.

In 2023, lithography sales were at USD 25.1bn and were overwhelmingly concentrated in ASML (NL) with a 92% market share, with small EU shares held by SUSS MicroTec (DE, 0.5%) and EV Group (AT, 0.2%). Within the Extreme Ultraviolet (EUV) segment, required for the most leading-edge chips, ASML holds 100% market share, with Canon (JP) and Nikon (JP) being competitors in Deep Ultraviolet (DUV) machines.

Resist processing equipment sales in 2023 were USD 3.4bn and were highly concentrated in Tokyo Electron (JP) with a market share of 92%, with SUSS MicroTec (DE) the only EU player with a measurable share of 2.3%.

1.3.1.5.1.3 Etch

Etch is the manufacturing step that selectively removes material from the wafer to transfer a pattern into an underlying layer. After lithography creates a patterned photoresist “stencil”, etch removes exposed regions of a target film (or silicon) while protected regions remain, thereby forming features such as trenches, holes, and device structures.

Etch is performed using either dry (plasma) etching, which offers high precision and vertical sidewalls, or wet chemical etching, which is used where high selectivity is required. Etch is critical because it determines the shape and dimensions of features and must stop accurately on the intended layer to avoid defects and yield loss.

The dry processing segment reached USD 15.6bn in 2023, with market leadership held by Lam Research (US) with a market share of 44.5%, followed by Tokyo Electron (JP) with a market share of 21% and Applied Materials (US) with a market share of 18%. EU presence was marginal (for example PVA TePla (DE) with a marginal market share of 0.3%).

⁽⁵⁹⁾ Bonnet, P., Ciani, A., Molnar, J., & Nardo, M. (2025). EU’s strengths and weaknesses in the global semiconductor sector (JRC141323, EUR 40253). Luxembourg: Publications Office of the European Union. <https://doi.org/10.2760/6302476>

When it comes to wet wafer processing systems, sales were USD 6.0bn in 2023, led by SCREEN (JP) with a market share of 35%, Tokyo Electron (JP) with a market share of 21% and Lam Research (US) with a market share of 16%. EU suppliers in this segment have a small market share with for example Siconnex (AT) at 0.3% of etch revenues and 0.1% market share for RENA (DE).

1.3.1.5.1.4 Clean

Clean is the manufacturing step that removes contamination and process residues from the wafer to prevent defects and enable reliable subsequent processing. It is used throughout FEOL and BEOL, including after lithography and etch (to remove photoresist and etch by-products), before deposition (to prepare surfaces), and after CMP (to remove slurry particles).

Cleaning is carried out using wet chemical processes (on batch wet benches or single-wafer tools) and, where needed, dry cleaning/ashing (often plasma-based) for resist and organic removal. Clean is yield-critical because microscopic particles or residual films can cause shorts, opens, poor adhesion, or increased leakage.

In the wet processing segment, 2023 market share data indicate the predominant role of Japanese suppliers. Here, SCREEN (JP) leads with a market share of 35%, followed by Tokyo Electron (JP) with market share of 21% and to a lesser extent by Lam (US) with a market share of 16%. In this segment EU suppliers (Siconnex (AT), RENA (DE), SEMYSCO (DE)) are present but play a relatively minor role.

When it comes to dry processing, LAM (US) in 2023 a market share of 44.5%, Tokyo Electron (JP) had a market share of 21% and Applied Materials (US) at 18%.

1.3.1.5.1.5 Metrology and inspection

Metrology and inspection are the manufacturing activities that measure features on a wafer and detect defects so the process can be controlled, and yield can be maintained.

The market for this segment amounted to USD 10.3bn in 2023 and was highly concentrated in KLA (US) with a market share of 60% and Applied Materials (US) at 12%, with EU suppliers holding smaller but relevant shares, including ASML (NL) with a market share of 6%, Bruker AXS (DE, 1%) and Semilab (HU, 1%).

For reticle inspection and repair (a critical enabler for lithography yield), the 2023 market was led by Lasertec (JP) with 50% market and KLA (US) with 43% market share. Zeiss (DE) accounts for a 5% market share and represents the principal EU presence in this segment

1.3.1.5.1.6 Planarisation

Planarisation is the process of flattening the wafer surface to ensure subsequent lithography and layer integration remain within focus and uniformity tolerances. In semiconductor manufacturing it is implemented primarily through chemical mechanical planarisation (CMP), which removes material using a combination of chemical reactions and mechanical polishing to restore a controlled, planar surface.

CMP equipment sales were USD 2.7bn in 2023 and were concentrated in Applied Materials (US) with a market share of 56% and Ebara (JP) at 30%, with no EU supplier reported as having a material global share in this segment.

1.3.1.5.2 Back-end

Assembly and packaging are the final steps in turning finished wafers into packaged chips and boards for end users. Assembly typically includes **wafer dicing and thinning, bonding and interconnect, moulding and sealing (encapsulation), inspection and handling and test equipment**. Packaging provides the electrical connections needed for signal transmission, power delivery, and voltage regulation, while also managing heat dissipation and providing the physical protection required for long-term reliability. ⁽⁶⁰⁾

In 2023, Japan accounted for 48% of the global market (up from 33% in 2017) and recorded the highest compound annual growth rate (15%) among the leading countries during the COVID-19 period and its aftermath. Japan also held a dominant position in dicing equipment, controlling over 92% of the market in 2023. In packaging equipment, Japan captured 51.4% of the global market in 2023, increasing to 75.3% in moulding and sealing systems.⁽⁶¹⁾ Singapore's global market share declined to 21% in 2023 (from 35% in 2017), reflecting its concentrated specialisation in bonding equipment, particularly wire bonding. In 2023, Singapore accounted for over 81% of global wire bonding sales (up from 7.5% in 2017). Singapore also held an effective monopoly in integrated assembly systems, with a 97% market share in 2023; the remaining 3% was held by Grohmann Engineering (DE). ⁽⁶²⁾

In 2023, the European Union held 14.5% of the global market for assembly and packaging equipment, down from 16% in 2017. The EU had limited to no presence in the dicing and assembly equipment segments. However, it maintained a significant position in bonding equipment, holding 26% of the global market in 2023, driven in particular by die attaching, where the EU's market share reached 43%. The EU was also a leading supplier in lead-finishing and marking systems, together with the Republic of Korea, jointly accounting for 34% of the global market in 2023. Finally, in moulding and sealing systems, the EU held 13% of the global market in 2023, ranking second to Japan. ⁽⁶³⁾

1.3.1.5.2.1 Wafer dicing and thinning

Wafer dicing is the process of separating the wafer into individual dies after wafer processing. It is executed by blade sawing or laser dicing, depending on materials and edge-quality requirements. Wafer thinning is the process of reducing wafer thickness to meet packaging requirements. It is performed primarily by backside grinding, often followed by polishing or stress-relief treatments, with the wafer supported on a carrier to prevent mechanical damage.

⁽⁶⁰⁾ Bonnet, P., Ciani, A., Molnar, J., & Nardo, M. (2025). EU's strengths and weaknesses in the global semiconductor sector (JRC141323, EUR 40253). Luxembourg: Publications Office of the European Union. <https://doi.org/10.2760/6302476>

⁽⁶¹⁾ Bonnet, P., Ciani, A., Molnar, J., & Nardo, M. (2025). EU's strengths and weaknesses in the global semiconductor sector (JRC141323, EUR 40253). Luxembourg: Publications Office of the European Union. <https://doi.org/10.2760/6302476>

⁽⁶²⁾ Bonnet, P., Ciani, A., Molnar, J., & Nardo, M. (2025). EU's strengths and weaknesses in the global semiconductor sector (JRC141323, EUR 40253). Luxembourg: Publications Office of the European Union. <https://doi.org/10.2760/6302476>

⁽⁶³⁾ Bonnet, P., Ciani, A., Molnar, J., & Nardo, M. (2025). EU's strengths and weaknesses in the global semiconductor sector (JRC141323, EUR 40253). Luxembourg: Publications Office of the European Union. <https://doi.org/10.2760/6302476>

In dicing and wafer thinning, dependence is structurally high. In 2023, DISCO (JP) has a market share of 83% in blade sawing. In laser sawing, DISCO (JP) has a market share of 78% and ACCRETECH/Tokyo Seimitsu (JP) has a market share of 14%. Backside grinding is similarly concentrated, with DISCO (JP) having a market share of 86%, while European participation is limited - for example G&N (DE) has a market share of 1.2%.

1.3.1.5.2.2 Bonding and interconnect

Bonding and interconnect equipment comprises the tools used to attach the semiconductor die to a package substrate and create the electrical connections between the die and the package.

Here, Europe's strongest position is in die attach (die attaching equipment). BESI (NL) has a global market share of 43% in 2023, followed by ASMPT (SG) with a market share of 21%. This concentration implies that a meaningful portion of global die attach capability is European-origin. However, Europe's position weakens in wire bonding. Kulicke & Soffa (SG) has a market share of 53% and ASMPT (SG) has a market share of 29%, while German suppliers Hesse (DE) has a market share of 5% and F&K Delvotec (DE) has a market share of 2%.

1.3.1.5.2.3 Moulding, sealing and finishing

Moulding, sealing and finishing equipment comprises the tools used to encapsulate and complete packaged semiconductor devices after the die has been attached and electrically connected.

In this segment, the dependency is again concentrated outside Europe. TOWA (JP) has a market share of 61% in moulding and sealing systems and APIC Yamada (JP) has a market share of 14%, while BESI (BE) has a market share of 13%, indicating a meaningful European position. In lead finishing and marking, BESI (BE) has a market share of 32%, alongside EO Technics (KR) with a market share of 26%. Smaller European presences include ROFIN (DE) with a market share of 1.3% and PacTech (DE) with a market share of 0.6%.

1.3.1.5.2.4 Inspection and handling

Inspection and handling equipment comprises the tools used to detect defects and manage product movement through packaging and test operations.

In this segment, the equipment ecosystem shows mixed dependency with only minor European footholds. In wafer-level packaging inspection systems, Onto Innovation (US) has a market share of 42%, Camtek (IL) has a market share of 28%, and KLA (US) has a market share of 27%, while Unity SC (FR) has a market share of 3%. In package handling equipment, Cohu (US) has a market share of 27% and Pentamaster (MY) has a market share of 10%. Europe is represented by SPEA (IT) with a market share of 3.2%, alongside marginal shares for German suppliers.

1.3.1.5.2.5 Test equipment

Test equipment comprises the tools used to verify that semiconductor devices meet electrical performance and reliability requirements before shipment and, in some cases, during intermediate production stages.

In test equipment, Europe's presence is concentrated in specific niches rather than the largest-volume segments. For system-on-chip test systems, Advantest (JP) has a market share of 59%

and Teradyne (US) has a market share of 31%, while SPEA (IT) has a market share of 1.5%. In burn-in test systems, European suppliers have more material positions: ELES (IT) has a market share of 5% and EDA Industries (IT) has a market share of 1.5%.

In handlers and probers (including wafer probing), leadership is again non-European, with ACCRETECH/Tokyo Seimitsu (JP) having a market share of 43% and Tokyo Electron (JP) having a market share of 29%.

1.3.2. Establishing a starting point for BAU scenario

a) Upstream segments

Table 6. Mapping of the upstream segments in the chips value chain. *Source: compiled by the authors.*

GVC segment	Value added characteristics	EU strengths	EU gaps	EU share in the global market	Chips Act relevance
IP EDA	Low-to-moderate capital intensity, very high R&D intensity. Value created through innovation, IP, and system integration. Profit margins typically 20–40%, driven by IP licensing and high switching costs.	One of the 3 EDA market leaders, Mentor Graphics, has been acquired by Siemens EDA, reducing EU's overdependence on US software tools ⁽⁶⁴⁾. ⁽⁶⁵⁾	The EU is dependent on the US, the UK, and Japan for Intellectual Property (IP) providers, which are vital for semiconductor design, with companies such as Cadence, Synopsys, or ARM being prominent in this area ⁽⁶⁶⁾. Many EU companies rely on Cadence and Synopsys due to long-term engagements and the significant costs and delays associated with switching EDA suppliers ⁽⁶⁷⁾.	EU27 share of the global semiconductor EDA market in 2023: 20.6 % ⁽⁶⁸⁾ EU27 share of the global semiconductor IP/licensing market in 2023: 0 % (the EU27 currently has no market share in this segment; the leading player is ARM in the United Kingdom). ⁽⁶⁹⁾	Pillar I: European Design Platform enables fabless SMEs and start-ups to design chips without incurring high software licensing costs. Offers collaborative prototyping environments. Competence Centres give fabless firms practical support, technical advice, and networking with foundries or integrators. Pilot Lines allow fabless companies to validate and prototype their designs on European technology

⁽⁶⁴⁾ DECISION Études & Conseil. (2024). *Economic analysis of the EU and global chips ecosystem*

⁽⁶⁵⁾ Ebrahimi, A. (2024). *Groundbreaking chip sovereignty: Europe's strategic push in the semiconductor race*. Ifri Memos, Institut français des relations internationales (IFRI). ISBN 979-10-373-0874-0.

⁽⁶⁶⁾ DECISION Études & Conseil. (2024). *Economic analysis of the EU and global chips ecosystem*

⁽⁶⁷⁾ DECISION Études & Conseil. (2024). *Economic analysis of the EU and global chips ecosystem*

⁽⁶⁸⁾ IDC (2025). Semiconductors D3: Second interim study report (Version 3.0). Prepared for the European Commission.

GVC segment	Value added characteristics	EU strengths	EU gaps	EU share in the global market	Chips Act relevance
					nodes Chips Fund (EIB/EIF instrument) provides access to capital for fabless start-ups, which often face large funding gaps in the design-to-tape-out stage. Also indirectly related to Pillar II and Pillar III.
Chemicals and raw materials	High technological barriers, stringent purity standards. Relatively moderate profit margins (10–15%), but materials quality (e.g. purity) critically determines chip yield and performance. Strategic sensitivity:	The EU holds a competitive edge in the supply of gases and chemicals necessary for advanced semiconductor manufacturing processes including etching and cleaning chemicals, fluorinated process gases, and CMP slurries. European suppliers are global leaders in several of these segments, underscoring chemicals as a core and indispensable strength of the EU ecosystem. ⁽⁷⁰⁾	Raw materials essential for semiconductor production are scarce and not necessarily extracted or produced within the EU, leading to heavy reliance on foreign imports ⁽⁷²⁾ The EU is reliant on critical materials like gallium, with 35% of the gallium used in the EU	The EU benefits from a strong industrial ecosystem, with leading players such as Merck, Air Liquide, BASF, Umicore, Atlas Copco (including Edwards Vacuum), and Linde. These EU players accounted for EUR 12 billion in sales on the global semiconductor materials market in 2021, representing a 24% market	Linked to Pillar III: Tracking of raw material dependencies and activation of emergency mechanisms.

⁽⁶⁹⁾ IDC. (2025). Semiconductors D3: Second interim study report (Version 3.0)

⁽⁷⁰⁾ DECISION Études & Conseil. (2024). *Economic analysis of the EU and global chips ecosystem*. Study for the European Commission, Directorate-General for Communications Networks, Content and Technology (DG CNECT).

GVC segment	Value added characteristics	EU strengths	EU gaps	EU share in the global market	Chips Act relevance
	supply chains concentrated in East Asia and the US; Europe is vulnerable in raw material extraction and refining , yet it holds strong and often market-leading positions in high-purity chemicals and specialty gases, which are indispensable for global semiconductor production.	The EU has significant domestic capacity for ultra-purified silicon, which is the most widely used material for producing silicon wafers, and is a net exporter of this material ⁽⁷¹⁾	being refined in Germany from raw gallium originating in China, which holds 98% of the world's production ⁽⁷³⁾ The EU faces potential foreign dependencies and risks of import disruption for other input products related to front-end manufacturing processes, including Bromine (with imports concentrated from Israel at 51%), Phosphorus (from Kazakhstan at 88%), Halides (from the US at 57%), Artificial Corundum (from China at 67%), and Chlorides (from Argentina at 60%) ⁽⁷⁴⁾	share ⁽⁷⁵⁾	

⁽⁷²⁾ European Court of Auditors. (2025). *The EU's strategy for microchips: Reasonable progress in its implementation, but the Chips Act is very unlikely to be sufficient to reach the overly ambitious Digital Decade target* (Special Report No. 12/2025). Publications Office of the European Union. <https://www.eca.europa.eu/en/publications/SR-2025-12>

⁽⁷¹⁾ Bonnet, P., Ciani, A., Molnar, J., & Nardo, M. (2025). *EU's strengths and weaknesses in the global semiconductor sector* (JRC141323, EUR 40253). Luxembourg: Publications Office of the European Union. <https://doi.org/10.2760/6302476>

⁽⁷³⁾ Cerutti, I., & Nardo, M. (2023). *Semiconductors in the EU: State of play, future trends and vulnerabilities of the semiconductor supply chain* (JRC133850, EUR 31625 EN). Luxembourg: Publications Office of the European Union. <https://doi.org/10.2760/038299>

⁽⁷⁴⁾ Cerutti, I., & Nardo, M. (2023). *Semiconductors in the EU: State of play, future trends and vulnerabilities of the semiconductor supply chain*

⁽⁷⁵⁾ DECISION Études & Conseil. (2024). *Economic analysis of the EU and global chips ecosystem*.

GVC segment	Value added characteristics	EU strengths	EU gaps	EU share in the global market	Chips Act relevance
Wafers and substrates	Moderate capital intensity but high precision; margins typically 15–25%. Key differentiator for advanced nodes and power semiconductors. Bottlenecks can constrain the entire manufacturing chain; wafer supply has long lead times (12–24 months).	The EU has a relatively strong global position in SOI wafers, with Soitec and Siltronic being notable players	Limited production scale compared to Asian competitors. Japan leads the market with 56% ⁽⁷⁶⁾ China holds large shares in key materials for wafers, such as silicon, accounting for 64% of the global supply ⁽⁷⁷⁾ and is also the dominant source of primary gallium, which is critical for GaN wafer and substrate manufacturing.	Europe's overall Europe's share in wafer production is 14% ⁽⁷⁸⁾	Linked to Pillar II (Funds new wafer fabs (Si, SiC, GaN) and advanced substrate production) and Pillar III, but with important limitations in direct intervention on substrate materials production.
Semiconductor manufacturing equipment	Extremely high technological and IP barriers; cumulative R&D intensity >10 % of revenue. Profit margins relatively high (20–30 %), driven by	The EU holds a strong global position in front-end equipment, particularly in photolithography ⁽⁷⁹⁾ ASML, an EU-based company, has a monopolistic position in EUV lithography and a strong	The EU is reliant on foreign suppliers, mostly from the US and partly from Japan, for etching and cleaning (e.g., LAM Research), metrology & quality control (e.g., KLA Tencor), and other front-	For front-end equipment in 2022, EU companies held a 24.4% market share ⁽⁸¹⁾ The EU's market share in the total equipment market	Linked with Pillar I: Providing public-funded pilot lines, prototyping and testing facilities. Linked with Pillar II: Equipment is essential for

⁽⁷⁶⁾ Cerutti, I., & Nardo, M. (2023). *Semiconductors in the EU: State of play, future trends and vulnerabilities of the semiconductor supply chain*

⁽⁷⁷⁾ Cerutti, I., & Nardo, M. (2023). *Semiconductors in the EU: State of play, future trends and vulnerabilities of the semiconductor supply chain*

⁽⁷⁸⁾ Cerutti, I., & Nardo, M. (2023). *Semiconductors in the EU: State of play, future trends and vulnerabilities of the semiconductor supply chain*

⁽⁷⁹⁾ DECISION Études & Conseil. (2024). *Economic analysis of the EU and global chips ecosystem*

GVC segment	Value added characteristics	EU strengths	EU gaps	EU share in the global market	Chips Act relevance
	after-sales service and installed base. Equipment defines achievable process nodes and is a main determinant of competitive advantage.	position in lithography equipment holding an 88% market share in 2022. ASML is also a significant supplier of metrology & inspection equipment, with a 12% global market share ⁽⁵⁰⁾ Overall, the EU is well-positioned in the equipment segment, acting as a net exporter with significant domestic production capacity in specialised machines for wafers and semiconductors	end segments (e.g. Applied Materials) ⁽⁸⁰⁾ Due to the absence of advanced manufacturing in Europe, sales of advanced equipment such as EUV machines in the EU is close to null.	was 26.4% in 2023 ⁽⁸²⁾	scaling domestic fabs. <i>Indirectly supporting the demand for the equipment</i>

⁽⁸¹⁾ DECISION Études & Conseil. (2024). *Economic analysis of the EU and global chips ecosystem*

⁽⁸⁰⁾ DECISION Études & Conseil. (2024). *Economic analysis of the EU and global chips ecosystem*

⁽⁸²⁾ Bonnet, P., Ciani, A., Molnar, J., & Nardo, M. (2025). *EU's strengths and weaknesses in the global semiconductor sector* (JRC141323, EUR 40253)

1.3.3. Semiconductor design, production and packaging

GVC segment	Value added characteristics	EU strengths	EU gaps	EU share in the global market	Chips Act importance
Fabless Fab-lite design	Very high R&D intensity with strong dependence on advanced EDA and IP. Value created through innovation, system integration, and differentiated architectures. Profit margins typically 20–40 %, supported by design differentiation and IP ownership.	The EU has important expertise in designing analogue chips, radio frequency (RF) components, sensors & MEMS, power semiconductors, microcontrollers, and silicon photonics ⁽⁸³⁾ Major fabless companies such as Qualcomm, Apple and Nvidia have well-established design centres with a considerable number of employees located	The EU is not as strong in designing digital logic components, which are increasingly critical due to the rise of AI ⁽⁸⁴⁾, ⁽⁸⁵⁾. The EU has no leading pure-play fabless players ⁽⁸⁶⁾.	Total EU27 semiconductor device companies' world market share in 2023: 10.1 %. Within EU27 semiconductor company revenue, 97 % comes from companies with fabs and 3 % from fabless companies. ⁽⁸⁷⁾	Pillar I support mechanisms (European Design Platform, Competence Centres, Pilot Lines) reduce design costs and provide access to prototyping and integration support for fabless firms. Chips Fund provides capital to fabless start-ups, which face large funding gaps in the design-to-tape-out stage.

⁽⁸³⁾ DECISION Études & Conseil. (2024). *Economic analysis of the EU and global chips ecosystem*

⁽⁸⁴⁾ DECISION Études & Conseil. (2024). *Economic analysis of the EU and global chips ecosystem*

⁽⁸⁵⁾ Cerutti, Isabella & Nardo, Michela (2023). *Semiconductors in the EU: State of play, future trends and vulnerabilities of the semiconductor supply chain*. JRC Technical Report, JRC133850.

⁽⁸⁶⁾ DECISION Études & Conseil. (2024). *Economic analysis of the EU and global chips ecosystem*

⁽⁸⁷⁾ IDC (2025). *Semiconductors D3: Second interim study report (Version 3.0)*. Prepared for the European Commission.

	High productivity, skilled employment, spillovers to research and digital industries.	in the EU.			Also indirectly connected to Pillar II and Pillar III.
Manufacturing and Production Integrated Design Manufacturers/Fab-lite	Very high capital intensity (fabs, equipment, cleanrooms). Value created through process know-how, yield optimisation, and scale. Margins typically 15–30 %, depending on node and utilisation rates. Economic contribution through large-scale	The EU has expertise in designing and manufacturing analog chips, radio frequency (RF) components, sensors & MEMS, power semiconductors, microcontrollers, and silicon photonics ⁽⁸⁸⁾ .	The EU has capacity in ASICs (Application-Specific Integrated Circuits) and has limited manufacturing capacity for mature nodes (22 nm) and none for cutting-edge microchips (7 nm and below) ⁽⁸⁹⁾ The EU does not have any prominent pure-play foundry that focuses on manufacturing of	EU27 semiconductor manufacturing revenue in 2023: EUR 51 billion; EU27 global market share in semiconductor device manufacturing (IDM + fabless + memory) in 2023: 10.1 %; 97 % of all EU27 semiconductor device revenue comes from IDMs ⁽⁹²⁾ EU27 global foundry market share in 2023: 0.9 %, equal to EUR	Pillar II: first-of-a-kind facilities and state aid, which enable large-scale investments in front-end manufacturing. Complementary actions under Pillar I (pilot lines and competence centres) strengthen R&D–manufacturing linkages, while Pillar III ensures supply chain coordination

⁽⁸⁸⁾ DECISION Études & Conseil. (2024). *Economic analysis of the EU and global chips ecosystem*.

⁽⁸⁹⁾ European Court of Auditors. (2025). *The EU's strategy for microchips: Reasonable progress in its implementation, but the Chips Act is very unlikely to be sufficient to reach the overly ambitious Digital Decade target* (Special Report No. 12/2025). Publications Office of the European Union. <https://www.eca.europa.eu/en/publications/SR-2025-12>

⁽⁹²⁾ IDC. (2025). Semiconductors D3: Second interim study report (Version 3.0). Prepared for the European Commission.

	investment, supply chain anchoring, and regional employment multipliers.		advanced chipa ⁽⁹⁰⁾ . The only companies manufacturing advanced process nodes of 16nm and below in the EU are foreign companies such as Intel, GlobalFoundries, and TSMC ⁽⁹¹⁾ .	0.8 billion out of a EUR 96 billion global foundry market ⁽⁹³⁾	and crisis response.
Assembly, Test, and Packaging (ATP)	Moderate capital intensity; margins typically 10–20 %. Value created through precision, yield optimisation, and reliability assurance. Labour- and process-intensive, but increasingly automated and	Europe has developed advanced Photonic Integrated Circuit (PIC) assembly and packaging capabilities, supported by pilot lines such as PIXAPP and specialised facilities like PHIX. European SMEs hold strong global	The EU has no relevant OSAT company headquartered in Europe, and back-end manufacturing is largely located in Asia due to its labour-intensive and scale-driven cost structure. As a result, even European firms active in assembly and	The EU's share in global ATP capacity was 3% in 2022 and is projected to remain 3% in 2032 ⁽⁹⁷⁾	Pillar I, through advanced packaging pilot lines and under Pillar II, which enables industrial deployment of FOAK back-end facilities. ATP stakeholders also benefit from R&D funding under the Chips Joint

⁽⁹⁰⁾ DECISION Études & Conseil. (2024). *Economic analysis of the EU and global chips ecosystem*.

⁽⁹¹⁾ DECISION Études & Conseil. (2024). *Economic analysis of the EU and global chips ecosystem*.

⁽⁹³⁾ IDC. (2025). Semiconductors D3: Second interim study report (Version 3.0). Prepared for the European Commission.

⁽⁹⁷⁾ Boston Consulting Group (BCG) & Semiconductor Industry Association (SIA) (2024). *Emerging Resilience in the Semiconductor Supply Chain*. May 2024.

	digitised. Final stage of value capture which determines chip performance, thermal management, and system integration quality.	positions in the design and production of packaging and assembly tools for photonic ICs. Extensive know-how in PIC packaging, assembly, and testing provides Europe with a solid technological and industrial base in this niche segment ⁽⁹⁴⁾. The APECS pilot line funded through Pillar I of the Chips Act is also stimulating the development of advanced packaging competences in Europe.	testing typically operate their high-volume production sites outside the EU, leaving only limited domestic capacity for advanced or high-volume ATP processes. ⁽⁹⁵⁾ Most packaging solutions available in Europe rely on legacy approaches.⁽⁹⁶⁾		Undertaking.

⁽⁹⁴⁾ DECISION Études & Conseil. (2024). *Economic analysis of the EU and global chips ecosystem*.

⁽⁹⁵⁾ DECISION Études & Conseil. (2024). *Economic analysis of the EU and global chips ecosystem*.

⁽⁹⁶⁾ Rosati, N., Bonnet, P., Ciani, A., Duch Brown, N., Miguez, S., & Zaurino, E. (2023). *The EC consultation on the semiconductors' value chain* (JRC133892, EUR 31585 EN)

1.3.4. Downstream integration and end-use applications

GVC segment	Value added characteristics	EU strengths	EU gaps	EU share in the global market	Chips importance Act
Downstream integration	Integration requires high engineering and software competence and often represents 15–25% of the final system value. Value capture depends on the sophistication of system design, intellectual property, and brand reputation. Economies of scope matter more than economies of scale: integrators that control software–hardware co-design (e.g. Tesla, Apple) capture	The EU benefits from strong vertical integration and close collaboration between European automakers and domestic chipmakers, such as NXP, Infineon, and STMicroelectronics, which has enabled European firms to become global leaders in semiconductors for key end-markets such as automotive and industrial automation. This collaboration fosters a robust domestic ecosystem for application-specific	Collaboration between semiconductor producers and Tier-1 system suppliers remains fragmented, meaning that outside the automotive sector there are few structured co-development mechanisms, shared technology roadmaps, or early-stage joint design cycles. This limits the ability to translate semiconductor innovations into competitive system-level products in	No single figure available EU companies owned 34% of the global semiconductor market for automotive in 2021. European suppliers are leading in “embedded systems” for applications such as Automotive, Industrial & robotics, Energies, Health & Care, Aerospace / Defence / Security, and telecommunications infrastructures.	Pillar I (R&D and pilot lines for heterogeneous integration), Competence Centres that connect chipmakers with system integrators and OEMs Pillar II measures that promote regional coordination and supply chain completeness.

GVC segment	Value added characteristics	EU strengths	EU gaps	EU share in the global market	Chips importance Act
	disproportionate margins. Increasingly, integration involves vertical collaboration with chipmakers to co-optimize designs (e.g. automotive OEMs specifying chip architectures for autonomous driving).	semiconductors, particularly in the automotive and wider embedded-systems industries. ⁽⁹⁸⁾. European public-private partnerships (PPPs), chipmakers, and Original Equipment Manufacturers (OEMs) have effectively utilised a vertically integrated cost-and-risk-sharing ecosystem in the automotive sector ⁽⁹⁹⁾.	several EU end-markets. ⁽¹⁰¹⁾. Europe lags in co-design capabilities for AI accelerators, cloud, and edge-computing hardware, constraining its competitiveness in next-generation data-driven applications ⁽¹⁰²⁾, ⁽¹⁰³⁾. Most European integration capacity focuses on mature embedded systems (automotive,	Infineon, NXP, and STMicroelectronics collectively own approximately 60% of the global market shares for SIM cards and identity documents ⁽¹⁰⁵⁾.	

⁽⁹⁸⁾ Ebrahimi, A. (2024). *Groundbreaking chip sovereignty: Europe's strategic push in the semiconductor race*. Institut français des relations internationales (IFRI). ISBN 979-10-373-0874-0.

⁽⁹⁹⁾ Ebrahimi, A. (2024). *Groundbreaking chip sovereignty: Europe's strategic push in the semiconductor race*. Institut français des relations internationales (IFRI). ISBN 979-10-373-0874-0.

⁽¹⁰¹⁾ Ebrahimi, A. (2024). *Groundbreaking chip sovereignty: Europe's strategic push in the semiconductor race*. Institut français des relations internationales (IFRI). ISBN 979-10-373-0874-0.

⁽¹⁰²⁾ European Semiconductor Industry Association. (2025). *Position paper on EU Chips Act 2*. Brussels: ESIA.

GVC segment	Value added characteristics	EU strengths	EU gaps	EU share in the global market	Chips importance Act
		European suppliers are leaders in “embedded systems” for key downstream applications including Automotive, Industrial & robotics, Energy, Health & Care, Aerospace / Defence / Security, and telecommunications infrastructures ⁽¹⁰⁰⁾ .	industrial). There is little domestic infrastructure for advanced packaging-to-system integration or prototyping of heterogeneous modules ⁽¹⁰⁴⁾ .		
End-use applications	Represents the largest aggregate economic value in the semiconductor chain, although distributed across many industries. Chips are	EU companies held 34% of the global semiconductor market for automotive in 2021. The EU’s		The EU has a strong market position in “embedded electronics industries,” which accounted for 64% of its semiconductor	Pillar I supports application-oriented R&D and competence centres. Pillar II secures manufacturing

⁽¹⁰³⁾ McKinsey & Company. (2024). McKinsey on semiconductors: *Creating value, pursuing innovation, and optimizing operations*. New York: McKinsey & Company.

⁽¹⁰⁵⁾ DECISION Études & Conseil. (2024). *Economic analysis of the EU and global chips ecosystem*.

⁽¹⁰⁰⁾ DECISION Études & Conseil. (2024). *Economic analysis of the EU and global chips ecosystem*.

⁽¹⁰⁴⁾ DECISION Études & Conseil. (2024). *Economic analysis of the EU and global chips ecosystem*.

GVC segment	Value added characteristics	EU strengths	EU gaps	EU share in the global market	Chips importance Act
	also increasingly the key enabler of innovation in a digital and AI-driven economy, since they determine the performance, efficiency, and functionality of products ranging from vehicles and industrial machinery to consumer electronics and AI systems. Chips account for 10–40% of the total cost of complex products (e.g. 35% in electric vehicles, ~25% in smartphones, ~15% in industrial	semiconductor demand is aligned with its embedded electronic production, with power & analogue, optoelectronics and sensors, and microcontrollers accounting for 63% of EU semiconductor consumption in 2022, compared to 39% globally ⁽¹⁰⁶⁾.		consumption in 2022, compared to 22% globally ⁽¹⁰⁷⁾.	capacity for critical sectors such as automotive, energy, and defence. Pillar III includes end-user industries in supply chain monitoring and crisis response.

⁽¹⁰⁶⁾ DECISION Études & Conseil. (2024). *Economic analysis of the EU and global chips ecosystem*.

⁽¹⁰⁷⁾ DECISION Études & Conseil. (2024). *Economic analysis of the EU and global chips ecosystem*.

GVC segment	Value added characteristics	EU strengths	EU gaps	EU share in the global market	Chips importance Act
	machinery). Value capture at this stage depends on product differentiation, brand equity, and software-enabled services (e.g. mobility platforms, IoT ecosystems). Strong spill-over effects to employment, R&D intensity, and regional competitiveness.				

Overall view

Table 7 below summarises the European Union's position along the global semiconductor value chain, combining quantitative indicators of market share and import dependency with a qualitative assessment of resilience and strategic importance. The figures illustrate that dependencies vary significantly by stage: while the EU holds strong positions in manufacturing equipment it remains heavily reliant on non-EU suppliers for wafer substrates, chip manufacturing, and especially assembly, test, and packaging (ATP). The resilience profile column highlights the nature of vulnerabilities that range from geopolitical and supply chain concentration risks; whereas the final column identifies each segment's strategic relevance for achieving the objectives of the EU Chips Act.

IDC 2023 revenue data confirm this asymmetric positioning. EU27-headquartered firms account for roughly 28 % of global capital-equipment revenues, around 21 % of the EDA market (largely reflecting the role of Siemens following its acquisition of Mentor Graphics), and about 17 % of semiconductor materials sales. By contrast, Europe's share of global foundry revenues is below 1 %, and OSAT and IP/licensing activities are negligible. The semiconductor device segment itself represents about 10 % of worldwide device revenues, driven mainly by IDMs such as Infineon, NXP and STMicroelectronics. This pattern underscores that the EU's comparative advantages lie upstream in equipment, design tools and materials, whereas it remains structurally weak in pure-play foundry, back-end services and leading-edge logic production, with important implications for resilience and policy design.

Table 7. The overview table of the EU semiconductors value chain. *Source: compiled by the authors.*

GVC Segment	EU Market Share	Dependency (imports)	Resilience profile	EU strategic importance
Materials	16.8 % in Materials as reported by IDC	39.5 % ⁽¹⁰⁸⁾	High exposure to geopolitical risks and export restrictions. Fundamental input for the entire semiconductor chain; disruption affects all downstream segments. Core enabler for front-end manufacturing and new wafers (SiC, GaN). Vulnerable to external shocks and capacity bottlenecks.	Ensuring access to high-purity materials and gases is essential for resilience and security of supply. Identified as a priority for strategic reserves and mandatory monitoring.
IP	~0% global share	Not applicable	Dominated by US providers, and ARM (UK-based, but owned by Softbank group, JP); structural dependency in key logic & AI IP	Critical upstream input ; absence of EU IP limits autonomy in advanced logic design
EDA	~20.6% (2023, IDC)	Not applicable (software)	Low → Moderate: EU presence exists (Siemens EDA), but ~80% dependency on US vendors	Essential for sovereign chip design capability ; limited EU presence, although significant participant in the western EDA

⁽¹⁰⁸⁾ Cerutti, Isabella & Nardo, Michela (2023). *Semiconductors in the EU: State of play, future trends and vulnerabilities of the semiconductor supply chain*. JRC Technical Report, JRC133850.

				ecosystem.
Semiconductor Manufacturing Equipment	~24–26 % of global equipment market (2023) 27.9 % in Capital equipment (2023) as reported by IDC	24.2% ⁽¹⁰⁹⁾	Identified as a strategic chokepoint due to concentration of suppliers and long lead times. EU leadership (ASML) gives strategic leverage globally, but dependency on certain US and Japanese (e.g. Tokyo Electron) is also significant. Very limited market for EUV/advanced manufacturing equipment in Europe.	Central to sustaining EU's comparative advantage in advanced manufacturing.

⁽¹⁰⁹⁾ Cerutti, Isabella & Nardo, Michela (2023). *Semiconductors in the EU: State of play, future trends and vulnerabilities of the semiconductor supply chain*. JRC Technical Report, JRC133850.

Semiconductor manufacturing	For foundry services: 0.9% (2023 IDC) For ATP: ~3 % of global ATP capacity (2022; projected constant to 2032) IDC (2023) reports a negligible market share) For IDMs: 10.1% (2023 IDC)	64% ⁽¹¹⁰⁾	Foundry: Moderate. new fabs help stabilise share; leading-edge gap persists ATPs: Lack of data transparency and extensive offshoring to Asia create major blind spots. This vulnerability was clearly exposed during the COVID-19 pandemic, when lockdown-related shutdowns of ATP facilities in Asia disrupted global supply and caused cascading shortages across downstream industries. Also, no real-time monitoring of back-end capacity or stockpiles. IDMs: Moderate. strong in automotive/power; weak in logic & memory	An integrated manufacturing chain, spanning front-end fabs, IDMs and advanced back-end (ATP), is the single critical enabler of Europe's autonomy, resilience and competitiveness in semiconductors.
Downstream Integration	No consolidated figure; ~34% share in global automotive semiconductors; ~60 % in SIM/ID chips	~70%*	EU downstream actors lack supply chain visibility and incentives for proactive management, although some end-customers have already begun diversifying their supplier base and geographic footprint as part of their own risk-mitigation strategies. However, these	Key to turning chip production into competitive industrial systems (automotive, robotics, energy).

⁽¹¹⁰⁾ Cerutti, Isabella & Nardo, Michela (2023). *Semiconductors in the EU: State of play, future trends and vulnerabilities of the semiconductor supply chain*. JRC Technical Report, JRC133850.

			diversification efforts remain uneven across sectors and are not yet integrated into a coordinated EU-wide resilience framework.	
End-Use Applications	~34 % global share in automotive semiconductors; 64 % of EU semiconductor demand in embedded industries (vs 22 % global)	<i>Demand side, not considered in this analysis of semiconductor supply dependencies</i>	Explicitly mentioned as excluded from current Chips Act crisis-response mechanisms. Largest economic and societal exposure to chip shortages. The EU has very limited presence in consumer electronics, particularly smartphones, which are the principal drivers of demand for leading-edge logic. This limits Europe's influence over supply allocation and reinforces dependence on third-country manufacturing ecosystems.	Incorporating end-users into resilience governance is vital for long-term preparedness and industrial continuity.

*There is no direct indicator for downstream integration dependency, as trade data in the semiconductor value-chain study stop at the chip level.

1.3.5. Modelling the BAU scenario

The dynamic baseline modelling builds directly on the quantitative and qualitative figures presented in the previous table, which summarises the European Union's current position across each segment of the semiconductor global value chain. These baseline indicators covering market share, import dependency, and resilience profile serve as the starting point for projecting the EU's relative performance to 2035 (with a check in point in 2028). Each value represents the best available estimate for 2021–2023, derived from Joint Research Centre dependency ratios, BCG–SIA and McKinsey capacity assessments, and complementary evidence from IFRI, DGE, and Eurostat.

In addition to these structural indicators, the modelling draws on IDC's 2023–2030 forecast series on revenue, which captures verified investment pipelines, corporate announcements, and regional growth expectations. The dataset reflects both global market recovery after the 2022 downturn and strong European capital formation driven by public subsidies and private investment in new fabs and equipment capacity.

To inform the long-run BAU trajectory, it is important to note that growth patterns in semiconductor devices largely determine the evolution of the entire value chain, since device demand drives equipment orders, EDA tool requirements, materials usage, and foundry utilisation. This relationship underpins the approach taken for post-2030 modelling.

Table 8. Compound Annual Growth Rates (CAGR) by Value Chain Segment, 2023–2030. Source: IDC 2030 study reporting.

Segment	IDC projection in 2030 (EUR Billion)	Projected CAGR 2023 – 2030	Projected European share of global market in 2030
Intellectual Property (IP)	-	-	-
Electronic Design Automation (EDA)	3.247	7,7 %	17,9%
Capital equipment	62.785	9,9 %	33,5%
Foundry services	1.007	3,0 %	0,5%
OSAT	-		-
Semiconductor devices	85.073	7,7 %	9,6%
Materials	14.319	5,1 %	18,7%
Total	166.432	8.3%	11.6%

To extend the BAU projection to 2035, we are applying a rate consistent with long-term global semiconductor trends observed in the literature. WSTS publishes only short- to medium-term forecasts, but a range of industry sources provide useful evidence for long-term semiconductor market growth. According to the WSTS Spring 2025 forecast, the global semiconductor market is expected to rebound strongly, expanding by +15.4 % in 2025 to USD 728 billion, followed by +9.9 % growth in 2026 to USD 800 billion. Looking further ahead, several independent analyses converge around a mid-single-digit long-term Compound Annual Growth Rate (CAGR). RootsAnalysis projects a 5.08 % CAGR from 2024 to 2035 for the global semiconductor market. Alvarez & Marsal, using WSTS historical data, assume a 5–

6 % CAGR to support their projection that the industry will reach USD 1 trillion by the mid-2030s. Similarly, the Futurum Group states that the semiconductor industry has stabilised around a 6 % long-term growth rate, which they adopt as the benchmark for their forecasts. Taken together, these sources justify the use of a 5–6 % compound annual growth rate (CAGR) as an industry consensus long-term assumption for modelling global semiconductor market expansion. Given these structural conditions, Europe’s semiconductor value chain revenues are assumed to grow in line with but below global averages.

In addition, the modelling distinguishes between value-chain segments according to their exposure to global AI-driven growth. Semiconductor devices shape demand for upstream activities and therefore drive overall value-chain dynamics. However, only certain upstream segments in Europe are positioned to benefit from AI-related revenue expansion. In particular, EDA and capital equipment suppliers, including ASML, are tightly linked to global leading-edge logic and AI accelerator demand, and their revenues can therefore be assumed to follow the global long-run CAGR (5-6%). In contrast, materials, devices, and foundry services in the EU remain tied to mature-node production as well as automotive and industrial applications, justifying a more conservative 3-4 % CAGR over 2030–2035.

Table 9. Assumptions for the revenue growth model. *Source: Compiled by the authors.*

Parameter	Global market	Europe (BAU)	Comment
2030–2035 CAGR	5–6 %	Two rates applied: 5–6 % for EDA and equipment; 3–4 % for materials, devices, and foundry (3.5% taken as a central estimate)	Adjusted for limited exposure to AI-driven growth and mature product mix
Growth driver	AI logic, HBM, accelerators	Automotive, power, industrial semiconductors	ASP divergence
Relative global share	Concentration in Asia and US	Stable at 11–12 % ⁽¹¹⁾	No structural capacity shift expected
Key risks	AI-cycle volatility, trade barriers, CAPEX constraints	Energy prices, project delays, limited AI participation	Structural, not cyclical

The BAU projection therefore applies differentiated growth assumptions across value-chain segments, with EDA and equipment following a 5–6 % CAGR and materials, devices and foundry following a 3–4 % CAGR. To illustrate these differentiated growth paths, the 2030 IDC values for the relevant segments (Table 2) are projected forward to 2035:

- **EDA (EUR 3.247 bn, 2030)**
 - 5 % CAGR → **EUR 4.14 bn in 2035**
 - 6 % CAGR → **EUR 4.33 bn in 2035**

⁽¹¹⁾ Europe’s recent revenue share has shown short-term volatility due to downturns in automotive and industrial semiconductors, although its medium-term structural share typically remains within the 10–12 % range.

- **Capital equipment (EUR 62.785 bn, 2030)**
 - 5 % CAGR → **EUR 80.2 bn in 2035**
 - 6 % CAGR → **EUR 83.9 bn in 2035**

Subtotal for EDA + equipment in 2035:
EUR 84.3–88.2 bn

- **Devices (EUR 85.073 bn, 2030), as also discussed in section 13.1.1, and included here for the sake of completeness**
 - 3 % CAGR → **EUR 98.7 bn**
 - 4 % CAGR → **EUR 103.5 bn**

- **Materials (EUR 14.319 bn, 2030)**
 - 3 % CAGR → **EUR 16.6 bn**
 - 4 % CAGR → **EUR 17.4 bn**

- **Foundry (EUR 1.007 bn, 2030)**
 - 3 % CAGR → **EUR 1.17 bn**
 - 4 % CAGR → **EUR 1.22 bn**

Subtotal for materials + devices + foundry in 2035:
EUR 116.5–122.1 bn

Combined EU27 semiconductor value chain projection for 2035:

- **Low case:** $84.3 + 116.5 \approx$ **EUR 200.8 bn**
- **High case:** $88.2 + 122.1 \approx$ **EUR 210.3 bn**
- **Central estimate** $\approx$ **EUR 205 bn**

Under the revised BAU assumption, which now reflects the distinct growth trajectories of AI-exposed (EDA, equipment) and mature-node (materials, devices, foundry¹¹²) activities, the EU27 semiconductor value chain increases from EUR 166.4 billion in 2030 to approximately EUR 201–210 billion in 2035. The central estimate of EUR 205 billion reflects the uplift from globally exposed equipment and EDA segments. Over the full 2023–2035 period, the EU27 semiconductor value chain is therefore projected to grow from EUR 95.9 billion to around EUR 205 billion. This corresponds to a cumulative increase of roughly 114 % and an average annual growth rate of around 6.4 %, with most of the expansion occurring before 2030, which is consistent with the assumptions in the BAU scenario described above.

From this baseline, the modelling assesses how changes in capacity, demand, and policy conditions influence Europe’s competitiveness and vulnerability over time. This approach captures both quantitative trends, such as shifts in market share or dependency, and qualitative changes in resilience.

The forward-looking assessment is structured around three key drivers: capacity evolution, demand dynamics, and policy and geo-economic conditions. Together, these drivers

¹¹² Foundry here refers to foundry activities by EU headquartered companies, which exclusively manufacture mature node semiconductors.

determine how Europe's market share, import dependency, and resilience are likely to develop under the business-as-usual scenario and under alternative policy scenarios.

Capacity evolution

- **Effect on market share:** New fabrication plants, wafer facilities, or equipment production increase the EU's contribution to global output. Additional European capacity therefore lifts market share relative to global totals.
- **Effect on import dependency:** Higher domestic output reduces the need for imports. Delays, cost overruns, or slow uptake of First-of-a-Kind facilities, as noted by the European Court of Auditors (2025), limit these gains.
- **Effect on resilience:** More domestic capacity increases redundancy and reduces supply chain length, improving resilience in front-end manufacturing and materials.

Policy and geo-economic conditions

- **Regulatory shocks:** Export controls, sanctions, or other restrictions reduce access to parts of the global supply chain and raise import dependency in affected segments.
- **Critical-material constraints:** Shortages of inputs such as gallium, germanium, or neon limit potential production growth. Diversification measures or strategic reserves help ease these constraints. The EU also remains exposed to export restrictions on critical materials such as gallium and germanium, where China dominates global processing and has already introduced targeted export controls. Diversification measures and the development of strategic reserves are intended to mitigate these risks, although their impact is expected to remain gradual over the baseline period.
- **Supplier concentration:** High global concentration in foundries and back-end service providers increases systemic risks and lowers resilience.
- **Environmental disruptions:** More frequent floods, storms, and droughts can interrupt global semiconductor production and logistics, as seen in Taiwan and Japan. These events increase volatility in import availability and may heighten dependency in the short term. Strengthening monitoring, stockpiling, and diversification helps mitigate these risks.
- **Positive policy levers:** Investments supported by the Chips Joint Undertaking, IPCEIs, and State-aid schemes can accelerate technology diffusion and expand domestic capacity. These measures can improve market share and resilience while gradually lowering import dependency.

Overview of Business-as-Usual (BAU) scenario

The Business-as-Usual (BAU) modelling indicates that Europe's position in the global semiconductor value chain remains broadly stable, but increasingly constrained by demand as consumption grows faster than domestic production through to 2035. Installed wafer-fabrication capacity in Europe is projected to reach around 1.39 million wafers per month (300 mm equivalent) by 2030, an increase of approximately 31 percent compared with 2023, with a **3.9% annual growth rate**. Applying assumed organic growth of 2% to 4% per year from 2030 onwards to reflect incremental brownfield expansion and future, currently unannounced projects, **overall capacity is projected to reach between 1.54 and 1.69 million wafers per month by 2035**. Given that global capacity is expected to expand at 3% to 5% per year, Europe's share of global wafer capacity therefore remains relatively stable at around 8%.

However, capacity stability contrasts with an expansion in European chip demand, especially from the automotive and industrial sectors. The World Semiconductor Trade Statistics (WSTS) projects a 75% increase in semiconductor shipments to Europe between 2017 and 2027, while the European semiconductor market which is valued at around EUR 50 billion in 2023 continues to grow ⁽¹¹³⁾. The automotive segment alone represents approximately 37% of semiconductors shipped to Europe, expanding from EUR 13.05 billion in 2023 to EUR 17.38 billion by 2026, an 8.2 percent CAGR ⁽¹¹⁴⁾. This is driven by rising semiconductor intensity per vehicle, particularly in electric and connected models that integrate up to 3,000 chips per unit, compared with 1,000–1,500 in conventional vehicles. Parallel growth in the industrial and communication sectors with shipments of analogue, logic, and sensor components up by 30–40% since 2020 further amplifies domestic consumption ⁽¹¹⁵⁾.

Although Europe has expanded its semiconductor manufacturing capacity since the COVID-19 shortages, in the long term this growth remains insufficient to keep pace with projected increases in semiconductor consumption. As a result, apparent consumption continues to outstrip domestic output, and import dependence remains high. Only limited improvements are visible in the upstream segments, where diversification efforts modestly reduce reliance on non-EU inputs.

Europe retains a strong position in lithography through ASML, which helps sustain a stable share of roughly 25% in this specific subsegment of semiconductor manufacturing equipment. However, this strength does not extend across the full equipment landscape.

By contrast, front-end manufacturing shows limited change: new fabs in Ireland, France, and Germany help stabilise Europe's position, but dependency remains close to 50% and market share around 9%. Here, very high dependency remains when it comes to advanced logic and memory. The most significant vulnerabilities persist in assembly, test, and packaging, where dependency exceeds 60%, and in downstream integration, where reliance on external suppliers for around 70% of system assembly continues.

Under the Business-as-Usual trajectory, the resilience of Europe's semiconductor value chain improves only marginally and unevenly across segments. Incremental capacity additions and limited diversification reduce exposure in a few upstream areas, particularly chemicals, and wafer substrates, but systemic vulnerabilities persist in the front-end and back-end stages where Europe remains structurally import-dependent. Resilience gains are further offset by external factors, including high global concentration in foundries and packaging services and the rising incidence of environmental disruptions, such as floods, storms, and droughts. These events have already disrupted semiconductor production in regions such as Taiwan and Japan and increase volatility in supply availability. As a result, the overall resilience profile stabilises rather than strengthens, with systemic exposure largely unchanged.

Table 10. Assumed direction for EU market share, import dependency and resilience under BAU scenario.

⁽¹¹³⁾ European Commission, Joint Research Centre. (2025). *EU's strengths and weaknesses in the global semiconductor sector (JRC141323)*. Publications Office of the European Union. <https://data.europa.eu/doi/10.2760/6302476>

⁽¹¹⁴⁾ Compound Annual Growth Rate.

⁽¹¹⁵⁾ European Commission, Joint Research Centre. (2025). *EU's strengths and weaknesses in the global semiconductor sector (JRC141323)*. Publications Office of the European Union. <https://data.europa.eu/doi/10.2760/6302476>

IDC Segment	EU Market Share (2023 → 2030 → 2035)	Import Dependency (2023 → 2030 → 2035)	Resilience Profile	Baseline summary
Intellectual Property (IP)	2023: <1 % 2030: <1 % 2035: stable	Not applicable	Low (→)	EU has limited IP footprint; ecosystem remains fragmented; dependency on US IP persists.
Electronic Design Automation (EDA)	2023: 21 % 2030: 18 % 2035: stable	Not applicable	Low → Moderate (↑)	Slight gains from EU design-ecosystem initiatives; strong reliance on US EDA vendors remains.
Capital Equipment	2023: 28 % 2030: 34 % 2035: slow growth	2023: ~50 % 2030: stable 2035: stable	High (→)	Strong leadership from ASML; dependence on US/Japanese process equipment persists.
Foundry Services	2023: 1 % 2030: 1 % 2035: stable	2023: 24 % 2030: stable 2035: stable	Moderate (↑)	EU remains dependent on overseas leading-edge foundries.
OSAT	2023: <1 % 2030: <1 % 2035: stable	2023: ~64 % 2030: stable 2035: slow decline	Low → Moderate (↑)	Limited reshoring for automotive and SiC; Asia maintains dominance.
IDMs and fabless	2023: 10 % 2030: 10 % 2035: stable	2023: ~50 % 2030: stable 2035: stable	Moderate (→)	Mature-node strength supports stability; limited exposure to AI logic caps growth. Very high dependency when it comes to advanced logic and memory that in the dependency figure is masked by significant capacity targeting automotive and industrial automation end users.
Materials	2023: 17 % 2030: 19 % 2035: slow growth	2023: ~29–47 % 2030: slow decline 2035: slow decline	Moderate → Moderately high (↑)	Critical Raw Materials Act reduces dependency; risks persist for Chinese-controlled gallium/germanium supply.
End-Use Applications	2023: Automotive represents more than 37% of semiconductor shipments to	<i>Not applicable (demand-side)</i>	Moderate but uneven (→)	EU demand grows in automotive and industrial sectors; supply reliance remains high.

	Europe 2030: slow decline 2035: slow decline			

Justification for the assumptions above:

The baseline and forward-looking indicators presented above are derived from a triangulation of official statistics, Joint Research Centre (JRC) analysis, industry forecasts, and academic and policy literature. Each segment of the semiconductor global value chain (GVC) draws on a combination of quantitative trade data, capacity benchmarks, and qualitative assessments of resilience and dependency.

For the Intellectual Property (IP) segment, the 2023 baseline reflects Europe's marginal global footprint (below 1 %), consistent with IDC reporting (2023) as well as McKinsey (2024) ⁽¹¹⁶⁾ and IFRI (2024) ⁽¹¹⁷⁾, which highlight the structural dominance of US IP licensors. Since IP does not map onto trade flows, no import dependency metric is reported, and resilience is assessed as remaining low and stable over the baseline period

For Electronic Design Automation (EDA), Europe's 2023 market share (around 21 %) follows IDC's reporting but is projected to decline modestly toward 2030. Dependency cannot be measured through trade statistics, yet qualitative evidence from **BCG-SIA (2024)** ⁽¹¹⁸⁾ and **Interface (2024)** ⁽¹¹⁹⁾ suggests that Europe remains heavily reliant on US EDA vendors.

For **semiconductor manufacturing equipment**, the baseline EU market share of **28 % in 2023, rising toward 34 % in 2030 is captured by IDC, BCG (2021), and McKinsey (2024)** ⁽¹²⁰⁾. These sources identify Europe's enduring leadership in lithography (ASML) and metrology, balanced by continuing reliance on non-EU suppliers for other critical equipment categories, including etching, deposition, and ion implantation tools from the US, as well as mask exposure equipment and EUV light sources from Japan. While the lithography segment is expected to remain a structural strength for Europe, the broader equipment landscape continues to exhibit significant dependencies on US and Japanese technologies.

For foundry services, Europe's market share remains small (around 1 %), consistent with IDC and BCG-SIA (2024) data⁽¹²¹⁾. The dependency rate (~24 %) reflects Europe's continued

⁽¹¹⁶⁾ McKinsey & Company. (2024). *McKinsey on semiconductors: Creating value, pursuing innovation, and optimizing operations* (No. 9, March 2024). McKinsey & Company.

⁽¹¹⁷⁾ Ebrahimi, A. (2024). *Groundbreaking chip sovereignty: Europe's strategic push in the semiconductor race*. Ifri Memos, Institut français des relations internationales (IFRI). ISBN 979-10-373-0874-0.

⁽¹¹⁸⁾ BCG & Semiconductor Industry Association (2024). *Emerging Resilience in the Semiconductor Supply Chain*. Boston Consulting Group and Semiconductor Industry Association, May 2024.

⁽¹¹⁹⁾ Kleinhans, J.-P. (2024), *The missing strategy in Europe's chip ambitions: Member States must drive the next steps*, Interface, July 2024.

⁽¹²⁰⁾ McKinsey & Company. (2024). *McKinsey on semiconductors: Creating value, pursuing innovation, and optimizing operations* (No. 9, March 2024). McKinsey & Company.

⁽¹²¹⁾ **BCG & Semiconductor Industry Association (2024)**. *Emerging Resilience in the Semiconductor Supply Chain*. Boston Consulting Group and Semiconductor Industry Association, May 2024.

need for advanced-node and leading-edge wafer capacity located mainly in Taiwan, South Korea, and the US. New European fabs stabilise capacity but do not materially change global share or structural dependence.

For **assembly, test, and packaging (ATP)**, the baseline dependency of around 64% is derived from the same JRC (2023) ⁽¹²²⁾ “chips” category after disaggregation. IDC reporting shows that **Europe’s market share remains negligible (<1 %)**, while McKinsey (2024) ⁽¹²³⁾ estimates that 85–90 percent of global packaging value is located in Asia. IFRI (2024) ⁽¹²⁴⁾ and SIA (2024) ⁽¹²⁵⁾ note limited reshoring of ATP for automotive and SiC devices, suggesting marginal gains in European share to 5–6 percent by 2035. Nonetheless, McKinsey (2025) ⁽¹²⁶⁾ emphasises that Europe’s back-end gap will remain its most persistent vulnerability.

For semiconductor vendors (including fabless), the baseline market share (~10 %) is drawn from IDC’s semiconductor device estimates, while the import dependency figure (~50 %) derives from the **JRC (2023)** ⁽¹²⁷⁾ “chips” dependency measure, adjusted to isolate front-end manufacturing. These values align with **BCG–SIA (2024)** ⁽¹²⁸⁾ findings that Europe holds only 9–10 % of global wafer capacity. Resilience is assessed as moderate, supported by Europe’s strong position in mature nodes but limited by minimal participation in leading-edge logic.

For materials (including gases, chemicals, and wafer substrates), Europe’s baseline market share (17 % in 2023, rising to 19 % in 2030) follows IDC segmentation, with import dependency values (29–47 %) derived from **JRC (2023)** ⁽¹²⁹⁾ estimates for chemicals, precursors, and wafers. Dependency is projected to decline slowly due to CRMA-driven diversification and expanded SiC and GaN substrate production, although structural reliance on Chinese-controlled gallium and germanium continues to constrain resilience.

The **downstream integration** segment (system assembly and electronic manufacturing services) is characterised by high import dependency of around 70% in 2023. This figure is based on Eurostat COMEXT trade statistics, BCG–SIA (2024) ⁽¹³⁰⁾ global supply chain analysis, and DGE (2024) ⁽¹³¹⁾. Minor reductions in dependency are consistent with

⁽¹²²⁾ Cerutti, Isabella & Nardo, Michela (2023). *Semiconductors in the EU: State of play, future trends and vulnerabilities of the semiconductor supply chain*. JRC Technical Report, JRC133850.

⁽¹²³⁾ McKinsey & Company. (2024). *McKinsey on semiconductors: Creating value, pursuing innovation, and optimizing operations* (No. 9, March 2024). McKinsey & Company.

⁽¹²⁴⁾ Ebrahimi, A. (2024). *Groundbreaking chip sovereignty: Europe’s strategic push in the semiconductor race*. Ifri Memos, Institut français des relations internationales (IFRI). ISBN 979-10-373-0874-0.

⁽¹²⁵⁾ **BCG & Semiconductor Industry Association (2024)**. *Emerging Resilience in the Semiconductor Supply Chain*. Boston Consulting Group and Semiconductor Industry Association, May 2024.

⁽¹²⁶⁾ **McKinsey & Company (2025)**. *Semiconductors have a big opportunity but barriers to scale remain*. February 2025.

⁽¹²⁷⁾ Cerutti, Isabella & Nardo, Michela (2023). *Semiconductors in the EU: State of play, future trends and vulnerabilities of the semiconductor supply chain*. JRC Technical Report, JRC133850.

⁽¹²⁸⁾ **BCG & Semiconductor Industry Association (2024)**. *Emerging Resilience in the Semiconductor Supply Chain*. Boston Consulting Group and Semiconductor Industry Association, May 2024.

⁽¹²⁹⁾ Cerutti, Isabella & Nardo, Michela (2023). *Semiconductors in the EU: State of play, future trends and vulnerabilities of the semiconductor supply chain*. JRC Technical Report, JRC133850. Publications Office of the European Union. ISBN 978-92-68-06549-5 (online). DOI: 10.2760/038299.

⁽¹³⁰⁾ **BCG & Semiconductor Industry Association (2024)**. *Emerging Resilience in the Semiconductor Supply Chain*. Boston Consulting Group and Semiconductor Industry Association, May 2024.

⁽¹³¹⁾ Direction Générale des Entreprises (DGE) (2024), *Les semi-conducteurs: un marché mondialisé et une dépendance européenne*, *Les Thémas de la DGE*, n° 27, Ministère de l’Économie, des Finances et de la Souveraineté industrielle et numérique, January 2024.

McKinsey (2025) ⁽¹³²⁾ projections of near-shoring in industrial automation and IFRI (2024) ⁽¹³³⁾ evidence of increased localisation in defence electronics and power systems.

Finally, **end-use applications** rely on WSTS (2024–2025) market data showing that semiconductor shipments to Europe amounted to about EUR 50 billion in 2023, with the automotive sector alone accounting for more than 37% of the semiconductors shipped to the region ⁽¹³⁴⁾. The WSTS Spring 2025 forecast, together with DGE (2024) ⁽¹³⁵⁾ and IFRI (2024) ⁽¹³⁶⁾, indicates that European semiconductor demand will continue expanding at 5–6% annually, with the automotive segment growing particularly fast at roughly 8.2% CAGR between 2023 and 2026. McKinsey (2025) ⁽¹³⁷⁾ and SIA (2024) ⁽¹³⁸⁾ imply that demand in embedded sectors will continue to rise faster than Europe’s domestic production capacity, reinforcing persistent import dependence.

1.4. The cost (price) competitiveness of the EU industry

In line with the Better Regulation Guidelines and the Better Regulation Toolbox (notably Tool #24 on Competition and Tool #21 on Competitiveness), the analysis distinguishes between two interrelated but distinct perspectives: intra-EU competition and extra-EU competitiveness. Here we focus on extra-EU competitiveness.

The extra-EU competitiveness perspective focuses on the cost and price competitiveness of EU semiconductor production in relation to global competitors. To assess Europe’s cost and price competitiveness in the global semiconductor industry, the analysis focuses on the **relative cost of production** in the EU compared with global benchmarks (Asian countries and U.S.), and on the **key cost drivers** that shape this gap.

1.4.1. Establishing a starting point for BAU scenario

Semiconductor manufacturing in the EU faces a **structurally higher cost base** than in leading East Asian hubs, with total fab production costs around 40–50% higher than in Taiwan, South Korea and China. ⁽¹³⁹⁾ Capital expenditure (CapEx) is the largest cost component, and capital efficiency in Europe is lower: producing a given manufacturing facility requires significantly more investment than in Taiwan, partly because fabs tend to be smaller on average and project lead times longer. Energy prices for industrial users are a major obstacle to investment, with electricity and gas costs well above US and Asian levels. Labour costs are also high when compared to other major regions: unit labour costs in EU fabs exceed those of major competitors, and estimates suggest that fab labour in Europe can

⁽¹³²⁾McKinsey & Company (2025). *Semiconductors have a big opportunity but barriers to scale remain*. February 2025.

⁽¹³³⁾Ebrahimi, A. (2024). *Groundbreaking chip sovereignty: Europe’s strategic push in the semiconductor race*. Ifri Memos, Institut français des relations internationales (IFRI). ISBN 979-10-373-0874-0.

⁽¹³⁴⁾ World Semiconductor Trade Statistics (WSTS) (2025), *Spring 2025 forecast summary and market data*, WSTS, Inc., May 2025

⁽¹³⁵⁾ Direction Générale des Entreprises (DGE) (2024), *Les semi-conducteurs: un marché mondialisé et une dépendance européenne*, Ministère de l’Économie, des Finances et de la Souveraineté industrielle et numérique, January 2024.

⁽¹³⁶⁾ Ebrahimi, A. (2024). *Groundbreaking chip sovereignty: Europe’s strategic push in the semiconductor race*. Ifri Memos, Institut français des relations internationales (IFRI). ISBN 979-10-373-0874-0.

⁽¹³⁷⁾ McKinsey & Company (2025). *Semiconductors have a big opportunity but barriers to scale remain*. February 2025.

⁽¹³⁸⁾ Boston Consulting Group (BCG) and Semiconductor Industry Association (SIA) (2024), *Attracting chips investment: Industry recommendations for policymakers*, August 2024.

⁽¹³⁹⁾ Decision Etudes & Conseil and YOLE Group, *Competitiveness of the EU semiconductor manufacturing industry*, Nov. 2025.

be two to three times more expensive than in East Asia, alongside specific bottlenecks in skilled construction trades and some technical roles. At the same time, the semiconductor industry is highly R&D-intensive globally, investing around 22% of revenues in R&D and 26% in capital expenditure. Finally, the EU is heavily reliant on imports of many specialty materials, gases and chemicals, which, despite a strong domestic supplier base in some segments, exposes the European semiconductor ecosystem to supply disruptions and price volatility.

The newly available evidence⁽¹⁴⁰⁾ confirms and strengthens these patterns. Recent benchmarking of fab-level cost structures shows that total semiconductor production costs in the EU remain structurally above those of all major competitors: EU = 100 (baseline), US = 84, Japan = 84, China = 61, Taiwan = 53, and South Korea = 50. This implies that, on average, EU fabs operate at a 16% cost premium relative to the US and at a 40–50 % premium relative to leading Asian hubs.

Two additional structural factors further widen the EU cost base ⁽¹⁴¹⁾:

- First, the cost of capital is considerably higher in the EU than in competing regions. The weighted average cost of capital (WACC) for semiconductor manufacturers operating in the EU is 8.3 %, exceeding that of the US (7.3 %), Japan (8.2 %), China (6.1 %), Taiwan (4.8 %), and South Korea (4.4 %). Higher equity risk premia in Europe, lower market capitalisation of EU-based semiconductor firms, and high exposure to cyclical automotive markets contribute to elevated financing costs.
- Second, unit labour costs in EU manufacturing fabs (0.38 in PPP terms) remain noticeably higher than in the US (0.35) and significantly above levels in China (0.15), Taiwan (0.12), Japan (0.16), and South Korea (0.11). Crucially, this gap is not driven by nominal wages but by lower labour productivity in EU fabs combined with considerably higher employers' social contributions, which in several EU Member States are among the highest in the OECD.

In the table below we outline the available evidence from the literature on the key cost components and possible benchmark figures in comparison to EU's global competitors such as USA, China and Taiwan.

Table 11. Key cost drivers in the Chips industry. *Source: compiled by the authors.*

Driver	Description	Knowledge base from the literature and additional details
Capital intensity and scale	High construction and equipment costs per wafer capacity. Smaller average fab size ⁽¹⁴²⁾ and higher	Constructing a new, state-of-the-art facility is expensive, with location-specific construction and equipment costs being significant drivers of investment decisions ⁽¹⁴³⁾ .

⁽¹⁴⁰⁾Decision Etudes & Conseil and YOLE Group, *Competitiveness of the EU semiconductor manufacturing industry*, Nov. 2025.

⁽¹⁴¹⁾Decision Etudes & Conseil and YOLE Group, *Competitiveness of the EU semiconductor manufacturing industry*, Nov. 2025.

⁽¹⁴²⁾ The reference to “smaller average fab size” is based on evidence that Europe’s semiconductor ecosystem is dominated by mid-scale fabs focused on mature-node, automotive, power, and analog manufacturing, rather than the large leading-edge

	compliance costs inflate EU unit costs.	Wafer fabrication, or front-end manufacturing, accounts for 64% of the industry's capital expenditure ⁽¹⁴⁴⁾. A state-of-the-art semiconductor fab can require roughly USD 5 billion for mature node fabs to USD 20 billion for advanced logic and memory fabs in capital expenditure, including land, building, and equipment ⁽¹⁴⁵⁾. Evidence by Decision & Yole ⁽¹⁴⁶⁾ shows that this effect is compounded in the EU by higher financing costs: semiconductor firms operating in Europe face an average WACC of 8.3 %, substantially higher than in Korea (4.4 %), Taiwan (4.8 %), or China (6.1 %). The industry and its supply chain depend on high utilisation (typically more than 75%) for favourable economics, subsidies, and lower capital utilisation could lead to further boom and bust cycles ⁽¹⁴⁷⁾. Large-scale operations can significantly reduce costs at fabs ⁽¹⁴⁸⁾.
Energy costs	Electricity and gas prices for large industrial consumers; Europe's exposure to volatile energy markets increases operational expenditure per wafer.	Energy prices in Europe are two to three times higher than in the US ⁽¹⁴⁹⁾. Subsidies for utilities can also differ, with Mainland China offering up to 70% and Taiwan 30% ⁽¹⁵⁰⁾. Some regions, like Germany, may offer caps on energy costs as part of subsidy packages for new fabs ⁽¹⁵¹⁾.

megafabs typical of Asia and the US, which achieve significantly greater economies of scale. Evidence drawn from JRC, IFRI, Interface, and industry reports (McKinsey, BCG, SIA) supports this structural distinction.

⁽¹⁴³⁾**Semiconductor Industry Association (SIA)** and **Boston Consulting Group (BCG)**, *Attracting Chips Investment: Industry Recommendations for Policymakers*, August 2024.

⁽¹⁴⁴⁾Boston Consulting Group (2021), *Strengthening the Global Semiconductor Supply Chain: A report by BCG and the Semiconductor Industry Association (SIA)*.

⁽¹⁴⁵⁾Boston Consulting Group (2021), *Strengthening the Global Semiconductor Supply Chain: A report by BCG and the Semiconductor Industry Association (SIA)*.

⁽¹⁴⁶⁾Decision Études & Conseil and YOLE Group, *Competitiveness of the EU semiconductor manufacturing industry*, Nov.2025

⁽¹⁴⁷⁾**McKinsey & Company (2025)**. *Semiconductors have a big opportunity but barriers to scale remain*. February 2025.

⁽¹⁴⁸⁾McKinsey & Company (2021), *McKinsey on Semiconductors: Creating value, pursuing innovation, and optimising operations*.

⁽¹⁴⁹⁾DECISION Études & Conseil. (2025). *European consumption of mainstream chips from third countries: Draft final report* (Contract No. EC-CNECT/2024/LVP/0074). European Commission, Directorate-General for Communications Networks, Content and Technology (DG CNECT).

⁽¹⁵⁰⁾DECISION Études & Conseil. (2025). *European consumption of mainstream chips from third countries*

⁽¹⁵¹⁾ **Boston Consulting Group (BCG) & Semiconductor Industry Association (SIA)**. (May 2024). *Emerging Resilience in the Semiconductor Supply Chain*.

		The updated 2025 data show that wholesale gas prices in the EU are around 2.8 times higher than in the US, directly translating into industrial electricity prices that are 137 % above US levels because of Europe's marginal pricing system ⁽¹⁵²⁾ .
Labour and productivity	Labour costs and productivity in semiconductor manufacturing and equipment operation.	Labour costs are a major factor in construction cost differences. Labour costs in Europe can be two to three times more expensive than in Asia ⁽¹⁵³⁾. Furthermore, labour productivity in major US fabs (Intel, Texas Instruments, GlobalFoundries) is roughly twice the level observed in leading EU fabs (Infineon, STMicroelectronics, Bosch), resulting in higher unit labour costs despite comparable nominal wages. Moreover, EU employers' social contributions, often double those in the US, further elevate total labour costs ⁽¹⁵⁴⁾. Maintenance costs, heavily influenced by labour rates and overtime, can be up to 50% higher in the US and 30% higher in Europe compared to East Asia ⁽¹⁵⁵⁾. The increased demand for skilled craft workers means projects often use less experienced workforces, exacerbating productivity issues and extending project timelines ⁽¹⁵⁶⁾. The industry faces a massive talent gap for engineers, estimated at over 100,000 each in the US and Europe, and upward of 200,000 in Asia-Pacific (excluding China). This talent challenge extends across the entire semiconductor value chain, including equipment design and manufacturing ⁽¹⁵⁷⁾.
Research and Development	Continuous innovation in chip design, materials, and	Designing a new state-of-the-art system-on-chip (SoC) for a flagship smartphone can exceed USD 1 billion ⁽¹⁵⁸⁾ , ⁽¹⁵⁹⁾ .

⁽¹⁵²⁾ Decision Etudes & Conseil and YOLE Group, *Competitiveness of the EU semiconductor manufacturing industry*, Nov.2025

⁽¹⁵³⁾ **McKinsey & Company (2025)**. *Semiconductors have a big opportunity but barriers to scale remain*. February 2025.

⁽¹⁵⁴⁾ Decision Etudes & Conseil and YOLE Group, *Competitiveness of the EU semiconductor manufacturing industry*, Nov.2025

⁽¹⁵⁵⁾ DECISION Études & Conseil. (2025). *European consumption of mainstream chips from third countries*

⁽¹⁵⁶⁾ **McKinsey & Company (2025)**. *Semiconductors have a big opportunity but barriers to scale remain*. February 2025.

⁽¹⁵⁷⁾ McKinsey & Company (2021), *McKinsey on Semiconductors: Creating value, pursuing innovation, and optimising operations*.

⁽¹⁵⁸⁾ Boston Consulting Group (2021), *Strengthening the Global Semiconductor Supply Chain: A report by BCG and the Semiconductor Industry Association (SIA)*.

(R&D) and design costs	manufacturing processes requires sustained high R&D spending. Advanced-node development drive significant fixed costs, while limited EU design scale raises per-project expenditure.	For a 5nm chip, design costs, including validation and IP qualification, are about USD 540 million, significantly higher than the USD 175 million for a 10 nm chip or USD 300 million for a seven nm chip ⁽¹⁶⁰⁾. The semiconductor industry has a high level of intensity in R&D, accounting for 22% of annual final chip revenues ⁽¹⁶¹⁾. Design activities account for 65% of the total industry R&D ⁽¹⁶²⁾.
Materials and inputs	Speciality gases, wafers, and chemicals' import dependency adds cost and risk premiums.	Specialty gases, chemicals, metals, and other materials are identified as a top cost item in the semiconductor industry ⁽¹⁶³⁾. Many essential raw materials, such as gallium, germanium, copper, and tungsten, are concentrated in a few locations globally. This concentration increases the dependence of intermediary chemical producers in these specific locations, some of which are geopolitically sensitive. This characteristic makes the supply chain vulnerable to disruptions or necessitates sourcing more expensive alternatives. It may also potentially lead to higher costs if trade restrictions are imposed ⁽¹⁶⁴⁾. Since companies often import many materials, border costs such as tariffs, fees, customs clearance, and regulatory approvals are decisive factors in cost assessments ⁽¹⁶⁵⁾.

Overall, we see that **capital intensity and scale** remain the dominant driver: building and equipping a state-of-the-art fab can require between **USD 4 billion and USD 20 billion** ⁽¹⁶⁶⁾, with **wafer fabrication alone accounting for around 64 % of total capital expenditure**. Smaller average fab sizes and higher compliance costs in Europe inflate per-wafer unit costs compared with Asia, where large-scale operations achieve substantial economies of scale.

⁽¹⁵⁹⁾ Cerutti, Isabella & Nardo, Michela (2023). *Semiconductors in the EU: State of play, future trends and vulnerabilities of the semiconductor supply chain*. JRC Technical Report, JRC133850.

⁽¹⁶⁰⁾ McKinsey & Company (2021), *McKinsey on Semiconductors: Creating value, pursuing innovation, and optimising operations*.

⁽¹⁶¹⁾ Boston Consulting Group (2021), *Strengthening the Global Semiconductor Supply Chain: A report by BCG and the Semiconductor Industry Association (SIA)*.

⁽¹⁶²⁾ Cerutti, Isabella & Nardo, Michela (2023). *Semiconductors in the EU: State of play, future trends and vulnerabilities of the semiconductor supply chain*. JRC Technical Report, JRC133850.

⁽¹⁶³⁾ Boston Consulting Group (BCG) and Semiconductor Industry Association (SIA) (2024), *Attracting chips investment: Industry recommendations for policymakers*, August 2024.

⁽¹⁶⁴⁾ **McKinsey & Company (2025)**. *Semiconductors have a big opportunity but barriers to scale remain*. February 2025.

⁽¹⁶⁵⁾ Boston Consulting Group (BCG) and Semiconductor Industry Association (SIA) (2024), *Attracting chips investment: Industry recommendations for policymakers*, August 2024.

⁽¹⁶⁶⁾ Building on BSC figure, converted to EUR from USD.

When all major components (capital, labour, energy, land) are combined, EU fabs remain 16% more expensive than US fabs and up to 50% more expensive than leading Asian fabs ⁽¹⁶⁷⁾.

1.4.2. Modelling the BAU scenario

Building on the state of play overview above we provide a logical inference on how EU

Information anchors
Global investment and cost structure: Industry plans roughly USD 1 trillion of new fabs by 2030 ⁽¹⁶⁸⁾, but structural cost gaps remain due to site productivity, logistics, and cluster effects. Europe faces higher construction and operating costs and slower ramp-ups compared with leading Asian sites. Build-and-commission timelines for EU based fabs are around 34 months, compared to 19 months in Taiwan. ⁽¹⁶⁹⁾
Node mix and ecosystem gaps: Europe's strengths are in automotive, power, analogue and sensors, with limited leading-edge logic. There are clear gaps in back-end, advanced packaging and substrates, which increasingly determine system-level performance and cost.
Talent constraints: Skills shortages in engineering and skilled trades are a binding constraint in Europe as well as the US and Asia, affecting time-to-build and OPEX.
Materials and inputs: The EU remains dependent on imported specialty gases, chemicals and critical raw materials with concentrated global supply, adding price and disruption risk premia.

Capital intensity and fab scale

- **Developments expected under BAU:** A number of EU greenfield and brownfield projects announced since 2023 complete construction and begin ramping. Local supplier bases deepen marginally, and experience curves reduce overruns. However, **average EU fabs remain smaller ⁽¹⁷⁰⁾ than Asian mega-fabs** and less embedded in very large, turnkey industrial parks.
- **Rationale:** Persistent **barriers to scale** in Europe and North America include higher construction costs and logistics frictions; the **European Court of Auditors (ECA)** underlines that public support levels and timelines fall short of transforming EU market share quickly ⁽¹⁷¹⁾. In addition, Europe faces structurally higher financing costs: the weighted average cost of capital (WACC) for semiconductor manufacturers is 8.3% in the EU, compared with 7.3 % in the US, 6.1 % in China, 4.8 % in Taiwan,

⁽¹⁶⁷⁾ Decision Etudes & Conseil and YOLE Group, *Competitiveness of the EU semiconductor manufacturing industry*, Nov.2025

⁽¹⁶⁸⁾ **McKinsey & Company (2025).** *Semiconductors have a big opportunity but barriers to scale remain*. February 2025.

⁽¹⁶⁹⁾ IDC “Semiconductors Market Data by Feature Size, Sector, and Region” Report

⁽¹⁷⁰⁾ The reference to “smaller average fab size” is based on evidence that Europe’s semiconductor ecosystem is dominated by mid-scale fabs focused on mature-node, automotive, power, and analog manufacturing, rather than the large leading-edge megafabs typical of Asia and the US, which achieve significantly greater economies of scale. Evidence drawn from JRC, IFRI, Interface, and industry reports (McKinsey, BCG, SIA) supports this structural distinction.

⁽¹⁷¹⁾ European Court of Auditors. (2025). *Special Report 12/2025 – The EU’s strategy for microchips: Reasonable progress in its implementation, but the Chips Act is very unlikely to be sufficient to reach the overly ambitious Digital Decade target*.

and 4.4% in South Korea ⁽¹⁷²⁾. These higher financing costs make large-scale investments more expensive to execute in Europe relative to leading competitors.

- **Implication for costs:** According to the comparative fab cost index by Decision & Yole ⁽¹⁷³⁾, Europe remains the highest-cost location among the major semiconductor manufacturing regions: EU = 100, US = 84, Japan = 84, China = 61, Taiwan = 53, Korea = 50. This evidence suggests that, even if some cost efficiencies materialise as EU sites mature, a significant structural cost gap remains between the EU and leading Asian ecosystems under a business-as-usual trajectory.

Operating expenditure (energy, labour, compliance)

- **Developments expected under BAU:** Energy markets stabilise relative to the 2022–2023 spike, with more long-term **power purchase agreements (PPAs)**, and **on-site renewables**. Labour productivity improves gradually through automation and learning, but **wage levels and compliance costs** in Europe remain structurally high. EU skills programmes, increased automation, and migration relieve the **worst shortages**, but global competition keeps talent **tight and expensive**. Construction and ramp-up timelines also remain longer in Europe, with typical build-and-commission periods of about 34 months compared with roughly 19 months in Taiwan, reinforcing cost and time-to-market disadvantages.
- **Rationale:** The ECA suggests **no near-term step-change** in competitiveness drivers from current policies ⁽¹⁷⁴⁾; McKinsey points to recurring OPEX headwinds in Europe and North America ⁽¹⁷⁵⁾. Europe faces structurally higher energy prices: the report shows that EU wholesale gas prices are around 2.8 times those in the US, which contributes to industrial electricity prices that are 137 % higher in the EU compared with the US. Labour cost pressures also persist with unit labour costs in EU semiconductor manufacturing (0.38) remaining above those in the US (0.35) and significantly above levels in Korea (0.11), Taiwan (0.12), China (0.15), and Japan (0.16), largely due to lower productivity and higher employers' social contributions in the EU ⁽¹⁷⁶⁾.
- **Implication for costs:** Europe remains a structurally higher-cost operating environment compared with major competitors. The report identifies energy and labour costs as two of the main contributors to the EU's higher fab cost index (EU = 100 vs 84 in the US) ⁽¹⁷⁷⁾. Under BAU, some efficiency gains may occur, but the evidence suggests that Europe's operating-cost disadvantage will persist.

Advanced packaging and substrates

⁽¹⁷²⁾ Decision Etudes & Conseil and YOLE Group, *Competitiveness of the EU semiconductor manufacturing industry*, Nov.2025

⁽¹⁷³⁾ Decision Etudes & Conseil and YOLE Group, *Competitiveness of the EU semiconductor manufacturing industry*, Nov.2025

⁽¹⁷⁴⁾ European Court of Auditors. (2025). *Special Report 12/2025 – The EU's strategy for microchips: Reasonable progress in its implementation, but the Chips Act is very unlikely to be sufficient to reach the overly ambitious Digital Decade target*.

⁽¹⁷⁵⁾ McKinsey & Company (2025). *Semiconductors have a big opportunity but barriers to scale remain*. February 2025.

⁽¹⁷⁶⁾ Decision Etudes & Conseil and YOLE Group, *Competitiveness of the EU semiconductor manufacturing industry*, Nov.2025

⁽¹⁷⁷⁾ Decision Etudes & Conseil and YOLE Group, *Competitiveness of the EU semiconductor manufacturing industry*, Nov.2025

- **Developments expected under BAU:** Europe pilots some **advanced-packaging lines** and niche OSAT activity, with new investments such as the planned SiliconBox advanced-packaging facility in Novara strengthening capabilities in specialised advanced packaging activities. However, **volume capacity remains concentrated in Asia**, which increasingly shapes system performance, cost and time-to-market.
- **Rationale:** The JRC (2025) ⁽¹⁷⁸⁾ shows Europe's strategic dependency on the US and Asia for advanced packaging and IC substrates. IFRI (2024) ⁽¹⁷⁹⁾ similarly highlights structural gaps in Europe's back-end capabilities. While Member State support has begun to include back-end initiatives such as Silicon Box in Italy and the (now-cancelled) Intel packaging project in Poland, the bulk of announced investments have been focused on front-end fabrication. Overall, the evidence indicates that Europe's structural gap in advanced packaging is likely to persist under BAU.
- **Implication for costs:** While firms offshore back-end processing because private production costs are lower in Asia, Europe's reliance on overseas packaging introduces additional logistics, coordination, and lead-time costs at the system level. As the Nexperia case illustrates, export restrictions imposed on back-end sites can have serious repercussions for European industry. These do not outweigh Asia's cost advantages for individual firms but nonetheless reduce Europe's ability to optimise time-to-market and design-manufacturing integration compared with a fully localised supply chain. (*Logical chain grounded in cited ecosystem gaps.*)

Materials, chemicals and gases

- **Developments expected under BAU:** Incremental **supplier diversification and recycling** reduce some risk premia, but EU remains **import-dependent** for many critical inputs with geopolitically concentrated supply. Continued investment in semiconductor manufacturing capacity is expected to encourage material suppliers to expand their presence.
- **Implication for costs:** continued exposure to **price volatility and border-compliance costs**, adding a thin but persistent premium to EU unit costs. (*Qualitative inference.*)

Key uncertainties

- **Energy price path:** faster convergence would narrow OPEX more quickly; renewed volatility would widen it. EU wholesale gas prices are currently 2.8 times higher than in the US and EU industrial electricity prices remain 137% higher ⁽¹⁸⁰⁾. These structural differences imply that even moderate volatility could significantly affect the EU cost base because energy is a major driver of fab operating expenditure.
- **Talent inflows:** stronger migration and training outcomes could shorten ramp times and reduce labour premia by the early 2030s. The EU still benefits from 1.1 million STEM graduates per year, more than the US (0.9 million), but growth in STEM output since 2015 has been only 11%, compared with 32% in the US and a near doubling in

⁽¹⁷⁸⁾ Bonnet, P., Ciani, A., Molnar, J., & Nardo, M. (2025). *EU's strengths and weaknesses in the global semiconductor sector* (JRC141323, EUR 40253). Luxembourg: Publications Office of the European Union. <https://doi.org/10.2760/6302476>

⁽¹⁷⁹⁾ Ebrahimi, A. (2024). *Groundbreaking chip sovereignty: Europe's strategic push in the semiconductor race*. Ifri Memos, Institut français des relations internationales (IFRI). ISBN 979-10-373-0874-0.

⁽¹⁸⁰⁾ Decision Etudes & Conseil and YOLE Group, *Competitiveness of the EU semiconductor manufacturing industry*, Nov.2025

China. This slower growth increases uncertainty regarding the EU's long-term talent advantage ⁽¹⁸¹⁾.

- **Global subsidies race:** escalation in the US or Asia could further widen gaps if EU support remains static. Japan, China, and the US have all announced larger semiconductor support packages than the EU Chips Act, in some cases several times higher ⁽¹⁸²⁾, which increases uncertainty about Europe's relative attractiveness for future capital-intensive projects.

1.5. Public budget effects

1.5.1. Establishing a starting point for BAU scenario

Public support for Europe's semiconductor ecosystem is already substantial, combining EU-level instruments, national state-aid schemes, and regional investment incentives.

To date, total announced public funding commitments under the EU Chips Act and related initiatives amount to approximately €32 billion, including both EU and national (without accounting for the IPCEI on Microelectronics and Communication Technologies).

At the EU level, the Chips Act also provides an indicative public envelope of additional EUR 11 billion over 2021-2030, financed mainly through:

- Horizon Europe and Digital Europe programmes for R&D and pilot-line development (Pillar I);
- First-of-a-Kind (FoaK) industrial-deployment support (Pillar II);
- Coordination, monitoring, and crisis-response measures (Pillar III).

At the national level, Member States have pledged the bulk of financial support through the IPCEI on Microelectronics and Communication Technologies and bespoke subsidy schemes. Germany, France, Italy, Ireland, and Austria together account for more than 80% of total national semiconductor funding.

In terms of fiscal revenues, the semiconductor sector remains modest but rising: it accounts for less than **0.3 % of EU GDP (≈ EUR 44 billion in gross value added)** and generates around **EUR 7.5 billion annually in tax receipts**, ⁽¹⁸³⁾ ⁽¹⁸⁴⁾ mainly through corporate taxation, labour contributions, and indirect taxes on high-value manufacturing ⁽¹⁸⁵⁾. The sector's potential for multiplier effects is high, yet most fiscal returns are geographically concentrated in host regions.

⁽¹⁸¹⁾Decision Etudes & Conseil and YOLE Group, *Competitiveness of the EU semiconductor manufacturing industry*, Nov.2025

⁽¹⁸²⁾Decision Etudes & Conseil and YOLE Group, *Competitiveness of the EU semiconductor manufacturing industry*, Nov.2025

⁽¹⁸³⁾ The effective fiscal yield (τ) used in this model represents the average share of gross value added accruing to public finances through corporate, labour, and indirect taxation. Based on OECD (2024) and JRC (2025) fiscal incidence data, and calibrated using semiconductor sector margins (Deloitte 2021; McKinsey 2025), τ is set at 16 % for 2023–2029 and 17 % for 2030–2035. This corresponds to approximately 9 % of GVA from payroll and social contributions, 4–5 % from corporate income tax, and 2–3 % from indirect levies.

⁽¹⁸⁴⁾ Here the 'semiconductor sector' refers to semiconductor manufacturers and not the broader semiconductor value chain.

⁽¹⁸⁵⁾ Bonnet, P., Ciani, A., Molnar, J., & Nardo, M. (2025). *EU's strengths and weaknesses in the global semiconductor sector* (EUR 40253 EN). Luxembourg: Publications Office of the European Union. <https://doi.org/10.2760/6302476>

Table 12. Starting parameters. *Source: Compiled by authors.*

Variable	Description	Value	Source
EU-27 GDP (2023)	Nominal GDP baseline	€14.6 trillion	Eurostat (AMECO)
Semiconductor sector GVA	0.3 % of GDP GVA=14,600×0.003=€43.8 billion.	≈ €44 billion	JRC (2025) ⁽¹⁸⁶⁾
Total public commitments (EU + MS)	Chips Act + IPCEI ME2 + national subsidies	€32 billion (2023–2030)	European Court of Auditors (2025), <i>Special Report 12/2025</i>
Effective fiscal yield (corporate, labour, indirect)	Average share of value added captured as fiscal revenue EUR 44 billion x 17% ≈ EUR 7.7 billion	16–17 %	JRC (2025) ⁽¹⁸⁷⁾ ; OECD Tax Revenue Database ⁽¹⁸⁸⁾
Sectoral output growth (BAU)	Compound annual growth rate of semiconductor GVA	6.9%	From the market size estimations
Discount rate	Real rate for long-term public investment appraisals	3 %	European Commission, Better Regulation Tool #61

1.5.2. Modelling the BAU scenario

Developments expected under BAU

Under a Business-As-Usual trajectory, the fiscal landscape of the semiconductor industry remains stable, with public-sector expenditure patterns following current commitments and limited expansion beyond projects already announced.

- **Public expenditure.** EU and national support continues through 2030 as existing fab and pilot-line projects are implemented. Expenditure peaks between 2026 and 2029, during the construction and ramp-up phase, and declines thereafter as facilities move to operational self-financing. No significant new EU-level budgetary envelopes are foreseen after 2030.
- **Public revenues.** As fabs reach full operation, corporate-tax revenues and social contributions rise gradually. Most fiscal gains accrue in Germany, France, Ireland, and Austria, where large-scale projects are located.
- **Net budgetary balance.** The overall fiscal balance of the Chips Act and related measures remains negative over most of the 2020s, reflecting the long gestation period of semiconductor investments. Only in the 2030s do cumulative public receipts begin to approach prior outlays, assuming stable global demand and high-capacity utilisation.

⁽¹⁸⁶⁾ Bonnet, P., Ciani, A., Molnar, J., & Nardo, M. (2025). *EU's strengths and weaknesses in the global semiconductor sector* (EUR 40253 EN). Luxembourg: Publications Office of the European Union. <https://doi.org/10.2760/6302476>

⁽¹⁸⁷⁾ Bonnet, P., Ciani, A., Molnar, J., & Nardo, M. (2025). *EU's strengths and weaknesses in the global semiconductor sector* (EUR 40253 EN). Luxembourg: Publications Office of the European Union. <https://doi.org/10.2760/6302476>

⁽¹⁸⁸⁾ *OECD Tax Revenue Statistics: Comparative Tables and Tax Revenue Database (Edition 2024)*. Paris: OECD Publishing. Available at <https://stats.oecd.org/Index.aspx?DataSetCode=REV>

Rationale and evidence base

The persistence of the current fiscal pattern is explained by structural and institutional factors:

1. **Capital intensity and sunk costs.** Semiconductor fabrication and equipment production are among the most capital-intensive industrial activities. Once established, these facilities create long-term lock-in and relocating them is economically prohibitive⁽¹⁸⁹⁾
2. **Fiscal-return dynamics.** Empirical modelling by Deloitte (2021)⁽¹⁹⁰⁾ suggests semiconductor multipliers of 1.2–1.5, meaning that for every euro of public investment, between EUR 1.20 and EUR 1.50 of additional economic output is generated. However, the realisation of these multipliers depends on sustained utilisation rates and global market stability.

Implications

Short-term (2025–2030)

- High fiscal outflows linked to construction subsidies and infrastructure provision.
- Limited immediate return in tax revenue due to investment write-offs and accelerated depreciation allowances.
- National budgets face concentration risks where large individual projects dominate expenditure⁽¹⁹¹⁾.

Medium-term (2030–2035)

- Operational fabs generate steady corporate-tax inflows and social contributions.
- Spillover effects (supplier VAT, construction, and services) strengthen local fiscal bases around centres of activity, where large scale front-end facilities reach maturity. Other clusters are more focused on R&D, design, and equipment, which yield smaller direct fiscal flows in the short to medium term.
- EU-level expenditure declines as pilot lines and competence centres move into self-sustaining models.

Long-term (post-2035 trend)

- Fiscal breakeven is achievable if facilities remain globally competitive and avoid obsolescence.
- Potential positive net position through continued exports and technology spillovers.
- Risk remains of fiscal asymmetry between Member States, as larger economies capture most revenue while smaller ones shoulder coordination or cohesion costs without direct returns.

⁽¹⁸⁹⁾ **McKinsey & Company. (2025).** *Semiconductors have a big opportunity, but barriers to scale remain.* New York: McKinsey Global Institute.

⁽¹⁹⁰⁾ Deloitte. (2021). *Measuring semiconductors' economic impact: How many jobs does the semiconductor industry create?* Deloitte Insights, September 2021.

⁽¹⁹¹⁾ European Court of Auditors. (2025). *Special Report 12/2025 – The EU's strategy for microchips: Reasonable progress in its implementation, but the Chips Act is very unlikely to be sufficient to reach the overly ambitious Digital Decade target.*

- High energy and water use in concentrated clusters may necessitate additional public investment in utilities and grid capacity, partly offsetting fiscal gains.
- Continued labour-market imbalances could require supplementary training budgets to address skills shortages, exerting additional fiscal pressure.

2. MODELLING SOCIAL IMPACTS

2.1. Jobs in the EU semiconductor industry

2.1.1. Establishing a starting point for BAU scenario

The semiconductor industry in Europe supports a substantial and growing labour force, concentrated in high-skill and high-value-added activities. In 2023, the European Chips Skills Academy estimated the **EU semiconductor workforce at approximately 382 000 jobs** across the full value chain, including around **263 000 in core design and production**. The top 25 employers account for roughly 40 % of this employment base ⁽¹⁹²⁾.

Employment is concentrated in a few regional clusters such as Saxony, Crolles-Grenoble, Eindhoven-Veldhoven, and Dresden, where manufacturing, equipment supply, and research organisations co-locate. These clusters benefit from strong productivity but face tight local labour markets.

Europe's chip workforce is highly skilled. Deloitte (2021) ⁽¹⁹³⁾ shows that semiconductor manufacturing employment is concentrated in engineers, technicians, and specialised trades, with wages more than double the private-sector average due to the high skill intensity and continuous-operation environment. ECSA (2024) ⁽¹⁹⁴⁾ and McKinsey (2024) ⁽¹⁹⁵⁾ confirm that Europe's semiconductor workforce is dominated by technical and engineering profiles requiring advanced qualifications, with wage premia and strong compliance and safety requirements consistent with global benchmarks. According to Deloitte (2021) ⁽¹⁹⁶⁾, semiconductor workers earn on average more than twice the private-sector wage and roughly 50% more than the manufacturing average in the US, reflecting the sector's high skill intensity and 24/7 operations. Although direct EU data is scarce, similar occupational structures suggest a substantial **wage premium in Europe as well, conservatively estimated at around 40–50 % above the manufacturing average**.

The quality of jobs is correspondingly high, with permanent contracts prevailing and considerable investment in training and safety. **Indirect and induced employment multipliers are significant:** U.S. evidence shows that each semiconductor job supports roughly 5–6 additional jobs in the wider economy (a total multiplier of about 6.7), according to Deloitte (2021) ⁽¹⁹⁷⁾ based on SIA/Oxford Economics modelling ⁽¹⁹⁸⁾. Given Europe's

⁽¹⁹²⁾ European Chips Skills Academy (ECSA). (2024). *European semiconductor skills strategy 2024*. Luxembourg: Publications Office of the EU.

⁽¹⁹³⁾ Deloitte. (2021). *Measuring semiconductors' economic impact*. Deloitte Insights.

⁽¹⁹⁴⁾ European Chips Skills Academy (ECSA). (2024). *European semiconductor skills strategy 2024*. Luxembourg: Publications Office of the EU.

⁽¹⁹⁵⁾ McKinsey & Company. (2024). *McKinsey on semiconductors: Creating value, pursuing innovation, and optimizing operations* (No. 9, March 2024). McKinsey & Company.

⁽¹⁹⁶⁾ Deloitte. (2021). *Measuring semiconductors' economic impact*. Deloitte Insights.

⁽¹⁹⁷⁾ Deloitte. (2021). *Measuring semiconductors' economic impact*. Deloitte Insights.

⁽¹⁹⁸⁾ <https://www.semiconductors.org/chipping-in-sia-jobs-report/>

dense supplier ecosystem, particularly in equipment and materials, the EU's multiplier effects are likely substantial, though not yet formally quantified.

The demand for skills already exceeds supply. McKinsey (2024) ⁽¹⁹⁹⁾ estimates a shortfall of over 100 000 engineers in Europe, similar in magnitude to the U.S. gap. Online vacancy data show that postings for semiconductor technical roles in the EU grew at over 75 % CAGR between 2018 and 2022, a clear signal of unmet demand ⁽²⁰⁰⁾. SEMI Europe (2024) ⁽²⁰¹⁾ similarly estimates that approximately 350 000 additional workers would be required by 2030 to meet the Chips Act objectives which is well above the current expansion pipeline. The Joint Research Centre (JRC, 2025) ⁽²⁰²⁾ lists skills shortages alongside fragmented markets and complex regulation as the main competitiveness constraints of the EU semiconductor ecosystem.

This demand projection assumes that only the announced increase in manufacturing capacity will take place over the course of this decade, and that no further significant investments in manufacturing capacity are made, except for organic expansions of current facilities.

Since job creation is proportional to the investment level, a further increase in public and private investment would result in a commensurate increase in high-quality and high-added value jobs, with the positive spill overs that this would have both from a social and an economic productivity perspective. This factor has not been quantitatively assessed in this social impacts model.

2.1.2. *Modelling the BAU scenario*

Developments expected under BAU

Under a business-as-usual trajectory, the EU semiconductor labour market expands gradually but remains constrained by structural skills shortages and uneven regional capacity. Between 2025 and 2030, the new fabs and expansions already under construction: **Intel Ireland, STMicroelectronics–GlobalFoundries Crolles, ESMC Dresden, Infineon Dresden, GlobalFoundries Dresden expansion, and the Catania SiC Campus**. They generate direct and indirect job growth as they ramp from construction to production. By 2030, the bulk of these facilities are expected to reach steady operation, with employment transitioning from construction trades to production technicians, maintenance engineers, and process specialists.

Beyond 2030, employment growth moderates as automation deepens and fabs reach maturity. Job creation increasingly depends on the localisation of **advanced packaging, compound-semiconductor production (SiC/GaN), and equipment manufacturing**, where Europe holds competitive strengths.

⁽¹⁹⁹⁾ McKinsey & Company. (2024). *McKinsey on semiconductors: Creating value, pursuing innovation, and optimizing operations* (No. 9, March 2024). McKinsey & Company.

⁽²⁰⁰⁾ McKinsey & Company. (2024). *McKinsey on semiconductors: Creating value, pursuing innovation, and optimizing operations* (No. 9, March 2024). McKinsey & Company.

⁽²⁰¹⁾ SEMI Europe. (2024). *Advocacy White Paper 2024*. Brussels: SEMI Europe.

⁽²⁰²⁾ European Commission, Joint Research Centre (JRC). (2025). *EU's strengths and weaknesses in the global semiconductor sector (JRC141323)*. Luxembourg: Publications Office of the EU.

Nevertheless, under BAU, the **skills constraint** remains binding: the pool of engineers and technicians grows too slowly to meet rising demand, even with national training and mobility programmes. ECSA (2024) ⁽²⁰³⁾ projects that, under current policies, the EU semiconductor sector will add around 156 000 new jobs by 2030 ($\approx 5\%$ CAGR) and experience about 271,000 cumulative openings when retirements and replacement needs are included. However, graduate inflows are projected to grow by only $\approx 1\%$ per year, implying a widening shortfall of around 16 800 unfilled technical roles by 2030. Unless the pace of education and reskilling accelerates markedly, the projected headcount increases in announced projects will not translate one-to-one into realised employment.

Rationale and evidence base

- **Industrial context:** McKinsey (2024) ⁽²⁰⁴⁾ projects about **USD 1 trillion in global fab investments by 2030**, implying **intense competition for qualified talent**. Europe captures a modest share of these projects, insufficient to transform its labour dynamics rapidly.
- **Policy context:** The Chips Act provides support for competence centres, skills initiatives, pilot lines and first-industrial deployment, but these initiatives are only now being implemented. It is therefore too early to assess their full impact on the talent gap, although current evidence suggests that substantial shortages will persist in the near term. The **European Court of Auditors (2025)** ⁽²⁰⁵⁾ observes that current public support levels and timelines “fall short of transforming EU market share quickly”.
- **Skills evidence:** ECSA (2024) ⁽²⁰⁶⁾ and SEMI Europe (2024) ⁽²⁰⁷⁾ highlight that the largest shortages will occur in **technicians, process engineers, and software/automation specialists**, reflecting the shift toward **smart manufacturing, advanced materials, and digital design integration**.
- **Geographical concentration:** Existing clusters (Dresden, Grenoble, Eindhoven, Catania, Southern Austria) attract investment and provide higher hiring efficiency, but new greenfield sites face slower ramp-up due to limited local talent pools which is highlighted in McKinsey’s (2024) ⁽²⁰⁸⁾ analysis.

Implications for employment and skills

- **Job creation:** The EU semiconductor workforce is expected to continue expanding through 2030 as ongoing investments reach full capacity. By 2035, employment growth slows but remains positive, driven by ecosystem expansion in equipment,

⁽²⁰³⁾ European Chips Skills Academy (ECSA). (2024). *European semiconductor skills strategy 2024*. Luxembourg: Publications Office of the EU.

⁽²⁰⁴⁾ McKinsey & Company. (2024). *McKinsey on semiconductors: Creating value, pursuing innovation, and optimizing operations* (No. 9, March 2024). McKinsey & Company.

⁽²⁰⁵⁾ European Court of Auditors. (2025). *Special Report 12/2025 – The EU’s strategy for microchips: Reasonable progress in its implementation, but the Chips Act is very unlikely to be sufficient to reach the overly ambitious Digital Decade target*. Luxembourg: Publications Office of the European Union.

⁽²⁰⁶⁾ European Chips Skills Academy (ECSA). (2024). *European semiconductor skills strategy 2024*. Luxembourg: Publications Office of the EU.

⁽²⁰⁷⁾ SEMI Europe. (2024). *Advocacy White Paper 2024*. Brussels: SEMI Europe.

⁽²⁰⁸⁾ McKinsey & Company. (2024). *McKinsey on semiconductors: Creating value, pursuing innovation, and optimizing operations* (No. 9, March 2024). McKinsey & Company.

materials, and specialised manufacturing. However, realised employment depends on mitigating the skills bottleneck.

- **Job quality:** Semiconductor jobs remain among the most stable and best-paid in manufacturing. High skill intensity and safety standards support good working conditions and strong career progression prospects.
- **Skills demand:** The composition of employment shifts toward **process automation, embedded software, AI/ML-assisted design, and compound-materials engineering**. Without significant training acceleration, the EU risks persistent reliance on third-country experts and cross-border mobility.
- **Systemic risk:** Labour shortages may become a structural drag on the effectiveness of Chips Act investments, limiting capacity utilisation and slowing Europe's technology-leadership ambitions.

2.2. SME/start-up ecosystem in the EU semiconductor industry

2.2.1. Establishing a starting point for BAU scenario

Small and Medium-sized Enterprises (SMEs) in the EU semiconductor industry face specific conditions and challenges. Historically, information on smaller players has been limited, providing only a partial picture of their involvement compared to larger companies ⁽²⁰⁹⁾.

One significant weakness in the EU semiconductor industry is the need for stronger cooperation between large companies and innovative SMEs, as SMEs currently struggle to gain attention ⁽²¹⁰⁾. This is particularly evident in the design of advanced processors, despite the EU having a thriving ecosystem of startups in this area ⁽²¹¹⁾. Large firms also tend to have more diversified expenditure on inputs across geographical areas than SMEs ⁽²¹²⁾.

To address these challenges, the Chips Act includes initiatives aimed at supporting SMEs and startups. These include a design platform designed to lower barriers to entry for chip design. Additionally, the Chips Fund offers various equity and debt solutions for SMEs and startups. Competence Centres are also being established in member states to facilitate access to the virtual design platform and pilot lines. The opening of these pilot lines is intended to provide SMEs and startups with easier and faster access to foundry services for both novel and older technologies.

SME and start-up role in the value chain: Europe's semiconductor ecosystem, in terms of number of companies, is dominated by small and medium-sized enterprises, which account for roughly 69% of all firms across the value chain.

The EU hosts a large number of small and mid-sized champions in equipment, specialty materials, sensors and MEMS, power electronics, and optoelectronics, where innovation and domain expertise matter more than scale. However, it has far fewer successful scale-ups in

⁽²⁰⁹⁾ Rosati, N., Bonnet, P., Ciani, A., Duch Brown, N., Miguez, S., & Zaurino, E. (2023). *The EC consultation on the semiconductors' value chain* (JRC133892, EUR 31585 EN).

⁽²¹⁰⁾ DECISION Études & Conseil. (2024). *Economic analysis of the EU and global chips ecosystem*. European Commission, Directorate-General for Communications Networks, Content and Technology (DG CNECT).

⁽²¹¹⁾ DECISION Études & Conseil. (2024). *Economic analysis of the EU and global chips ecosystem*. European Commission, Directorate-General for Communications Networks, Content and Technology (DG CNECT).

⁽²¹²⁾ Rosati, N., Bonnet, P., Ciani, A., Duch Brown, N., Miguez, S., & Zaurino, E. (2023). *The EC consultation on the semiconductors' value chain* (JRC133892, EUR 31585 EN).

fabless design and virtually no globally competitive EDA providers beyond Siemens EDA (the result of the acquisition of US-based Mentor Graphics by Siemens AG in 2017). This structural pattern mirrors Europe's technological strengths in optoelectronics, MEMS, and power semiconductors, but also its relative weakness in advanced logic design and digital system-on-chip innovation, where large U.S. and Asian firms dominate⁽²¹³⁾.

Access to finance and scale-up pathways: Persistent late-stage funding gaps constrain EU chip start-ups and fabless SMEs from moving beyond prototypes to growth manufacturing. Although policy instruments such as the Chips Fund and InvestEU exist on paper, Interface (2024)⁽²¹⁴⁾, IFRI (2024)⁽²¹⁵⁾, and JRC (2025)⁽²¹⁶⁾ note that investment capacity and deal flow remain limited compared with U.S. and Asian ecosystems. McKinsey (2024)⁽²¹⁷⁾ similarly highlights Europe's structural deficit in late-stage venture capital and corporate investment.

Access to shared infrastructure and tools: The Chips Act introduced a Design Platform (DP), a network of competence centres, pilot lines, and a Chips Fund precisely to lower barriers for SMEs and start-ups. These measures are designed to ease access to EDA/IP, multi-project wafers (MPWs), and expert support, and to blend equity/debt for young firms. Implementation is underway but still maturing; practical access and throughput for SMEs varies by Member State.

Administrative burden and access to support: Implementation of the Chips Act spans several overlapping instruments: the Chips Joint Undertaking, the Chips Fund, the Design Platform, national state-aid schemes under Pillar II and IPCEI ME2, as well as Horizon Europe and InvestEU windows. Each of them has a separate application, eligibility, and reporting requirements. For smaller firms, this multi-layered structure results in high fixed compliance costs and lengthy approval timelines. The ECA (2025)⁽²¹⁸⁾ and Interface (2024)⁽²¹⁹⁾ note that the absence of a single-entry point and duplication between EU and national levels increase transaction costs, while IFRI (2024)⁽²²⁰⁾ and JRC (2025)⁽²²¹⁾ highlight uneven administrative capacity across Member States, especially in State aid management. SMEs active in cross-border or pilot projects are particularly affected, as differing national procedures often require multiple notifications and audits. Large firms can absorb these costs through dedicated compliance resources, but smaller companies frequently withdraw or forgo

⁽²¹³⁾ Survey data collected by DG CNECT from Member States for Chips Act Pillar III mapping and elaborated by the JRC.

⁽²¹⁴⁾ Kleinhans, J.-P. (2024), *The missing strategy in Europe's chip ambitions: Member States must drive the next steps*, Interface, July 2024.

⁽²¹⁵⁾ Ebrahimi, A. (2024). *Groundbreaking chip sovereignty: Europe's strategic push in the semiconductor race*. Ifri Memos, Institut français des relations internationales (IFRI). ISBN 979-10-373-0874-0.

⁽²¹⁶⁾ Bonnet, P., Ciani, A., Molnar, J., & Nardo, M. (2025). *EU's strengths and weaknesses in the global semiconductor sector* (JRC141323, EUR 40253). Luxembourg: Publications Office of the European Union. <https://doi.org/10.2760/6302476>

⁽²¹⁷⁾ McKinsey & Company (2021), *McKinsey on Semiconductors: Creating value, pursuing innovation, and optimising operations*.

⁽²¹⁸⁾ European Court of Auditors. (2025). *Special Report 12/2025 – The EU's strategy for microchips: Reasonable progress in its implementation, but the Chips Act is very unlikely to be sufficient to reach the overly ambitious Digital Decade target*. Luxembourg: Publications Office of the European Union.

⁽²¹⁹⁾ Kleinhans, J.-P. (2024), *The missing strategy in Europe's chip ambitions: Member States must drive the next steps*, Interface, July 2024.

⁽²²⁰⁾ Ebrahimi, A. (2024). *Groundbreaking chip sovereignty: Europe's strategic push in the semiconductor race*. Ifri Memos, Institut français des relations internationales (IFRI). ISBN 979-10-373-0874-0.

⁽²²¹⁾ Bonnet, P., Ciani, A., Molnar, J., & Nardo, M. (2025). *EU's strengths and weaknesses in the global semiconductor sector* (JRC141323, EUR 40253). Luxembourg: Publications Office of the European Union. <https://doi.org/10.2760/6302476>

participation. As a result, SMEs face slower access to support and lower participation rates in major semiconductor programmes.

2.2.2. Modelling the BAU scenario

2.2.2.1 Access to finance and scale-up

- **Developments expected under BAU:** Gradual improvement in seed and Series A availability is expected via the Chips Fund, the Design Platform, and InvestEU windows. However, little progress is anticipated at late-stage growth and expansion rounds, as these financing gaps stem from broader structural weaknesses in the EU capital market. These issues go beyond the scope of sector-specific instruments and cannot be resolved without deeper systemic reforms such as a functioning Capital Markets Union.
- **Rationale:** Interface (2024) ⁽²²²⁾ notes that while the Chips Act's instruments such as pilot lines, the competence centres and the Chips Fund formally exist, their strategic follow-through and implementation capacity remain limited. Member States differ markedly in how they execute and resource these instruments, creating uneven access for start-ups and SMEs. As a result, the transition from prototype development to commercial manufacturing remains constrained, and the pipeline from pilot to product is only partially functional under current conditions.
- **Implications for SMEs:** By 2028, many SMEs gain first access to the Chips Act's Design Platform and competence centres, improving their ability to design and prototype new chips. However, access to large-scale follow-on financing for industrialisation and scaling remain scarce, leaving promising fabless firms unable to design at leading edge nodes or move from prototype runs to market-ready production. Some relocate intellectual property or exit early to attract non-EU investment. The critical transition between Technology Readiness Levels 6 and 8 (the “valley of death”) therefore remains a high-risk stage under BAU conditions, and this challenge is unlikely to be fully resolved even under alternative scenarios. The underlying barriers are structural – notably the shortage of late-stage capital, limited domestic demand-pull, and Europe's fragmented financing landscape – and extend beyond what sectoral instruments such as the Chips Act can realistically address.

2.2.2.2 Access to infrastructure and tools (DP, competence centres, pilot lines)

- **Developments expected under BAU:** Access to shared design and prototyping infrastructure improves gradually as the Virtual Design Platform, competence centres, and pilot lines reach maturity. SMEs benefit from expanded multi-project wafer services and more predictable conditions for EDA tools, alongside financial support, which lower entry barriers and accelerate prototyping. Bottlenecks, however, persist in securing affordable access to design tools, navigating heterogeneous access conditions across Member States, and obtaining timely technical assistance, reflecting broader coordination and capacity challenges rather than specific technical constraints.

⁽²²²⁾Kleinhans, J.-P. (2024), *The missing strategy in Europe's chip ambitions: Member States must drive the next steps*, Interface, July 2024.

- **Rationale:** Pillar I of the Chips Act was designed to also ease SME entry into semiconductor innovation, but practical capacity and coordination are still catching up, as noted by Interface (2024) ⁽²²³⁾ and the ECA (2025) ⁽²²⁴⁾.
- **Implications for SMEs:** Entry costs for first-time tape-outs and lab prototyping decline, improving time-to-prototype and customer validation. Yet cross-country disparities persist, and scaling beyond prototype remains constrained by dependence on non-EU foundries and OSATs.

Overall, by 2035, it is expected that the Design Platform, competence centres, and pilot lines will have expanded and become accessible, lowering entry barriers and improving prototyping speed for SMEs. Some regional clusters strengthen around Europe's established niches in equipment, materials, and power electronics. Yet core structural constraints persist and the late-stage financing gap remains wide.

2.3. R&D&I leadership in the EU semiconductor industry

Competitive advantage can be achieved through cost (and hence price) or the innovation, sophistication and quality of chips. As discussed in Section 1.3 of this annex, the EU holds a strong market position in the design and manufacture of analogue chips, radio-frequency (RF) components, sensors and MEMS, power semiconductors, microcontrollers, and silicon photonics ⁽²²⁵⁾, ⁽²²⁶⁾. European suppliers are global leaders in embedded systems serving strategic industrial sectors such as automotive, robotics, energy, healthcare, aerospace, defence, and telecommunications infrastructures ⁽²²⁷⁾, ⁽²²⁸⁾, ⁽²²⁹⁾. European firms such as STMicroelectronics, Infineon, Robert Bosch, and NXP are recognised global leaders in power electronics and sensors, particularly for heavy industrial and automotive uses ⁽²³⁰⁾, ⁽²³¹⁾.

The EU is also home to world-class research and innovation centres, including IMEC in Belgium, CEA-Leti in France, and Fraunhofer in Germany, which have contributed to major technological breakthroughs in microelectronics ⁽²³²⁾, ⁽²³³⁾, ⁽²³⁴⁾.

⁽²²³⁾ Kleinhans, J.-P. (2024), *The missing strategy in Europe's chip ambitions: Member States must drive the next steps*, Interface, July 2024.

⁽²²⁴⁾ European Court of Auditors. (2025). *Special Report 12/2025 – The EU's strategy for microchips: Reasonable progress in its implementation, but the Chips Act is very unlikely to be sufficient to reach the overly ambitious Digital Decade target*.

⁽²²⁵⁾ DECISION Études & Conseil. (2024). *Economic analysis of the EU and global chips ecosystem*. European Commission, Directorate-General for Communications Networks, Content and Technology (DG CNECT).

⁽²²⁶⁾ Cerutti, I., Nardo, M., et al. (2024). *Applying the SCAN methodology to the Semiconductor Supply Chain*. JRC Technical Report, JRC141323. Publications Office of the European Union

⁽²²⁷⁾ European Semiconductor Industry Association. (2025). *Position paper on EU Chips Act 2*. Brussels: ESIA.

⁽²²⁸⁾ DECISION Études & Conseil. (2024). *Economic analysis of the EU and global chips ecosystem*. European Commission, Directorate-General for Communications Networks, Content and Technology (DG CNECT).

⁽²²⁹⁾ Cerutti, I., Nardo, M., et al. (2024). *Applying the SCAN methodology to the Semiconductor Supply Chain*. JRC Technical Report, JRC141323. Publications Office of the European Union

⁽²³⁰⁾ Ebrahimi, A. (2024). *Groundbreaking chip sovereignty: Europe's strategic push in the semiconductor race*. Ifri Memos, Institut français des relations internationales (IFRI). ISBN 979-10-373-0874-0.

⁽²³¹⁾ Cerutti, Isabella & Nardo, Michela (2023). *Semiconductors in the EU: State of play, future trends and vulnerabilities of the semiconductor supply chain*. JRC Technical Report, JRC133850.

⁽²³²⁾ DECISION Études & Conseil. (2024). *Economic analysis of the EU and global chips ecosystem*. European Commission, Directorate-General for Communications Networks, Content and Technology (DG CNECT).

⁽²³³⁾ Cerutti, Isabella & Nardo, Michela (2023). *Semiconductors in the EU: State of play, future trends and vulnerabilities of the semiconductor supply chain*. JRC Technical Report, JRC133850.

⁽²³⁴⁾ Cerutti, I., Nardo, M., et al. (2024). *Applying the SCAN methodology to the Semiconductor Supply Chain*. JRC Technical Report, JRC141323. Publications Office of the European Union

Within the supply chain, the EU possesses a clear competitive advantage in manufacturing equipment, led by ASML in the Netherlands, the world's sole provider of extreme ultraviolet (EUV) lithography tools and with an 88% market share in the broader lithography market in 2022 ⁽²³⁵⁾, ⁽²³⁶⁾. Germany's Siemens also plays a critical role in electronic design software ⁽²³⁷⁾.

However, despite these strengths, the EU remains absent from the technological frontier of semiconductor innovation. It plays only a minor role in global chip design, accounting for about 9% of the global market ⁽²³⁸⁾, and lacks production capacity for the leading edge and advanced nodes (below 16 nm) ⁽²³⁹⁾, which are overwhelmingly concentrated in Taiwan and South Korea, with a smaller share in the US ⁽²⁴⁰⁾, ⁽²⁴¹⁾. Most EU production focuses on mature nodes (40 nm and above), serving industrial and automotive demand rather than leading-edge computing applications ⁽²⁴²⁾. Europe also lacks large-scale pure-play foundries and depends on other regions for advanced-node manufacturing ⁽²⁴³⁾. In addition, Europe's strong public research base does not consistently translate into industrial leadership. Although organisations such as IMEC, CEA-Leti and Fraunhofer develop world-class technologies, commercialisation channels and scaling partnerships remain limited and many innovations pioneered in European pilot lines are industrialised in non-EU foundries. While the EU benefits from a growing base of innovative fabless startups, collaboration between large incumbents and smaller firms remains limited ⁽²⁴⁴⁾. Finally, structural barriers, including fragmented markets, and complex regulatory environments, further constrain the translation of research into competitive industrial capacity. As a result, the EU's semiconductor ecosystem shows high technological sophistication but does not convert its research excellence into global leadership in advanced chip design and manufacturing ⁽²⁴⁵⁾, ⁽²⁴⁶⁾.

⁽²³⁵⁾ DECISION Études & Conseil. (2024). *Economic analysis of the EU and global chips ecosystem*. European Commission, Directorate-General for Communications Networks, Content and Technology (DG CNECT).

⁽²³⁶⁾ Ebrahimi, A. (2024). *Groundbreaking chip sovereignty: Europe's strategic push in the semiconductor race*. Ifri Memos, Institut français des relations internationales (IFRI). ISBN 979-10-373-0874-0.

⁽²³⁷⁾ Ebrahimi, A. (2024). *Groundbreaking chip sovereignty: Europe's strategic push in the semiconductor race*. Ifri Memos, Institut français des relations internationales (IFRI). ISBN 979-10-373-0874-0.

⁽²³⁸⁾ Ebrahimi, A. (2024). *Groundbreaking chip sovereignty: Europe's strategic push in the semiconductor race*. Ifri Memos, Institut français des relations internationales (IFRI). ISBN 979-10-373-0874-0.

⁽²³⁹⁾ IDC. (2025). *Semiconductors D3: Second interim study report (Version 3.0)*. Prepared for the European Commission.

⁽²⁴⁰⁾ Ebrahimi, A. (2024). *Groundbreaking chip sovereignty: Europe's strategic push in the semiconductor race*. Ifri Memos, Institut français des relations internationales (IFRI). ISBN 979-10-373-0874-0.

⁽²⁴¹⁾ DECISION Études & Conseil. (2024). *Economic analysis of the EU and global chips ecosystem*. European Commission, Directorate-General for Communications Networks, Content and Technology (DG CNECT).

⁽²⁴²⁾ DECISION Études & Conseil. (2024). *Economic analysis of the EU and global chips ecosystem*. European Commission, Directorate-General for Communications Networks, Content and Technology (DG CNECT).

⁽²⁴³⁾ DECISION Études & Conseil. (2024). *Economic analysis of the EU and global chips ecosystem*. European Commission, Directorate-General for Communications Networks, Content and Technology (DG CNECT).

⁽²⁴⁴⁾ DECISION Études & Conseil. (2024). *Economic analysis of the EU and global chips ecosystem*. European Commission, Directorate-General for Communications Networks, Content and Technology (DG CNECT).

⁽²⁴⁵⁾ Cerutti, Isabella & Nardo, Michela (2023). *Semiconductors in the EU: State of play, future trends and vulnerabilities of the semiconductor supply chain*. JRC Technical Report, JRC133850.

⁽²⁴⁶⁾ Bonnet, P., Ciani, A., Molnar, J., & Nardo, M. (2025). *EU's strengths and weaknesses in the global semiconductor sector* (JRC141323, EUR 40253). Luxembourg: Publications Office of the European Union. <https://doi.org/10.2760/6302476>

2.3.1. Establishing a starting point for BAU scenario

Quantitative indicators of R&D and innovation effort

The EU semiconductor ecosystem demonstrates high R&D intensity but remains structurally constrained in scale, market penetration, advanced-node chip design and high-volume manufacturing, despite strong European leadership in process research and enabling technologies such as EUV lithography. The table below summarises the key indicators that define the 2023 starting point, benchmarked against major global competitors.

Table 13. Starting point for R&D and innovation BAU. *Source: Compiled by the authors.*

Indicator	Indicative EU figure (2023)	Benchmark comparison	Reference and justification
Effectiveness of technology transfer (lab-to-fab conversion of research outputs)	Low to moderate; a significant proportion of pilot-line technologies are industrialised outside the EU	Higher conversion rates in the US, Taiwan, and South Korea	JRC (2025) ⁽²⁴⁷⁾ highlights fragmentation between research and manufacturing; ECA (2025) ⁽²⁴⁸⁾ notes that technology developed in EU pilot lines is frequently scaled abroad; IFRI (2024) ⁽²⁴⁹⁾ and BCG & SIA (2024) ⁽²⁵⁰⁾ underline the absence of large-scale EU foundries capable of absorbing advanced research.
R&D intensity (R&D expenditure as % of semiconductor revenue)	≈ 22 % (± 2 pp)	Global average ~22 % (U.S. 23 %; Asia 21 %)	McKinsey & Company (2025) ⁽²⁵¹⁾ : “Semiconductor industry averages about 22 % of revenue in R&D.” Deloitte (2021) ⁽²⁵²⁾ : “Typically reinvest 20–25 % of revenue in R&D.” Company reports: ASML 15 %, Infineon 14 %, ST 13 %, NXP 16 %. Adjusted upward for Europe’s strong public-research component gives ≈ 22 %.
Share of global	≈ 9–10 % (± 2 pp)	U.S. ≈ 50 %;	McKinsey (2024) ⁽²⁵³⁾ : Europe’s

⁽²⁴⁷⁾ European Commission, Joint Research Centre (JRC). (2025). *EU’s strengths and weaknesses in the global semiconductor sector (JRC141323)*. Luxembourg: Publications Office of the European Union.

⁽²⁴⁸⁾ European Court of Auditors. (2025). *Special Report 12/2025 – The EU’s strategy for microchips: Reasonable progress in its implementation, but the Chips Act is very unlikely to be sufficient to reach the overly ambitious Digital Decade target*.

⁽²⁴⁹⁾ Ebrahimi, A. (2024). *Groundbreaking chip sovereignty: Europe’s strategic push in the semiconductor race*. Ifri Memos, Institut français des relations internationales (IFRI). ISBN 979-10-373-0874-0.

⁽²⁵⁰⁾ **Boston Consulting Group (BCG) & Semiconductor Industry Association (SIA)**. (May 2024). *Emerging Resilience in the Semiconductor Supply Chain*.

⁽²⁵¹⁾ **McKinsey & Company (2025)**. *Semiconductors have a big opportunity but barriers to scale remain*. February 2025.

⁽²⁵²⁾ **Deloitte**. (2021). *Measuring semiconductors’ economic impact*. Deloitte Insights.

semiconductor R&D spending		Asia $\approx$ 35 %	revenue share $\approx$ 10 % of global industry $\rightarrow$ assumed proportional R&D share. JRC (2025) ⁽²⁵⁴⁾ reports EU accounts for roughly 10% of semiconductor value-added. Given that semiconductor R&D intensity is relatively constant worldwide (around 20–25 % of revenue; McKinsey 2025; Deloitte 2021), it is reasonable to assume that regional R&D spending scales proportionally with regional industry revenue. Accordingly, Europe’s approximate 10% share of global semiconductor revenue implies a similar order of magnitude for its share of global R&D expenditure ($\approx$ 9–10 %).
Share of global chip-design market	$\approx$ 9 %	U.S. $\approx$ 60 %; China $\approx$ 16 %; Taiwan $\approx$ 8 %	JRC (2025) ⁽²⁵⁵⁾: EU $\approx$ 9 % of global chip-design revenue (including European IDMs). BCG & SIA (2024) ⁽²⁵⁶⁾: “The US retains > 60 % of global chip-design.”
Share of global advanced-node patents (< 16 nm)	< 5 %	Dominated by U.S., Taiwan, Korea	JRC (2025), IFRI (2024), and BCG–SIA (2024) show that the EU has limited domestic production capacity at <16 nm except for the Intel manufacturing in Leixlip, Ireland. Advanced-node process innovation is concentrated in Taiwan (TSMC), South Korea (Samsung) and the US (Intel and leading U.S. design–EDA ecosystems), though IMEC and CEA-Leti are innovating a lot for manufacturing below 2nm and FD-SOI below 7nm. Outside of the

⁽²⁵³⁾ McKinsey & Company. (2024). *McKinsey on Semiconductors: Creating value, pursuing innovation, and optimizing operations*. McKinsey & Company.

⁽²⁵⁴⁾ European Commission, Joint Research Centre (JRC). (2025). *EU’s strengths and weaknesses in the global semiconductor sector (JRC141323)*. Luxembourg: Publications Office of the European Union.

⁽²⁵⁵⁾ European Commission, Joint Research Centre (JRC). (2025). *EU’s strengths and weaknesses in the global semiconductor sector (JRC141323)*. Luxembourg: Publications Office of the European Union.

⁽²⁵⁶⁾ **Boston Consulting Group (BCG) & Semiconductor Industry Association (SIA)**. (May 2024). *Emerging Resilience in the Semiconductor Supply Chain*.

			patents hold by RTOs, European patenting strength lies in equipment, materials, lithography and photonics rather than advanced CMOS logic. Given the strong correlation between leading-edge manufacturing and process-technology patenting, Europe's share of <16 nm patents is therefore inferred to be very small, typically estimated at below 5 %.
Top 10 EDA/design-tool vendors headquartered in EU	1 (Siemens EDA)	3 in U.S.	IFRI (2024) ⁽²⁵⁷⁾ : lists Siemens EDA as Europe's sole global-tier EDA provider.
Public R&D funding for microelectronics (EU + MS)	≈ EUR 3–4 billion annually	U.S./Asia ≈ EUR 7–15 billion	ECA (2025) ⁽²⁵⁸⁾ : notes Chips Act public component “covers a small fraction” of global subsidies; combined EU-level and national programmes ≈ EUR 43 billion over 2021–2030, this translates to an annual average of roughly EUR 4 billion per year.

2.3.2. Modelling the BAU scenario

In the BAU model, we explicitly assume that Europe's strong research base does not translate proportionally into industrial capacity, due to persistent lab-to-fab bottlenecks, limited domestic absorption capacity, and structural fragmentation. As a result, R&D inputs increase, but technology-transfer outcomes remain modest, in line with the evidence from JRC (2025) ⁽²⁵⁹⁾, ECA (2025) ⁽²⁶⁰⁾, IFRI (2024) ⁽²⁶¹⁾, and BCG–SIA (2024) ⁽²⁶²⁾.

Technology transfer and industrial scaling (lab-to-fab)

- **Developments expected under BAU:** Under the business-as-usual scenario, Europe's pilot lines continue to generate high-quality scientific outputs in advanced logic, power electronics, compound semiconductors, photonics, and materials engineering. However, the rate of industrial uptake remains limited. Most European IDMs operate at mature nodes and demonstrate only partial incentives to integrate new process

⁽²⁵⁷⁾ Ebrahimi, A. (2024). *Groundbreaking chip sovereignty: Europe's strategic push in the semiconductor race*. Ifri Memos, Institut français des relations internationales (IFRI). ISBN 979-10-373-0874-0.

⁽²⁵⁸⁾ European Court of Auditors. (2025). *Special Report 12/2025 – The EU's strategy for microchips: Reasonable progress in its implementation, but the Chips Act is very unlikely to be sufficient to reach the overly ambitious Digital Decade target*.

⁽²⁵⁹⁾ European Commission, Joint Research Centre (JRC). (2025). *EU's strengths and weaknesses in the global semiconductor sector (JRC141323)*. Luxembourg: Publications Office of the European Union.

⁽²⁶⁰⁾ European Court of Auditors. (2025). *Special Report 12/2025 – The EU's strategy for microchips: Reasonable progress in its implementation, but the Chips Act is very unlikely to be sufficient to reach the overly ambitious Digital Decade target*.

⁽²⁶¹⁾ Ebrahimi, A. (2024). *Groundbreaking chip sovereignty: Europe's strategic push in the semiconductor race*. Ifri Memos, Institut français des relations internationales (IFRI). ISBN 979-10-373-0874-0.

⁽²⁶²⁾ **Boston Consulting Group (BCG) & Semiconductor Industry Association (SIA)**. (May 2024). *Emerging Resilience in the Semiconductor Supply Chain*.

modules that require costly requalification. The EU's limited presence in advanced-node manufacturing further restricts opportunities for domestic scaling. Consequently, although pilot lines strengthen Europe's technological capabilities, a significant share of innovations is expected to be commercialised in non-EU foundries where larger design ecosystems and high-volume manufacturing platforms are available.

- **Rationale:** Evidence from the JRC (2025) ⁽²⁶³⁾, IFRI (2024) ⁽²⁶⁴⁾, and BCG–SIA (2024) ⁽²⁶⁵⁾ shows that the EU's innovation pipeline is weakened by structural fragmentation between research organisations, early-stage firms, and large industrial players. The ECA (2025) ⁽²⁶⁶⁾ stresses that technologies developed within EU-funded pilot lines are often industrialised abroad, underscoring limited domestic absorption capacity. In contrast, the US, Taiwan, and South Korea benefit from dense co-development ecosystems in which research institutes, EDA suppliers, design houses, and advanced foundries jointly validate and scale innovations. Without a comparable industrial base, Europe's capability to transform research excellence into competitive market positions remains constrained.
- **Implication for competitiveness:** Under BAU, Europe's research institutions consolidate their position as global leaders in semiconductor science, but the Union makes only modest progress in commercialising these advances domestically. Weak lab-to-fab scaling reduces the economic return on public R&D investment, slows the emergence of European design champions, and allows competing regions to capture value added from technologies that originate in Europe. As a result, Europe's innovation strengths translate into incremental rather than structural competitiveness gains in high-growth semiconductor segments.

R&D intensity (R&D as % of semiconductor revenue)

- **Developments expected under BAU:** The European semiconductor ecosystem maintains a structurally high R&D intensity. Newly built fabs in Ireland, France, Germany, and Italy reinforce the applied-research interface between equipment suppliers, materials firms, and integrated device manufacturers. Pilot lines increase Europe's leadership in the development of process technology. However, these additions mainly broaden production rather than altering the R&D-to-revenue ratio, which remains close to the global average.
- **Rationale:** McKinsey (2025) ⁽²⁶⁷⁾ and Deloitte (2021) ⁽²⁶⁸⁾ find that R&D intensity in semiconductors is remarkably uniform worldwide at about one-fifth of revenue. Company data for ASML, Infineon, STMicroelectronics, and NXP confirm that European firms already operate within this band. Neither new subsidies nor new fabs are expected to change this structural parameter.
- **Implication for competitiveness:** The EU sustains a world-class research effort and strong public-private science base, but high R&D intensity alone does not guarantee

⁽²⁶³⁾ European Commission, Joint Research Centre (JRC). (2025). *EU's strengths and weaknesses in the global semiconductor sector (JRC141323)*. Luxembourg: Publications Office of the European Union.

⁽²⁶⁴⁾ Ebrahimi, A. (2024). *Groundbreaking chip sovereignty: Europe's strategic push in the semiconductor race*. Ifri Memos, Institut français des relations internationales (IFRI). ISBN 979-10-373-0874-0.

⁽²⁶⁵⁾ Boston Consulting Group (BCG) & Semiconductor Industry Association (SIA). (May 2024). *Emerging Resilience in the Semiconductor Supply Chain*.

⁽²⁶⁶⁾ European Court of Auditors. (2025). *Special Report 12/2025 – The EU's strategy for microchips: Reasonable progress in its implementation, but the Chips Act is very unlikely to be sufficient to reach the overly ambitious Digital Decade target*.

⁽²⁶⁷⁾ McKinsey & Company (2025). *Semiconductors have a big opportunity but barriers to scale remain*. February 2025.

⁽²⁶⁸⁾ Deloitte. (2021). *Measuring semiconductors' economic impact*. Deloitte Insights.

technological leadership. Without greater design scale or faster commercialisation, high R&D effort continues to yield incremental rather than transformational advantages.

Share of global semiconductor R&D spending

- **Developments expected under BAU:** Absolute R&D spending in Europe rises as new fabs and pilot lines come online, yet the EU's global share changes little. Growth elsewhere, particularly in Asia and the US, keeps relative positions broadly stable through 2035. European technology developed in the pilot lines is industrialised elsewhere.
- **Rationale:** Global R&D intensity remains constant, meaning regional spending scales with output. Europe's announced fabs expand capacity but not enough to alter the global distribution. The ECA (2025) ⁽²⁶⁹⁾ and JRC (2025) ⁽²⁷⁰⁾ both note that current investment levels are modest compared with the subsidy waves in Asia and North America.
- **Implication for competitiveness:** Europe strengthens its applied-research network and process-engineering skills, but its overall share of global semiconductor R&D remains modest. Without a wider industrial base, Europe's innovation influence grows only gradually.

Share of global chip-design market

- **Developments expected under BAU:** The EU's design activity grows within its established strengths such as embedded systems, automotive, industrial control, and RF/power electronics. New FD-SOI and automotive-logic fabs stimulate local design collaboration but this does not alter Europe's marginal position in the global fabless design market, which remains dominated by U.S. and Asian firms.
- **Rationale:** The JRC (2025) ⁽²⁷¹⁾ reports that Europe accounts for around 9 % of global design revenues when including design carried out within IDMs and embedded-system suppliers, while the BCG & SIA (2024) ⁽²⁷²⁾ estimate that the US retains more than 60 %. However, Europe's share of the global **fabless semiconductor market**, the segment that defines global competitiveness in advanced chip design, is **below 1 %**, according to IFRI (2024) and BCG–SIA (2024). This reflects both the limited scale of Europe's fabless sector and persistent dependence on non-EU EDA tools and manufacturing ecosystems.
- **Implication for competitiveness:** Incremental design growth reinforces Europe's role in high-reliability and industrial segments but Europe's position in globally competitive fabless design remains largely unchanged. Limited EDA autonomy, scale constraints, and shallow late-stage venture capital restrict the emergence of European design champions capable of competing in leading-edge markets.

⁽²⁶⁹⁾ European Court of Auditors. (2025). *Special Report 12/2025 – The EU's strategy for microchips: Reasonable progress in its implementation, but the Chips Act is very unlikely to be sufficient to reach the overly ambitious Digital Decade target.*

⁽²⁷⁰⁾ European Commission, Joint Research Centre (JRC). (2025). *EU's strengths and weaknesses in the global semiconductor sector (JRC141323)*. Luxembourg: Publications Office of the European Union.

⁽²⁷¹⁾ European Commission, Joint Research Centre (JRC). (2025). *EU's strengths and weaknesses in the global semiconductor sector (JRC141323)*. Luxembourg: Publications Office of the European Union.

⁽²⁷²⁾ **Boston Consulting Group (BCG) & Semiconductor Industry Association (SIA)**. (May 2024). *Emerging Resilience in the Semiconductor Supply Chain*.

Share of global advanced-node patents

- **Developments expected under BAU:** Most leading-edge process patents continue to originate outside the EU. New facilities hosting advanced-node production (e.g. Intel Ireland and ESMC Dresden) operate with process IP developed abroad. European patenting remains concentrated in enabling technologies, notably EUV lithography, advanced metrology, power devices, SiC/GaN, and photonics. These fields are at the cutting edge of semiconductor innovation, but they do not substitute for the scale and design ecosystems required for advanced-node CMOS process development.
- **Rationale:** Bruegel (2025) ⁽²⁷³⁾ shows that the EU accounts for only a small fraction of radical innovation patents ⁽²⁷⁴⁾, while McKinsey (2025) ⁽²⁷⁵⁾ and JRC (2025) ⁽²⁷⁶⁾ confirm that Europe's innovation strength lies upstream in equipment and materials rather than node development.
- **Implication for competitiveness:** The EU maintains technological leadership in production equipment and materials science, but it does not close the frontier gap in logic and memory process innovation. Its comparative advantage remains in enabling rather than defining the leading edge.

Public R&D funding for microelectronics (EU + Member States)

- **Developments expected under BAU:** Public support through the Chips Act, IPCEI ME2, and national programmes remains broadly stable at around the current annual level. Funding streams shift towards construction phases of the new fabs but remain modest compared with U.S. and Asian subsidy envelopes.
- **Rationale:** ECA (2025) ⁽²⁷⁷⁾ calculates combined EU and Member-State commitments at about EUR 11 billion over 2021–2030 and describes this as “a small fraction” of global support. The JRC (2025) ⁽²⁷⁸⁾ confirms that Asian and U.S. programmes are considerably larger in scale and faster in implementation.
- **Implication for competitiveness:** Existing funding is sufficient to maintain Europe's strong research institutions and pilot lines but not to transform its position in global innovation hierarchies. Without a significant increase in scale or focus on design and back-end innovation, structural gaps persist.

3. REGIONAL AND TERRITORIAL EFFECTS

3.1. Establishing a starting point for BAU scenario

The European semiconductor landscape is **polycentric but highly uneven**. A handful of core clusters such as **Leuven-Eindhoven (Belgium – the Netherlands), the Dresden area /**

⁽²⁷³⁾ Bruegel. (2025). *Europe's technological divide: Radical novelties, diffusion, and the global race for frontier innovation* (Working Paper 07/2025). Brussels: Bruegel. <https://www.bruegel.org/sites/default/files/2025-07/WP%2007%202025.pdf>

⁽²⁷⁴⁾ Patent families representing entirely new combinations of technology codes in the global patent system. In semiconductors, these identify frontier breakthroughs in materials, device structures, and manufacturing processes. Between 2019 and 2023, the EU produced only 804 such patents, compared with 3 203 in the US and 2 892 in China.

⁽²⁷⁵⁾ McKinsey & Company (2025). *Semiconductors have a big opportunity but barriers to scale remain*. February 2025.

⁽²⁷⁶⁾ European Commission, Joint Research Centre (JRC). (2025). *EU's strengths and weaknesses in the global semiconductor sector (JRC141323)*. Luxembourg: Publications Office of the European Union.

⁽²⁷⁷⁾ European Court of Auditors. (2025). *Special Report 12/2025 – The EU's strategy for microchips: Reasonable progress in its implementation, but the Chips Act is very unlikely to be sufficient to reach the overly ambitious Digital Decade target*.

⁽²⁷⁸⁾ European Commission, Joint Research Centre (JRC). (2025). *EU's strengths and weaknesses in the global semiconductor sector (JRC141323)*. Luxembourg: Publications Office of the European Union.

Saxony (Germany), the Munich area (Germany), the Grenoble area (France), Ireland, the axis Graz-Villach (Austria), and the axis Milano-Turino (Italy) account for the majority of industrial output, R&D investment, and employment. Other regions contribute mainly through packaging, materials, or design services ⁽²⁷⁹⁾.

The six core clusters, that collectively cover less than **8 % of the EU population**, account for the vast majority of semiconductor value creation. Data from **McKinsey (2025)** ⁽²⁸⁰⁾ indicate that approximately **80 % of wafer-fabrication capacity** and **over 70 % of semiconductor-related R&D personnel** are concentrated in these areas, confirming Europe's exceptionally high locational concentration relative to other advanced industries.

The **Joint Research Centre** ⁽²⁸¹⁾ similarly identifies this pattern as one of *geographical lock-in*, where existing clusters continue to attract incremental investment due to cumulative advantages in know-how, infrastructure, and established industrial ecosystems. These regions have become self-reinforcing “centres of gravity” within the European semiconductor landscape, benefiting disproportionately from new fab announcements under the Chips Act and IPCEI ME2.

JRC (2025) ⁽²⁸²⁾ explains that more than **85 % of EU semiconductor exports** originate in just five Member States (Germany, France, the Netherlands, Ireland, and Austria), underscoring the strong asymmetry between core and peripheral regions. **McKinsey (2024)** ⁽²⁸³⁾ also notes that semiconductor ecosystems exhibit strong *path-dependence*: once established, clusters maintain durable competitive advantages through cumulative knowledge spillovers and sunk infrastructure costs, making it extremely difficult for new regions to catch up without major coordinated interventions.

The European semiconductor system thus exhibits certain regional specialisations

- Regions with broad semiconductor activity (Dresden, Grenoble, Eindhoven–Leuven, Munich, Ireland, Milano-Turino, and Graz–Vienna) host IDMs, equipment suppliers, and major R&D institutes.
- Regions with focused technological specialisations (Catania, Regensburg, Villach, Brno, and Wrocław) concentrate on areas including power electronics, metrology, and automotive applications.
- Regions with strong support and complementary activities (Portugal, Hungary, parts of Eastern and Southern Europe) primarily host assembly, testing, or material-processing activities which are more labour intensive.

⁽²⁷⁹⁾ DECISION Études & Conseil (2024), *Mapping of the European Semiconductor Industry and Value Chain: Company Distribution, Regional Clusters and Investment Dynamics*, study prepared for DG CONNECT, European Commission, Brussels.

⁽²⁸⁰⁾ McKinsey & Company (2025), *Semiconductors Have a Big Opportunity, but Barriers to Scale Remain*, McKinsey Global Institute, April 2025.

⁽²⁸¹⁾ European Commission, Joint Research Centre (2025), *EU's Strengths and Weaknesses in the Global Semiconductor Sector*, Publications Office of the European Union, Luxembourg, doi:10.2760/6302476.

⁽²⁸²⁾ Bonnet, P., Ciani, A., Molnar, J., & Nardo, M. (2025). *EU's strengths and weaknesses in the global semiconductor sector* (EUR 40253 EN). Luxembourg: Publications Office of the European Union. <https://doi.org/10.2760/6302476>

⁽²⁸³⁾ McKinsey & Company. (2024). *McKinsey on semiconductors: Creating value, pursuing innovation, and optimizing operations*. New York: McKinsey Global Institute.

This division reflects both market forces and policy design: state-aid frameworks and investment incentives have largely supported existing industrial bases where returns are highest, rather than diffusing activity geographically. The **ECA (2025)** ⁽²⁸⁴⁾ confirms that national co-financing under the Chips Act and IPCEI schemes has been predominantly channelled toward incumbent centres, given their readiness and project scale.

Economic and policy implications

The current degree of concentration delivers clear **efficiency gains** through agglomeration, but it raises **territorial cohesion concerns**:

- **Positive effects:**
 - o Deepened regional specialisation and productivity gains from clustering.
 - o Enhanced innovation networks between firms, research institutes, and universities.
 - o Economies of scale in infrastructure, logistics, and skilled-labour attraction.
- **Negative effects:**
 - o Persistent **geographic inequality** between innovation-intensive regions and the rest of the EU.
 - o **Barriers to entry** for emerging regions lacking pre-existing semiconductor capacity or infrastructure.
 - o **Skill and wage polarisation**, as talent and investment concentrate further in core clusters.

3.2. Modelling the BAU scenario

Under a **Business-as-usual (BAU)** trajectory, Europe's semiconductor geography remains **highly concentrated and path-dependent**. The major industrial and research hubs established before 2025 continue to attract the vast majority of investments, talent, and public support. While new fabs and R&D facilities expand capacity within existing clusters, there is limited diffusion of semiconductor activity to peripheral regions. This results in gradual strengthening of existing agglomerations rather than a structural shift in the European territorial landscape.

Developments expected under BAU

Continuation of core-cluster dominance. Between 2025 and 2035, announced semiconductor investments, including **Intel Ireland, STMicroelectronics–GlobalFoundries Crolles, ESMC Dresden, Infineon Dresden and Villach, and Catania SiC Campus**, consolidate existing regional ecosystems rather than create new ones. By 2035, approximately **80 % of EU semiconductor employment and value added** remains concentrated in the same six core clusters.

Peripheral or emerging regions (e.g. Poland, Czech Republic, Hungary, Portugal, southern Italy) experience moderate growth through supplier linkages, logistics, and equipment subcontracting but remain secondary players. This spatial concentration mirrors the industrial

⁽²⁸⁴⁾ European Court of Auditors. (2025). *Special report 12/2025: The EU's strategy for microchips – Reasonable progress in its implementation, but the Chips Act is very unlikely to be sufficient to reach the overly ambitious Digital Decade target.*

geography of other global semiconductor ecosystems, such as the U.S. ‘*Silicon Triangle*’ (linking California, Arizona, and Texas) and the East Asian manufacturing corridor connecting Taiwan, Japan, and South Korea ⁽²⁸⁵⁾, ⁽²⁸⁶⁾.

Limited emergence of new hubs. Despite EU policy efforts to enhance territorial cohesion, most **new greenfield fabs and pilot lines** locate near existing ecosystems to exploit established infrastructure, supplier proximity, and skilled labour pools. New entrants in Central and Eastern Europe mainly target packaging, assembly, or materials production rather than high-value design or advanced-node manufacturing. **JRC (2025)** ⁽²⁸⁷⁾ projects that under current policies, fewer than **20 % of new semiconductor investments** by 2035 will occur outside the existing top-tier regions.

Cross-border consolidation and functional integration. Core regions become increasingly interconnected across borders, forming a **North-Central European semiconductor corridor** linking the Netherlands, Belgium, Germany, France, and Austria. Industrial interdependencies, e.g. between ASML (Netherlands) and imec (Belgium) strengthen vertical integration within this corridor. This cross-border clustering reinforces Europe’s strengths in equipment, materials, and power devices but further marginalises outer regions.

Regional spillovers and supplier linkages. Peripheral regions benefit from indirect employment and supply chain effects during fab construction and through service provision. Supplier multipliers estimated by **Deloitte (2021)** ⁽²⁸⁸⁾ and **McKinsey (2024)** ⁽²⁸⁹⁾ suggest that each direct semiconductor job supports 5–6 indirect jobs, mainly in construction, utilities, and logistics. However, these spillovers remain largely **localised near established hubs**; broader diffusion toward less developed regions is minimal without additional policy intervention.

Rationale and evidence base

The persistence of concentration under BAU reflects several reinforcing factors:

1. **Infrastructure and sunk capital:** Semiconductor fabs and equipment clusters are among the most capital-intensive industrial assets, creating long-term lock-in effects once located. **McKinsey (2025)** ⁽²⁹⁰⁾ explains that global semiconductor investments show strong path-dependence due to the high irreversibility of capital expenditure and skill accumulation.

⁽²⁸⁵⁾ McKinsey & Company. (2025). *Semiconductors have a big opportunity, but barriers to scale remain*. New York: McKinsey Global Institute.

⁽²⁸⁶⁾ Boston Consulting Group (BCG) & Semiconductor Industry Association (SIA). (2024). *Emerging resilience in the semiconductor supply chain*. May 2024. Boston: Boston Consulting Group and Semiconductor Industry Association.

⁽²⁸⁷⁾ Bonnet, P., Ciani, A., Molnar, J., & Nardo, M. (2025). *EU’s strengths and weaknesses in the global semiconductor sector* (EUR 40253 EN). Luxembourg: Publications Office of the European Union. <https://doi.org/10.2760/6302476>

⁽²⁸⁸⁾ Deloitte. (2021). *Measuring semiconductors’ economic impact: How many jobs does the semiconductor industry create?* Deloitte Insights, September 2021.

⁽²⁸⁹⁾ McKinsey & Company. (2024). *McKinsey on semiconductors: Creating value, pursuing innovation, and optimizing operations*. New York: McKinsey Global Institute.

⁽²⁹⁰⁾ McKinsey & Company. (2025). *Semiconductors have a big opportunity, but barriers to scale remain*. New York: McKinsey Global Institute.

2. **Talent availability:** The **European Chips Skills Academy** ⁽²⁹¹⁾ and **JRC (2025)** ⁽²⁹²⁾ highlight persistent labour shortages, with engineering and technician gaps particularly acute outside existing hubs. Firms therefore concentrate expansion where talent pools and training infrastructure already exist. Although Competence Centres are being established in all Member States to broaden access to design support, specialised training, and prototyping services, their impact under BAU is expected to improve participation rather than materially shift the location of large-scale industrial investments.
3. **Network and innovation effects:** Co-location of R&D, suppliers, and production drives economies of scope. **BCG (2024)** ⁽²⁹³⁾ notes that advanced-packaging and materials innovation depend on physical proximity between design centres and fabs, favouring the established clusters.
4. **Policy structure:** State-aid rules and IPCEI frameworks incentivise large-scale projects requiring national co-financing. **ECA (2025)** ⁽²⁹⁴⁾ reports that this has channelled most support to high-capacity incumbents in Germany, France, Ireland, and the Netherlands, limiting the potential for geographical diversification. While Competence Centres provide nationwide support services, they do not alter the underlying factors shaping the siting of major manufacturing projects under BAU.

Implications

Regional concentration and productivity. Under BAU, the **top six NUTS-2 regions** slowly increase their combined share of semiconductor-related value added, driven by cumulative investment and productivity gains. Agglomeration effects enhance efficiency and innovation capacity but create **structural divergence** between high-performing clusters and lagging regions.

Labour markets and skills. Regional labour-market effects mirror the overall pattern of agglomeration. Core regions face **tight labour markets** and wage pressures, while peripheral regions experience limited job creation. Cross-border mobility of engineers remains insufficient to offset regional imbalances, as **McKinsey (2024)** ⁽²⁹⁵⁾ and **ECSA (2024)** ⁽²⁹⁶⁾ report.

Environmental and infrastructure pressures. High-capacity clusters such as Dresden, Crolles–Grenoble, and Dublin experience growing strain on local **energy and water systems**, reinforcing regional environmental pressures identified in section 3.3. In contrast, potential sites with available capacity in peripheral regions remain underutilised.

⁽²⁹¹⁾ European Chips Skills Academy. (2024). ECSA Skills Strategy 2024 (rev 20052025). <https://chipsacademy.eu/wp-content/uploads/2025/05/ECSA-Skills-Strategy-2024-rev-20052025.pdf>

⁽²⁹²⁾ Bonnet, P., Ciani, A., Molnar, J., & Nardo, M. (2025). *EU's strengths and weaknesses in the global semiconductor sector* (EUR 40253 EN). Luxembourg: Publications Office of the European Union. <https://doi.org/10.2760/6302476>

⁽²⁹³⁾ Boston Consulting Group. (2024). *Advanced packaging is reshaping the chip industry*. Boston: Boston Consulting Group, February 2024.

⁽²⁹⁴⁾ European Court of Auditors. (2025). *Special Report 12/2025 – The EU's strategy for microchips: Reasonable progress in its implementation, but the Chips Act is very unlikely to be sufficient to reach the overly ambitious Digital Decade target*.

⁽²⁹⁵⁾ McKinsey & Company. (2024). *McKinsey on semiconductors: Creating value, pursuing innovation, and optimizing operations*. New York: McKinsey Global Institute.

⁽²⁹⁶⁾ European Chips Skills Academy. (2024). ECSA Skills Strategy 2024 (rev 20052025). <https://chipsacademy.eu/wp-content/uploads/2025/05/ECSA-Skills-Strategy-2024-rev-20052025.pdf>

Overall, under BAU conditions, the **regional geography of Europe's semiconductor industry remains largely unchanged through 2035.**

- Existing high-tech clusters consolidate their dominance, benefiting from cumulative investment, infrastructure, and skills ecosystems.
- Cross-border integration between Benelux, Germany, France, and Austria forms a competitive “semiconductor corridor”, but without significant geographic expansion.
- Peripheral Member States gain limited spillovers, primarily through supply chain participation and service contracts, without achieving substantial localisation of high-value activities.
- Territorial cohesion objectives therefore remain only partially fulfilled, as structural imbalances persist between innovation-intensive core regions and industrial peripheries.

4. MODELLING ENVIRONMENTAL IMPACTS

4.1. Environmental impacts

4.1.1. Establishing a starting point for BAU scenario

When addressing sustainability in semiconductor manufacturing, attention often alternates between climate-related and broader environmental considerations. Climate concerns primarily pertain to greenhouse gas (GHG) emissions, including those from high global warming potential (GWP) gases and the energy consumption associated with raw materials mining and processing as well as chemicals refinement and wafer fabrication. These factors are commonly monitored using the Greenhouse Gas (GHG) Protocol, a widely adopted and standardised global framework.

Regarding the climate impact of chip production in Europe, scope 1 (mainly fluorinated gases) and scope 2 (mainly energy consumption) emissions are dominating the sectors carbon footprint (see below). ⁽²⁹⁷⁾ Scope 3 covers emissions across the entire value chain, both upstream and downstream. Semiconductor manufacturers generally do not report the climate footprint of their products, as these are classified as *intermediate goods*. This lack of disclosure, combined with limited research on the ecological footprint during end-product operation, makes it challenging to obtain reliable and granular data on overall environmental impacts. ⁽²⁹⁸⁾ It is nevertheless important to note that the ecological impact during the operational phase of end-products varies substantially depending on their final application. Battery-powered devices such as tablets and smartphones exhibit higher emissions during manufacturing, whereas data centres - characterised by intensive energy use - generate significant emissions during operation. This issue is particularly pronounced in GPU-based data centres used for artificial intelligence (AI), where extreme thermal stress leads to accelerated hardware degradation. As a result, GPUs often need to be replaced every two to four years, a phenomenon known as *chip aging*.

⁽²⁹⁷⁾ Interface (2024). Chip Production's Ecological Footprint: Mapping Climate and Environmental Impact. <https://www.interface-eu.org/publications/chip-productions-ecological-footprint>

⁽²⁹⁸⁾ Interface (2024). Chip Production's Ecological Footprint: Mapping Climate and Environmental Impact. <https://www.interface-eu.org/publications/chip-productions-ecological-footprint>

Environmental considerations, by contrast, encompass aspects such as water consumption, the ecological impacts of raw material extraction, risks of chemical contamination to ecosystems and human health via forever chemicals (such as PFAS), and the challenges of waste management arising from chip production and electronic device end-of-life processes. In addition, greenfield investments are requiring massive land to host the large-scale clean-room infrastructure. ⁽²⁹⁹⁾

Scope 1 emissions (direct emissions) and PFAS

The environmental impacts of semiconductor production in the EU are regulated, inter alia, by Regulation (EU) No 2024/573 on fluorinated greenhouse gases (F-gases). F-gases are human-made chemicals that are very strong greenhouse gases (GHG), often several thousand times stronger than carbon dioxide (CO₂). Under the F-gas Regulation, the semiconductor industry sector is covered by a prohibition to intentionally emit F-gases as well as requirements to take technically and economically feasible measures to minimise unintentional (“leakage”) of these gases. These rules have been reinforced recently with the new 2024 update of the Regulation.

While the production of semiconductors uses some of the F-gases with the highest global warming potential (e.g. trifluoromethane (HFC-23), perfluorocarbons (PFCs), nitrogen trifluoride (NF₃), sulphur hexafluoride (SF₆) etc.), the quantities are still modest amounting currently to about a few percent of total current F-gas emissions in the EU. ⁽³⁰⁰⁾

Generally, the EU semiconductor industry is taking stricter measures during its manufacturing processes to prevent emitting F-gases compared to other world regions. The sector is claiming to have made substantial investments to implement reduction practices at operations across Europe. The European Semiconductor Industry Association (ESIA) estimated in 2021 that the industry had achieved a 42% absolute emission reduction of PFCs between 2010 and 2020. ⁽³⁰¹⁾ If looked at from a global perspective, an increased and significant production of semiconductors in the EU while minimising where possible emissions, is likely to save emissions from F-gases at global scale.

While past efforts have reduced emissions by substituting longer-chain per-and polyfluoroalkyl substances (PFAS) with short-chain alternatives, further reductions necessitate entirely new compounds, presenting a complex challenge. Switching to alternative chemicals involves balancing global warming potential (GWP) and atmospheric persistence, often leading to trade-offs. For instance, while CHF₃ has a higher GWP than CF₄, CF₄ stays longer in the atmosphere.

Despite the urgency, transitioning away from harmful compounds will require time, with challenges varying across processes. Solutions for cleaning processes may emerge within 5–10 years, while alternatives for dry etching could take more than 15 years. Generally,

⁽²⁹⁹⁾ Interface (2024). Chip Production’s Ecological Footprint: Mapping Climate and Environmental Impact. <https://www.interface-eu.org/publications/chip-productions-ecological-footprint>

⁽³⁰⁰⁾ See Impact Assessment to: Regulation (EU) No 517/2014 of the European Parliament and of the Council of 16 April 2014 on fluorinated greenhouse gases and repealing Regulation (EC) No 842/2006 Text with EEA relevance: https://ec.europa.eu/clima/document/download/9013881e-8d5d-429e-9112-c908f127c833_en?filename=f-gases_impact_assessment_en.pdf

⁽³⁰¹⁾ <https://www.electronicsspecifier.com/industries/alternative-energy/european-fluorinated-greenhouse-gas-emissions-cut-by-42>

implementation of non-PFAS alternatives is expected to take 15 to more than 20 years. This transition incurs substantial research and transition costs, underscoring the need for a long-term commitment to sustainability. Certain of these forever chemicals used in semiconductor manufacturing are included in the proposed ban on PFAS under the REACH regulation. ⁽³⁰²⁾

Scope 2 emissions (indirect emissions)

Electricity represents the largest share of energy consumption in semiconductor manufacturing and is the primary source of GHG emissions in chip production. The amount of electricity used varies significantly depending on factors such as chip type, manufacturing process complexity, and lithography technology. More advanced processes, such as extreme ultraviolet (EUV) lithography, consume substantially more energy. For instance, 5 nm logic manufacturing processes require roughly three times as much electricity as 32 nm processes. This illustrates that it is not possible to provide a general estimate of energy consumption per wafer without specifying the manufacturing process, technology type, and node. ⁽³⁰³⁾

Very broadly speaking estimates suggest that large, advanced wafer fabrication facilities can draw more than 100 MW of continuous power - comparable to the electricity demand of a small city. From a global perspective, total energy consumption in semiconductor manufacturing increased by approximately 125% between 2015 and 2023. This growth is driven not only by the increasing complexity of manufacturing processes and equipment but also by the substantial expansion of global production capacity and increased operation of abatement equipment. ⁽³⁰⁴⁾

There are two distinct methods for scope 2 accounting. A location-based method reflects the average emissions intensity of grids on which energy consumption occurs (using mostly grid-average emission factor data). ⁽³⁰⁵⁾ A market-based method reflects emissions from electricity that companies have purposefully chosen (or their lack of choice). ⁽³⁰⁶⁾ In the estimations below, both scope 2 accounting methods will be presented.

4.1.2. Environmental impact assessment for BAU scenario

Reported total emissions from EU chip production in 2021 amounted to be between 10.67 Mio tCO₂e and 13.67 Mio tCO₂e. ⁽³⁰⁷⁾ Assuming, no major changes in total emissions by 2024, this matches our own calculations for scope 1 and 2 emissions in Europe. Assuming that Europe's current yearly manufacturing capacity of wafers is around 12.84 Mio, scope 1 emissions are estimated to reach between 821 760 ⁽³⁰⁸⁾ – 1 027 000 ⁽³⁰⁹⁾ tCO₂e, with scope 2 (location-based) being around 4 173 000 ⁽²⁹⁰⁾ – 5 392 800 ⁽³⁰⁸⁾ tCO₂e. Our analysis lacks the reporting on scope 3 emissions due to missing standardisation. However, as the average share

⁽³⁰²⁾ <https://www.interface-eu.org/publications/chip-productions-ecological-footprint>

⁽³⁰³⁾ <https://www.interface-eu.org/publications/semiconductor-emission-explorer>

⁽³⁰⁴⁾ <https://www.interface-eu.org/publications/semiconductor-emission-explorer>

⁽³⁰⁵⁾ [Scope 2 Guidance.pdf](#)

⁽³⁰⁶⁾ [Scope 2 Guidance.pdf](#)

⁽³⁰⁷⁾ <https://www.interface-eu.org/publications/chip-productions-ecological-footprint>

⁽³⁰⁸⁾ Own calculations

⁽³⁰⁹⁾ [Die Setup - imec.netzero](#); technologies: N28 (Logic Mobile SoC, 300 mm), Germany - average ; 10 mm die size X and die size Y: yield 85%; IPCC Tier 2C with combustion abatement model

of scope 3 emissions among the 20 largest chip manufacturers was 65% in 2021 ⁽³¹⁰⁾, and assuming scope 3 emissions did not change significantly over the last 3 years, the total emissions from EU chip manufacturing in 2024 are indeed estimated to be between 10.67 Mio tCO₂e and 13.67 Mio tCO₂e. Using imec.netzero model ⁽³¹¹⁾, total scope 3 emissions are estimated to be around 3 466 800 tCO₂e.

Estimated EU's total scope 1 and 2 emissions (location and market-based) were calculated based on scope 1 and 2 emissions reported for the Global Foundries (GF) fab in Dresden in 2023 assuming maximum yearly wafer capacity of 950 000. ⁽³¹²⁾ Data from Global Foundries fab in Dresden were purposefully chosen to reflect as much as possible the European reality. Among available disclosures, only GlobalFoundries provided **both site-level emissions data and corresponding wafer capacity**, which enabled transparent calculation of emissions intensity and supports a defensible proxy for European fab operations.

Additionally, imec.netzero multi-parametric Life-Cycle Assessment model that calculates the environmental footprint for the fabrication of integrated circuits in a high-volume semiconductor fab was also used and the data achieved are consistent with our own calculations. ⁽³¹³⁾ One of the major additional benefits of the imec.netzero model is the inclusion of scope 3 emissions.

To estimate total EU emissions for scope 1 and 2, first emissions per wafer were calculated for the **Global Foundries fab in Dresden**.

Maximum yearly wafer capacity /wpy	950 000 ⁽³¹⁴⁾
Scope 1 emissions / tCO ₂ e	60 831 ⁽³¹⁵⁾
Scope 2 emissions (location-based) / tCO ₂ e	308 337 ⁽³¹⁶⁾
Scope 2 emissions (market-based) / tCO ₂ e	273 995 ⁽³¹⁷⁾
Scope 1 emissions / tCO ₂ e/wafer	≈ 0.064
Scope 2(location-based) emissions / tCO ₂ e/wafer	≈ 0.325
Scope 2 (market-based) emissions / tCO ₂ e/wafer	≈ 0.288
Total current capacity /wpy	≈ 12.84 Mio
Estimated total scope 1 emissions / tCO ₂ e	≈ 821 760

⁽³¹⁰⁾ <https://www.interface-eu.org/publications/chip-productions-ecological-footprint>

⁽³¹¹⁾ [Die Setup - imec.netzero](#); technologies: N28 (Logic Mobile SoC, 300 mm), Germany - average ; 10 mm die size X and die size Y: yield 85%; IPCC Tier 2C with combustion abatement model

⁽³¹²⁾ 2023 data are taken into account as from 1st January 2024, a cogeneration plant at the Dresden site came under the operational control of GF and the emissions from the plant are being reported as scope 1 emissions. Before 1st January 2024 they were categorised as scope 2 emissions.

⁽³¹³⁾ [Die Setup - imec.netzero](#); technologies: N28 (Logic Mobile SoC, 300 mm), Germany - average ; 10 mm die size X and die size Y: yield 85%; IPCC Tier 2C with combustion abatement model

⁽³¹⁴⁾ [Dresden: Facts, figures, data | GlobalFoundries](#)

⁽³¹⁵⁾ [CDP -GlobalFoundries-Inc.-09-10-2024-CORPORATE_public_version.pdf](#)

⁽³¹⁶⁾ [CDP -GlobalFoundries-Inc.-09-10-2024-CORPORATE_public_version.pdf](#)

⁽³¹⁷⁾ [CDP -GlobalFoundries-Inc.-09-10-2024-CORPORATE_public_version.pdf](#)

Estimated total current scope 2 (location-based) emissions / tCO ₂ e	≈ 4 173 000
Estimated total current scope 2 (market-based) emissions / tCO ₂ e	≈ 3 697 920

Data achieved from imec.netzero model for N28 (Logic Mobile SoC, 300 mm) are presented in the Table below. ⁽³¹⁸⁾

Scope 1 emissions / tCO ₂ e/wafer	0.08 ⁽³¹⁷⁾
Estimated total scope 1 emissions / tCO ₂ e	1 027 000
Scope 2 emissions / tCO ₂ e/wafer	0.42 ⁽³¹⁷⁾
Estimated total current scope 2 (location-based) emissions / tCO ₂ e	5 392 800
Scope 3 emissions / tCO ₂ e/wafer	0.27 ⁽³¹⁷⁾
Estimated total current scope 3 emissions / tCO ₂ e	3 466 800

However, because Europe accounts for only a small share of global semiconductor manufacturing capacity compared with its Asian counterparts, its associated emissions remain well below those of high-emitting sectors.

Water

A large semiconductor fabrication plant (fab) uses up to 38 million litres per day, equivalent to the daily water consumption of around 300,000 people in Germany. ⁽³¹⁹⁾ Water is primarily used for ultrapure water (UPW) production, a complex process that involves multi-stage treatments, such as reverse osmosis and ultrafiltration, with water reuse and recycling being common on-site practices. ⁽³²⁰⁾

Semiconductor manufacturing in Europe reflects the global characteristics of the industry: it is among the most resource- and energy-intensive industrial activities per unit of value added. The deployment of advanced wafer fabrication processes in Europe would likely result in a substantial increase in emissions. However, European fabs benefit from a comparatively low-carbon electricity mix: the average grid emission intensity is roughly one-third that of major East Asian manufacturing regions. ⁽³²¹⁾ Despite this advantage, electricity use remains the single largest contributor to lifecycle emissions, accounting for approximately 60–70% of total CO₂-equivalent emissions in front-end manufacturing. ⁽³²²⁾⁽³²³⁾⁽³²⁴⁾

⁽³¹⁸⁾ [Die Setup - imec.netzero](#); technologies: N28 (Logic Mobile SoC, 300 mm), Germany - average ; 10 mm die size X and die size Y: yield 85%; IPCC Tier 2C with combustion abatement model

⁽³¹⁹⁾ Interface (2024). Chip Production's Ecological Footprint: Mapping Climate and Environmental Impact. <https://www.interface-eu.org/publications/chip-productions-ecological-footprint>

⁽³²⁰⁾ IMEC. (2022). *Sustainable Semiconductor Manufacturing: A Path Forward*. IMEC Research Report.

⁽³²¹⁾ International Energy Agency (IEA). (2023). *Energy Efficiency in Industry: Semiconductor Manufacturing Focus*. Paris: IEA.

⁽³²²⁾ European Commission, Joint Research Centre (JRC). (2025). *EU's strengths and weaknesses in the global semiconductor sector (JRC141323)*. Luxembourg: Publications Office of the European Union.

⁽³²³⁾ McKinsey & Company. (2025). *Semiconductors have a big opportunity—but barriers to scale remain*. McKinsey Global Institute.

Overall, semiconductor manufacturing is extremely water intensive. Current water withdrawal per wafer in Europe is estimated to be about 10.75 m³ ⁽³²⁵⁾ (some reports give even higher values of 15 m³ per 12-inch wafer ⁽³²⁶⁾), which accounts for around 138 Mio m³ water used per year during semiconductor manufacturing, assuming 12.8 Mio wafer capacity in the EU.

Waste

Apart from GHG emissions and various volatile organic compounds that are released into the atmosphere, front-end manufacturing generates chemical waste, solid waste, wastewater, slurries and abrasives and packaging waste. In the last eight years, the amount of waste generated in the semiconductor industry has nearly doubled. ⁽³²⁷⁾

Regarding the environmental impact, it is important to differentiate between general or non-hazardous waste and hazardous waste. ⁽³²⁸⁾ For most semiconductor manufacturers, the ratio between hazardous and non-hazardous waste is 40%–60%. ⁽³²⁹⁾ Unused or spent chemicals, such as those that can be categorised as PFAS, often contain waste acids, waste solvents, waste copper sulphate, heavy metals, etc., which end up in either chemical waste or wastewater. ⁽³³⁰⁾ If not treated properly, they pose a high risk to environmental and human health. The same applies to waste slurries, which consist of solid and potentially abrasive and hazardous particles suspended in water from chemical mechanical polishing (CMP) processes. ⁽³³¹⁾

Front-end manufacturers have put in place waste classification and separation, as well as safe treatment practices to comply with regulations and increase the share of recyclable waste. Within the last decade, most manufacturers have achieved high external recycling rates and very low rates of disposal to landfill. A low share of hazardous waste needs to be treated by specially authorised companies. On average, around 70% of all hazardous and non-hazardous wastes can be recycled for reuse in other industries. ⁽³³²⁾ It is much more difficult to recycle waste to be reused within the front-end manufacturing process itself. The share of preparation for reuse in a fab varies significantly and is mostly applied to chemical reuse from hazardous waste. A recent example is the invention of neon gas recycling technology, which can reduce emissions in the production and usage of neon gas, as well as in waste treatment. ⁽³³³⁾ Additionally, waste is burnt with recovery for energy; only 1%–5% of waste is sent to landfill. ⁽³³⁴⁾

⁽³²⁴⁾ IMEC. (2022). *Sustainable Semiconductor Manufacturing: A Path Forward*. IMEC Research Report.

⁽³²⁵⁾ Calculations based on total water withdrawals by Global Foundries in 2023 ([CDP -GlobalFoundries-Inc.-09-10-2024-CORPORATE_public_version.pdf](#)) assuming total wafer shipments of 2.2 Mio wpy

⁽³²⁶⁾ [Water-Europe-Socio-Economic-Study-1.pdf](#)

⁽³²⁷⁾ Ian King (2022): Chipmakers' \$52 Billion US Bonanza Imperils Environmental Gains. Bloomberg.

⁽³²⁸⁾ [Waste | NXP Semiconductors](#)

⁽³²⁹⁾ Interface (2024). Chip Production's Ecological Footprint: Mapping Climate and Environmental Impact. [Chip Production's Ecological Footprint: Mapping Climate and Environmental Impact](#)

⁽³³⁰⁾ [Waste | NXP Semiconductors](#)

⁽³³¹⁾ [Waste | NXP Semiconductors](#)

⁽³³²⁾ Interface (2024). Chip Production's Ecological Footprint: Mapping Climate and Environmental Impact. [Chip Production's Ecological Footprint: Mapping Climate and Environmental Impact](#)

⁽³³³⁾ <https://www.gasworld.com/story/industrys-first-neon-gas-recycling-technology-announced-by-sk-hynix-temc/2136766.article/>

⁽³³⁴⁾ Ibid Interface (2024). Chip Production's Ecological Footprint: Mapping Climate and Environmental Impact. [Chip Production's Ecological Footprint: Mapping Climate and Environmental Impact](#)

4.1.3. Modelling for different scenarios

Developments expected under BAU to 2035

Energy consumption: Under BAU, the total energy demand of Europe's semiconductor industry increases substantially as announced fabs in Germany, France, Ireland, and Italy become operational. Despite continued grid decarbonisation and growing uptake of power purchase agreements (PPAs) and on-site renewables, absolute electricity use more than doubles by 2035. Energy intensity per wafer will most likely grow due to the transition to more advanced lithography equipment, growing overall complexity in manufacturing processes and increased use of abatement equipment.

Water use and waste treatment: Water stress becomes an increasing constraint on site selection, particularly in regions with limited freshwater availability such as Saxony and southern France. ⁽³³⁵⁾ Most new fabs incorporate water-recycling systems targeting 75–85 % reuse, yet total consumption still rises with industry expansion and growing complexity of manufacturing processes. ⁽³³⁶⁾⁽³³⁷⁾ Chemical-waste treatment and ultrapure-water systems continue to account for roughly 20–30 % of fab operating expenditure related to utilities. ⁽³³⁸⁾⁽³³⁹⁾

With the estimated 20.28 Mio wpy produced in Europe in 2035, the water withdrawal will reach 218 Mio m³.

Land use and spatial footprint: Land requirements expand through new industrial parks and fab extensions, but EU planning and permitting rules constrain excessive sprawl. ⁽³⁴⁰⁾ Environmental impact assessments (EIAs) and biodiversity-offset obligations remain stringent, while approval timelines continue to be long due to the environmental sensitivity of large-scale semiconductor sites. ⁽³⁴¹⁾

Emissions:

Under BAU, EU front-end manufacturing capacity grows, from 1.07 million wpm in 2023 to around 1.48 million wpm by 2030 and 1.56–1.82 million wpm by 2035, maintaining a stable 8–9% of global capacity share. Taking the average of this range, under BAU the EU's front-end manufacturing capacity in 2035 will reach 1.69 Mio wpm, which is 20.28 Mio wpy (as estimated in Annex 4, Section 1.2). Therefore, based on the scope 1 and 2 emissions reported for the Global Foundries (GF) fab in Dresden in 2023, and extrapolating to European wafer production capacity, the total Europe's scope 1 and 2 emissions from front-end manufacturing in 2035 can be estimated.

⁽³³⁵⁾ European Commission, Joint Research Centre (JRC). (2025). *EU's strengths and weaknesses in the global semiconductor sector (JRC141323)*. Luxembourg: Publications Office of the European Union.

⁽³³⁶⁾ SEMI. (2023). *Sustainability in the Semiconductor Manufacturing Supply Chain*. SEMI Global Update.

⁽³³⁷⁾ McKinsey & Company. (2025). *Semiconductors have a big opportunity—but barriers to scale remain*. McKinsey Global Institute.

⁽³³⁸⁾ IMEC. (2022). *Sustainable Semiconductor Manufacturing: A Path Forward*. IMEC Research Report.

⁽³³⁹⁾ SEMI. (2023). *Sustainability in the Semiconductor Manufacturing Supply Chain*. SEMI Global Update.

⁽³⁴⁰⁾ European Court of Auditors. (2025). *Special Report 12/2025 – The EU's strategy for microchips: Reasonable progress in its implementation, but the Chips Act is very unlikely to be sufficient to reach the overly ambitious Digital Decade target*.

⁽³⁴¹⁾ European Commission, Joint Research Centre (JRC). (2025). *EU's strengths and weaknesses in the global semiconductor sector (JRC141323)*. Luxembourg: Publications Office of the European Union.

Estimated average capacity in 2035 / wpy	≈ 20.28 Mio
Estimated total scope 1 emissions in 2035 under BAU / tCO ₂ e	≈ 1 297 920
Estimated total scope 2 (location-based) emissions in 2035 under BAU / tCO ₂ e	≈ 6 591 000
Estimated total scope 2 (market-based) emissions in 2035 under BAU / tCO ₂ e	≈ 5 840 640
Estimated total scope 1 emissions in 2035 under BAU using imec.netzero model ⁽³⁴²⁾ / tCO ₂ e	1 622 400
Estimated total scope 2 emissions in 2035 under BAU using imec.netzero model ⁽³⁴³⁾ / tCO ₂ e	8 517 600
Estimated total scope 3 emissions in 2035 under BAU using imec.netzero model ⁽³⁴⁴⁾ / tCO ₂ e	5 475 600

Emissions from fluorinated gases (e.g. perfluorocarbons [PFCs], SF₆) decline slightly owing to substitution and abatement technologies, supported by international efforts under the Kyoto-Protocol gases framework. ⁽³⁴⁵⁾ Nevertheless, indirect emissions from electricity consumption dominate the sector's carbon balance until full grid decarbonisation is achieved. ⁽³⁴⁶⁾⁽³⁴⁷⁾ By 2035, Europe's fab-related emissions intensity is expected to fall by roughly 20–25 %, but total emissions still rise in line with overall capacity growth. ⁽³⁴⁸⁾⁽³⁴⁹⁾

Rationale

Environmental performance improves gradually under BAU thanks to incremental technology gains, stricter EU environmental standards, and a cleaner electricity mix. ⁽³⁵⁰⁾⁽³⁵¹⁾ European fabs benefit from ongoing grid decarbonisation, adoption of power purchase agreements (PPAs), and diffusion of energy- and water-efficiency technologies such as heat recovery and closed-loop recycling. ⁽³⁵²⁾⁽³⁵³⁾

⁽³⁴²⁾ [Die Setup - imec.netzero](#); technologies: N28 (Logic Mobile SoC, 300 mm), Germany - average ; 10 mm die size X and die size Y: yield 85%; IPCC Tier 2C with combustion abatement model

⁽³⁴³⁾ [Die Setup - imec.netzero](#); technologies: N28 (Logic Mobile SoC, 300 mm), Germany - average ; 10 mm die size X and die size Y: yield 85%; IPCC Tier 2C with combustion abatement model

⁽³⁴⁴⁾ [Die Setup - imec.netzero](#); technologies: N28 (Logic Mobile SoC, 300 mm), Germany - average ; 10 mm die size X and die size Y: yield 85%; IPCC Tier 2C with combustion abatement model

⁽³⁴⁵⁾ IMEC. (2022). *Sustainable Semiconductor Manufacturing: A Path Forward*. IMEC Research Report.

⁽³⁴⁶⁾ McKinsey (2025). *Semiconductors have a big opportunity—but barriers to scale remain*. McKinsey Global Institute.

⁽³⁴⁷⁾ International Energy Agency (IEA). (2023). *Energy Efficiency in Industry: Semiconductor Manufacturing Focus*. Paris: IEA.

⁽³⁴⁸⁾ European Commission, Joint Research Centre (JRC). (2025). *EU's strengths and weaknesses in the global semiconductor sector (JRC141323)*. Luxembourg: Publications Office of the European Union.

⁽³⁴⁹⁾ McKinsey (2025). *Semiconductors have a big opportunity—but barriers to scale remain*. McKinsey Global Institute.

⁽³⁵⁰⁾ European Commission, Joint Research Centre (JRC). (2025). *EU's strengths and weaknesses in the global semiconductor sector (JRC141323)*. Luxembourg: Publications Office of the European Union.

⁽³⁵¹⁾ International Energy Agency (IEA). (2023). *Energy Efficiency in Industry: Semiconductor Manufacturing Focus*. Paris: IEA.

⁽³⁵²⁾ IMEC. (2022). *Sustainable Semiconductor Manufacturing: A Path Forward*. IMEC Research Report.

⁽³⁵³⁾ McKinsey (2025). *Semiconductors have a big opportunity—but barriers to scale remain*. McKinsey Global Institute.

However, structural factors such as high capital intensity, dependence on specialty chemicals, and the 24/7 operational nature of fabs limit the scope for deep decarbonisation without major technological or process breakthroughs. ⁽³⁵⁴⁾⁽³⁵⁵⁾⁽³⁵⁶⁾

Implications

Under BAU conditions, Europe's semiconductor expansion increases the industry's absolute environmental footprint despite moderate efficiency gains. ⁽³⁵⁷⁾⁽³⁵⁸⁾ SMEs in supply chain segments particularly in materials, chemicals, and component processing face higher compliance costs as environmental reporting and permitting become more stringent under EU legislation such as the Industrial Emissions Directive and CSRD, while large fabs are better positioned to absorb these through scale and dedicated compliance teams. ⁽³⁵⁹⁾⁽³⁶⁰⁾ Water and energy efficiency technologies, including closed-loop recycling, waste-heat recovery, and renewable PPAs, become standard features of new facilities by the early 2030s, ⁽³⁶¹⁾⁽³⁶²⁾ but their diffusion across smaller suppliers remains uneven. In comparison to other manufacturing regions internationally, Europe has positioned itself as the frontier manufacturing hub when it comes to more sustainable solutions not only due to the availability of renewable energy but also due to its excellent research and development strengths in the supplier markets (equipment & chemicals) as well as in chip production.

4.1.4. Developments expected under Policy Option 1

It was assumed that, under Policy Option 1 (PO1), more favourable policy frameworks would lead to a growth rate of 4% from 2030 onwards. This would lead to the capacity of 20.3 Mio wafer per year, which in turn would account to between 1.3 – 1.6 MtCO₂ in scope 1 emissions and 6.6 – 8.526 MtCO₂ in scope 2 emissions (location-based). Estimated EU's total scope 1 and 2 emissions (location-based) of PO1 were calculated based on scope 1 and 2 emissions reported for the Global Foundries (GF) fab in Dresden in 2023 and imec.netzero model. ⁽³⁶³⁾⁽³⁶⁴⁾

4.1.5. Developments expected under Policy Option 2

Under Policy Option 2, two scenarios were envisaged:

1. Scenario 1 - in which new investments broadly replicate the current European wafer mix and technology profile;

⁽³⁵⁴⁾ IMEC. (2022). *Sustainable Semiconductor Manufacturing: A Path Forward*. IMEC Research Report.

⁽³⁵⁵⁾ McKinsey (2025). *Semiconductors have a big opportunity—but barriers to scale remain*. McKinsey Global Institute.

⁽³⁵⁶⁾ Boston Consulting Group (BCG). (2024). *Advanced packaging is reshaping the chip industry*. BCG Report.

⁽³⁵⁷⁾ European Commission, Joint Research Centre (JRC). (2025). *EU's strengths and weaknesses in the global semiconductor sector (JRC141323)*. Luxembourg: Publications Office of the European Union.

⁽³⁵⁸⁾ McKinsey (2025). *Semiconductors have a big opportunity—but barriers to scale remain*. McKinsey Global Institute.

⁽³⁵⁹⁾ European Court of Auditors. (2025). *Special Report 12/2025 – The EU's strategy for microchips: Reasonable progress in its implementation, but the Chips Act is very unlikely to be sufficient to reach the overly ambitious Digital Decade target*.

⁽³⁶⁰⁾ Ebrahimi, A. (2024). *Groundbreaking chip sovereignty: Europe's strategic push in the semiconductor race*. Ifri Memos, Institut français des relations internationales (IFRI). ISBN 979-10-373-0874-0.

⁽³⁶¹⁾ IMEC. (2022). *Sustainable Semiconductor Manufacturing: A Path Forward*. IMEC Research Report.

⁽³⁶²⁾ SEMI. (2023). *Sustainability in the Semiconductor Manufacturing Supply Chain*. SEMI Global Update.

⁽³⁶³⁾ [CDP -GlobalFoundries-Inc.-09-10-2024-CORPORATE_public_version.pdf](#)

⁽³⁶⁴⁾ [Die Setup - imec.netzero](#); technologies: N28 (Logic Mobile SoC, 300 mm), Germany - average ; 10 mm die size X and die size Y: yield 85%; IPCC Tier 2C with combustion abatement model

2. Scenario 2 - in which part of the investment is redirected towards a cutting-edge logic fab, with the remainder following the current European mix.

The estimation of additional scope 1 and 2 emissions resulting from future investments for scenario 1 was based on emissions from Global Foundries fab in Dresden in 2023 and taking into consideration the expansion of the current European wafer mix as presented in Annex 4, section 1.2.

Scenario 1:

Total estimated capacity in 2035 in scenario 1/wpy	≈ 22.0 Mio
Estimated total scope 1 emissions in 2035 in scenario 1/ tCO ₂ e	≈ 1 409 859
Estimated total scope 2 (location-based) emissions in 2035 in scenario 1 / tCO ₂ e	≈ 7 146 221
Estimated total scope 2 (market-based) emissions in 2035 in scenario 1 / tCO ₂ e	≈ 6 350 288
Total estimated water withdrawal per year in 2035 in scenario 1/ Mio m ³	≈ 236.5
Estimated total scope 1 emissions in 2035 in scenario 1 using imec.netzero model ⁽³⁶⁵⁾ / tCO ₂ e	1 761 426
Estimated total scope 2 emissions in 2035 in scenario 1 using imec.netzero model ⁽³⁶⁶⁾ / tCO ₂ e	9 247 486
Estimated total scope 3 emissions in 2035 in scenario 1 using imec.netzero model ⁽³⁶⁷⁾ / tCO ₂ e	5 944 813

In scenario 1, the total water withdrawal would increase to 236.5 Mio m³ per year, which is around 8.5% increase in water withdrawal compared to the baseline scenario.

The estimation of additional scope 1 and 2 emissions resulting from future investments for scenario 2 was based on emissions from Global Foundries fab in Dresden in 2023 and as well as scope 1 and 2 emissions of TSMC fabs Japan, also taking into consideration the expansion of mainstream manufacturing capacities and **assuming emergence of leading-edge manufacturing** as presented in Annex 4, Section 1.1 and 1.2.

⁽³⁶⁵⁾ [Die Setup - imec.netzero](#); technologies: N28 (Logic Mobile SoC, 300 mm), Germany - average ; 10 mm die size X and die size Y: yield 85%; IPCC Tier 2C with combustion abatement model

⁽³⁶⁶⁾ [Die Setup - imec.netzero](#); technologies: N28 (Logic Mobile SoC, 300 mm), Germany - average ; 10 mm die size X and die size Y: yield 85%; IPCC Tier 2C with combustion abatement model

⁽³⁶⁷⁾ [Die Setup - imec.netzero](#); technologies: N28 (Logic Mobile SoC, 300 mm), Germany - average ; 10 mm die size X and die size Y: yield 85%; IPCC Tier 2C with combustion abatement model

Scenario 2:

Total estimated capacity in 2035 of mainstream manufacturing in scenario 2 / wpy	≈ 20.4 Mio
Estimated total scope 1 emissions in 2035 of mainstream manufacturing in scenario 2/ tCO ₂ e per year	≈ 1 303 394
Estimated total scope 2 (location-based) emissions in 2035 of mainstream manufacturing in scenario 2/ tCO ₂ e per year	≈ 6 606 576
Estimated total scope 2 (market-based) emissions in 2035 of mainstream manufacturing in scenario 2/ tCO ₂ e per year	≈ 5 870 747
Total estimated water withdrawal per year in 2035 of mainstream manufacturing in scenario 2/ Mio m ³ per year	≈ 222.5
Estimated total scope 1 in 2035 of mainstream manufacturing in scenario 2 using imec.netzero model ⁽³⁶⁸⁾ / tCO ₂ e	1 628 412
Estimated total scope 2 emissions in 2035 of mainstream manufacturing in scenario 2 using imec.netzero model ⁽³⁶⁹⁾ / tCO ₂ e	8 549 164
Estimated total scope 3 emissions in 2035 of mainstream manufacturing in scenario 2 using imec.netzero model ⁽³⁷⁰⁾ / tCO ₂ e	5 495 891

The data to calculate the environmental impact of one leading-edge fab in Europe were based on the emissions reported by TSMC in 2024 and taking into consideration that TSMC's wafer manufacturing capacity in 2024 was 12.9 Mio. ⁽³⁷¹⁾ Using TSMC as a proxy for leading-edge fab emissions in Europe can be justified on technical and operational grounds. Firstly, leading-edge fabs are dominated by process node physics and equipment sets (EUV lithography, advanced deposition/etch, ultra-pure water systems). TSMC operates the same class of tools and nodes expected in Europe, making its per-wafer and per-area intensities a defensible starting point. Secondly, TSMC represents a global efficiency frontier for high-volume advanced manufacturing. Using a best-practice operator avoids underestimating process-intrinsic loads and provides a conservative, performance-anchored baseline for scope 1 (process gases) and scope 2 (electricity demand before grid adjustment). While TSMC's portfolio and scale in Taiwan will differ from a new proposed European site, scale efficiencies mainly affect overhead energy (HVAC, utilities) rather than tool energy per wafer. Additionally, imec.netzero multi-parametric Life-Cycle Assessment model that calculates the environmental footprint for the fabrication of integrated circuits in a high-volume

⁽³⁶⁸⁾ [Die Setup - imec.netzero](#); technologies: N28 (Logic Mobile SoC, 300 mm), Germany - average ; 10 mm die size X and die size Y: yield 85%; IPCC Tier 2C with combustion abatement model

⁽³⁶⁹⁾ [Die Setup - imec.netzero](#); technologies: N28 (Logic Mobile SoC, 300 mm), Germany - average ; 10 mm die size X and die size Y: yield 85%; IPCC Tier 2C with combustion abatement model

⁽³⁷⁰⁾ [Die Setup - imec.netzero](#); technologies: N28 (Logic Mobile SoC, 300 mm), Germany - average ; 10 mm die size X and die size Y: yield 85%; IPCC Tier 2C with combustion abatement model

⁽³⁷¹⁾ esg.tsmc.com/en-US/file/public/2024-TSMC-Sustainability-Report-e.pdf

semiconductor fab was also used and the data achieved are consistent with our own calculations, confirming their credibility and relevance. ⁽³⁷²⁾

Maximum yearly wafer capacity / wpy	12.9 Mio
Scope 1 emissions / tCO ₂ e per year	1 826 000
Scope 2 emissions (location-based) / tCO ₂ e per year	12 674 921
Scope 2 emissions (market-based) / tCO ₂ e per year	10 957 397
Scope 1 emissions / tCO ₂ e/wafer	≈ 0.141550
Scope 2 (location-based) emissions / tCO ₂ e/wafer	≈ 0.9824806
Scope 2 (market-based) emissions / tCO ₂ e/wafer	≈ 0.8493798
Energy consumption / GWh/wafer	≈ 0.00213
Water withdrawal / m ³ /wafer	≈ 9.98
Scope 1 emissions from imec.netzero model / tCO ₂ e/wafer	0.15 ⁽³⁷³⁾
Scope 2 emissions from imec.netzero model / tCO ₂ e/wafer	0.92 ⁽³⁷⁴⁾
Scope 3 emissions from imec.netzero model / tCO ₂ e/wafer	0.48 ⁽³⁷⁵⁾

As modelled in Annex 4, section 1.2, the estimated capacity of a leading-edge fab could reach 25 000 wpm so 300 000 wpy in 2035. Taking this into consideration, total scope 1 and 2 emissions could be calculated based on the TSMC data. ⁽³⁷⁶⁾

Total estimated capacity in 2035 of advanced manufacturing in scenario 2 / wpy	≈ 300 000
Estimated scope 1 emissions of one leading-edge fab in scenario 2 / tCO ₂ e per year	≈ 42 465
Estimated scope 2 (location-based) of one leading-edge fab in scenario 2 / tCO ₂ e per year	≈ 294 766
Estimated scope 2 (market-based) of one leading-edge fab in scenario 2 / tCO ₂ e per year	≈ 254 814
Estimated energy consumption of a one leading-edge / GWh per year	≈ 639

⁽³⁷²⁾ [Die Setup - imec.netzero](#); technologies: N2 (Logic Mobile SoC, 300 mm), Germany -average ; 10 mm die size X and die size Y: yield 85%; IPCC Tier 2C with combustion abatement model

⁽³⁷³⁾ [Die Setup - imec.netzero](#); technologies: N2 (Logic Mobile SoC, 300 mm), Germany -average ; 10 mm die size X and die size Y: yield 85%; IPCC Tier 2C with combustion abatement model

⁽³⁷⁴⁾ [Die Setup - imec.netzero](#); technologies: N2 (Logic Mobile SoC, 300 mm), Germany -average ; 10 mm die size X and die size Y: yield 85%; IPCC Tier 2C with combustion abatement model

⁽³⁷⁵⁾ [Die Setup - imec.netzero](#); technologies: N2 (Logic Mobile SoC, 300 mm), Germany -average ; 10 mm die size X and die size Y: yield 85%; IPCC Tier 2C with combustion abatement model

⁽³⁷⁶⁾ esg.tsmc.com/en-US/file/public/2024-TSMC-Sustainability-Report-e.pdf

Estimated water withdrawal of one leading-edge fab in scenario 2 / Mio m ³ per year	≈ 2.994
Estimated total scope 1 in 2035 one leading-edge fab in scenario 2 using imec.netzero model ⁽³⁷⁷⁾ / tCO ₂ e	45 000
Estimated total scope 2 emissions in 2035 of one leading-edge fab in scenario 2 using imec.netzero model ⁽³⁷⁸⁾ / tCO ₂ e	276 000
Estimated total scope 3 emissions in 2035 of one leading-edge fab in scenario 2 using imec.netzero model ⁽³⁷⁹⁾ / tCO ₂ e	144 000

It should be noted that in Taiwan, the power system remains heavily dependent on fossil fuels—with more than 80 % of generation from gas and coal and an average carbon intensity above ~0.50 tCO₂ per MWh (≈ 500 gCO₂/kWh) in 2024/25 – reflecting limited low-carbon penetration in its grid mix. ⁽³⁸⁰⁾ In contrast, the Europe electricity system, particularly at the EU level, benefits from a far higher share of renewables and nuclear generation combined with aggressive decarbonization policies. As a result, the average carbon intensity of electricity generation in the EU in 2024 was around 0.21–0.24 tCO₂/kWh (≈ 210–240 gCO₂/kWh), less than half the global average and substantially below typical Taiwanese levels. ⁽³⁸¹⁾ This structural difference means that, for identical electricity use, scope 2 emissions (location-based) calculated with European grid factors are often **~40% or more lower** than when Taiwan’s grid mix is applied, a gap driven by Europe’s greater penetration of low-carbon energy sources and ongoing decarbonization of its power sector.

Additionally, it is estimated that **emissions per wafer are expected to increase due to more complex manufacturing processes**. The analysis results indicate an average annual increase of 5.79% in emissions per wafer since 2013. ⁽³⁸²⁾ Assuming that the above analysis was conducted for the year 2025, and accounting for an average annual increase of 5.79% in emissions per wafer, the revised calculations are presented below:

Estimated scope 1 emissions in 2035 for a leading-edge fab in scenario 2 assuming 5.79% annual increase / tCO ₂ e	≈ 74 555
Estimated scope 2 (location-based) of a leading-edge fab in scenario 2 assuming 5.79% annual increase / tCO ₂ e	≈ 517 515
Estimated scope 2 (location-based) of a leading-edge fab in scenario 2 assuming 5.79% annual increase adjusted for European electricity mix /	≈ 310 509

⁽³⁷⁷⁾ [Die Setup - imec.netzero](#); technologies: N2 (Logic Mobile SoC, 300 mm), Germany -average ; 10 mm die size X and die size Y: yield 85%; IPCC Tier 2C with combustion abatement model

⁽³⁷⁸⁾ [Die Setup - imec.netzero](#); technologies: N2 (Logic Mobile SoC, 300 mm), Germany -average ; 10 mm die size X and die size Y: yield 85%; IPCC Tier 2C with combustion abatement model

⁽³⁷⁹⁾ [Die Setup - imec.netzero](#); technologies: N2 (Logic Mobile SoC, 300 mm), Germany -average ; 10 mm die size X and die size Y: yield 85%; IPCC Tier 2C with combustion abatement model

⁽³⁸⁰⁾ [Republic of China \(Taiwan\) Electricity Generation Mix 2025 | Low-Carbon Power Data](#)

⁽³⁸¹⁾ [Global Electricity Review 2025 | Ember](#)

⁽³⁸²⁾ Interface (2024). Chip Production’s Ecological Footprint: Mapping Climate and Environmental Impact. [Chip Production’s Ecological Footprint: Mapping Climate and Environmental Impact](#)

tCO ₂ e	
Estimated scope 2 (market-based) of a leading-edge fab in scenario 2 assuming 5.79% annual increase / tCO ₂ e	≈ 447 372
Estimated total scope 1 emissions in 2035 of one leading-edge fab in scenario 2 using imec.netzero model ⁽³⁸³⁾ assuming 5.79% annual increase / tCO ₂ e	79 005
Estimated total scope 2 emissions in 2035 of one leading-edge fab in scenario 2 using imec.netzero model ⁽³⁸⁴⁾ assuming 5.79% annual increase / tCO ₂ e	484 568
Estimated scope 2 of a leading-edge fab in scenario 2 assuming 5.79% annual increase adjusted for European electricity mix using imec.netzero model ⁽³⁸⁵⁾ / tCO ₂ e	290 740
Estimated total scope 3 emissions in 2035 of one leading-edge fab in scenario 2 using imec.netzero model ⁽³⁸⁶⁾ assuming 5.79% annual increase / tCO ₂ e	252 818

	Total scope 1 emissions in 2035 under Scenario 2 / tCO₂e	Total scope 2 emissions (location-based) in 2035 under Scenario 2 / tCO₂e	Total scope 3 emissions in 2035 under Scenario 2 / tCO₂e
Mainstream nodes	1 303 394 - 1 628 412	6 606 576 - 8 549 164	5 495 891
Advanced nodes	74 555 – 79 005	290 740 – 310 509	252 818
Total	1 377 949 – 1 707 417	6 918 085 – 8 839 904	5 748 709

The estimated water consumption in scenario 2 under PO2 is around 222.3 Mio m³ per year. This estimation is on the lower end as it based on water consumption of a TSMC fab in Taiwan, where there is a high water scarcity and therefore a stronger emphasis on water reuse

⁽³⁸³⁾ [Die Setup - imec.netzero](#); technologies: N2 (Logic Mobile SoC, 300 mm), Germany -average ; 10 mm die size X and die size Y: yield 85%; IPCC Tier 2C with combustion abatement model

⁽³⁸⁴⁾ [Die Setup - imec.netzero](#); technologies: N2 (Logic Mobile SoC, 300 mm), Germany -average ; 10 mm die size X and die size Y: yield 85%; IPCC Tier 2C with combustion abatement model

⁽³⁸⁵⁾ [Die Setup - imec.netzero](#); technologies: N2 (Logic Mobile SoC, 300 mm), Germany -average ; 10 mm die size X and die size Y: yield 85%; IPCC Tier 2C with combustion abatement model

⁽³⁸⁶⁾ [Die Setup - imec.netzero](#); technologies: N2 (Logic Mobile SoC, 300 mm), Germany -average ; 10 mm die size X and die size Y: yield 85%; IPCC Tier 2C with combustion abatement model

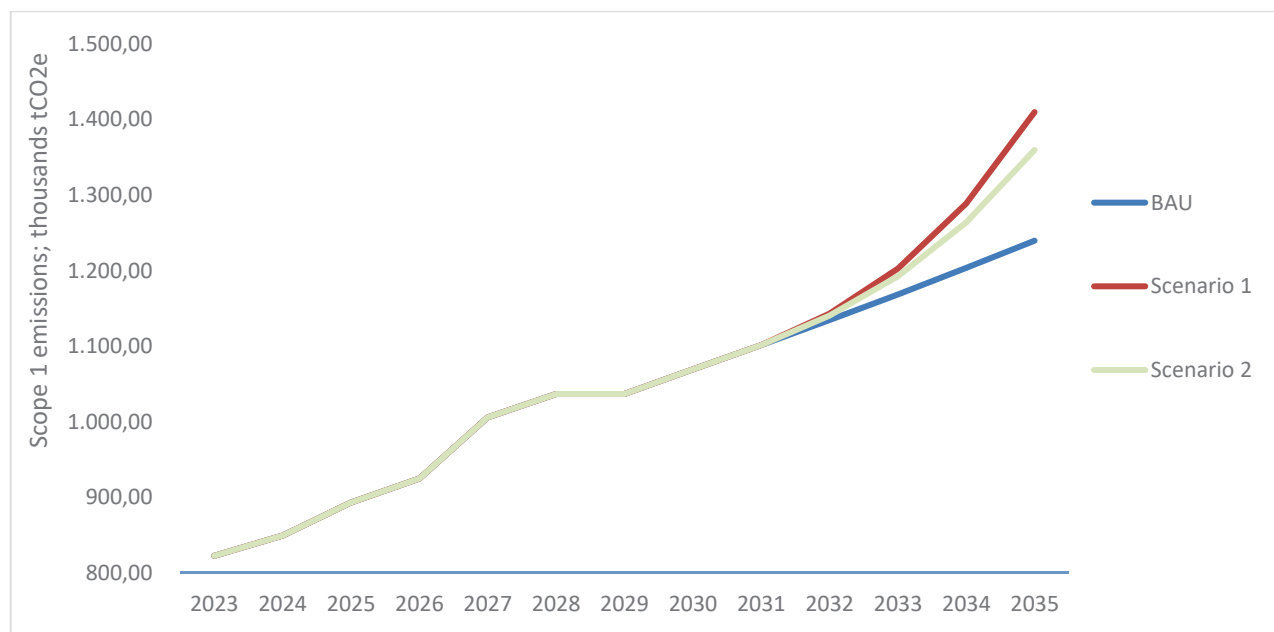
and recycling (80% in Taiwan), while fabs in Europe typically have lower recycling rates (10%–14%).⁽³⁸⁷⁾ This suggests that water consumption in Europe will be higher however the adoption of advanced water management technologies, including recycling and advanced treatment, can improve competitiveness, circularity and water efficiency in semiconductor production.

Furthermore, if scenario 2 of Policy Option 2 would take place, the increase in the use of materials would also happen. Leading-edge chips – especially those less than 10 nm – and advanced packaging (AP) require increasingly complex manufacturing methods, which increases the demand for the materials that enable these processes and create the finished products. As semiconductor technology progresses to use smaller nodes, the number of mask layers – used as part of the process that defines and fills conductive channels in the chip – for producing a single wafer increases disproportionately. For example, while a 65 nm process node wafer may require about 40 mask layers to complete, a leading-edge 5- or 3-nm process node requires up to 110 mask layers.⁽³⁸⁸⁾

Beyond node size, AP is also increasing material consumption. Many AP technologies use interposers or base dies to connect multiple chips, require carrier wafers as part of the manufacturing process, or include an increasing number of interconnects (through-silicon via, for example). All these incremental process steps require more materials than mature technologies do.

The shift to using more mask layers and consuming additional materials as part of AP processes could increase Europe’s total material consumption by as much as 65% and many of these materials may need to come from international markets.⁽³⁸⁹⁾

Figure 21. Projected emissions under difference scenarios. *Source: prepared by the authors.*



⁽³⁸⁷⁾ Interface (2024). Chip Production’s Ecological Footprint: Mapping Climate and Environmental Impact. [Chip Production’s Ecological Footprint: Mapping Climate and Environmental Impact](#)

⁽³⁸⁸⁾ [Semiconductors have a big opportunity—but barriers to scale remain | McKinsey](#)

⁽³⁸⁹⁾ [Semiconductors have a big opportunity—but barriers to scale remain | McKinsey](#)

4.1.6. Costs of environmental impacts

From 2015 to 2025 the EU ETS carbon prices have been fluctuating a lot, ranging from very low prices, mostly below €10 / tCO₂ between 2015-2017, to €60–90 between 2022 -2023, before easing somewhat in 2024 – 2025 (€60 – €90 / tCO₂). Looking ahead, most outlooks point to a structurally tighter market with increasing scarcity of allowances, declining free allocation, and stricter caps, implying a renewed upward trend over the 2030s, with many analyst scenarios placing average EU ETS prices by 2035 well above today's levels - often in the range of roughly €190 – 300 per tonne of CO₂, depending on policy ambition, economic conditions, and technological progress. ⁽³⁹⁰⁾

Therefore, taking into consideration aggregated scope 1 and 2 emissions (location-based), environmental costs for each policy option in 2035 could be predicated in the ranges as follows:

- Baseline scenario BAU = €1.459 – €2.256 bln
- Policy Option 1 = €1.531 – €2.368 bln
- Policy Option 2, scenario 1 = €1.659 – €2.566 bln
- Policy Option 2, scenario 2 = €1.621 – €2.507 bln

The other possibility is to use the True Price method. This method developed the principles and methodology to monetise a wide set of social and environmental costs. ⁽³⁹¹⁾ For environmental impacts, monetisation factor of €0.163 /kgCO₂e was used describing restoration cost which expresses the abatement cost for achieving the policy targets of reducing GHG emissions to meet the 2-degree target as set in the Paris Agreement. ⁽³⁴⁸⁾ Using this factor, restoration cost for different policy options in 2035 can be estimated:

- Baseline scenario BAU = €1.226 bln
- Policy Option 1 = €1.286 bln
- Policy Option 2, scenario 1 = €1.394 bln
- Policy Option 2, scenario 2 = €1.385 bln

⁽³⁹⁰⁾ [EU ETS Market Outlook 1H 2024: Prices Valley Before Rally | BloombergNEF](#)

⁽³⁹¹⁾ [MONETISATION FACTORS FOR TRUE PRICING - True Price](#)

5. COMPARATIVE ANALYSIS OF INVESTMENT, CAPACITY AND EMPLOYMENT OUTCOMES RELATED TO STRATEGIC PROJECTS

Modelling approach and baseline assumptions

The modelling relies on an empirical bottom-up calibration using first-of-a-kind (FOAK) semiconductor manufacturing projects supported to date in the EU. These projects constitute the only observable set of investments for which reasonably consistent information is available on:

- total investment volumes (public and private),
- planned wafer fabrication capacity, and
- announced direct employment at steady state.

The reference sample therefore reflects revealed investment behaviour under EU and Member State support schemes, rather than hypothetical or benchmarked fab configurations. This approach is consistent with the Better Regulation principle of grounding quantitative analysis in observed evidence where available, while acknowledging that the sample remains limited in size and heterogeneous in technological scope.

To ensure comparability across projects of different scale and technology profiles, the available FOAK data were normalised into intensity ratios, expressed as:

- wafer capacity per EUR billion of total investment; and
- direct employment per EUR billion of total investment.

Using the consolidated FOAK figures provided:

- total investment: EUR 31.23 billion;
- total planned new jobs: approximately 5,700; and
- total planned new wafer capacity: approximately 2.08 million wafers per year (around 173,000 wafers per month).

From these figures, the model derives average investment intensities that serve as proportional scaling parameters. These parameters implicitly capture the current European technology mix, capital intensity, and labour productivity embedded in recent supported projects.

The derived intensity ratios are then applied proportionally to the assumed EUR 40 billion investment envelope associated with strategic semiconductor projects, comprising public support and crowd-in private investment. The model assumes that:

- the full envelope translates into realised manufacturing investment;
- investment efficiency, in terms of capacity and employment per euro invested, remains constant relative to the FOAK reference sample; and
- no major structural break occurs in technology choice, production scale, or automation intensity relative to recent projects.

Under these assumptions, additional wafer capacity and employment are estimated by scaling up the FOAK-based ratios to the larger investment envelope. This proportional approach ensures internal consistency between observed projects and forward-looking estimates, while deliberately avoiding optimistic assumptions about learning effects or step-changes in productivity.

The modelling approach is intentionally conservative and subject to several limitations:

- FOAK projects may not yet reflect steady-state performance, as ramp-up periods and learning effects are ongoing.
- Publicly announced employment and capacity figures may change as projects progress.
- The sample does not include a fully operational leading-edge logic fab in Europe, limiting direct observability for advanced-node scenarios.

The modelling of Strategic Projects impacts relies on a total investment envelope of **EUR 40 billion**, comprising **EUR 15 billion in public support** (Competitiveness Fund, State aid, including Member State contributions) and **EUR 25 billion in private investment**. This envelope is assumed to be fully allocated to new manufacturing capacity and associated on-site activities.

Two scenarios are assessed:

- **scenario 1**, in which new investments broadly replicate the current European wafer mix and technology profile (i.e. mostly on mainstream chips); and
- **scenario 2**, in which part of the investment is redirected towards a cutting-edge logic fab, with the remainder following the current European mix.

Pessimistic scenario: continuation of the current European wafer mix

The pessimistic scenario assumes that new investments follow the **existing structure of semiconductor manufacturing in Europe**, characterised by a dominance of mature nodes and specialty technologies. The allocation of funding across technology segments is derived from **first-of-a-kind (FOAK) investments observed to date**, and the same proportional distribution is applied to the new EUR 40 billion envelope.

This scenario therefore reflects a continuation of current strengths, rather than a structural shift towards advanced logic manufacturing.

Employment and capacity impacts

Under this scenario, the model estimates:

- **Total new jobs: 7,301**
- **Total new wafer capacity: 2,660,263 wafers per year**, equivalent to
- **221,689 wafers per month**

Indirect employment

The evidence from the Intel Magdeburg case and the wider literature suggests that **no single indirect employment multiplier is universally appropriate** for semiconductor investments. Instead, the choice depends on the **purpose of the modelling** and the **degree of conservatism required**. **High-end estimates, such as the SIA multiplier of 6.7,** ⁽³⁹²⁾ reflect the full ecosystem effects observed in the US, where the multiplier captures a mature and highly localised semiconductor ecosystem, including upstream suppliers, specialised services, and downstream activities. There, semiconductor supply chains are deeper, labour mobility is

⁽³⁹²⁾ The US semiconductor industry workforce and how federal incentives will increase domestic jobs – SIA, Oxford Economics - <https://www.semiconductors.org/chipping-in-sia-jobs-report/>

higher, and a large share of upstream and downstream activities is domestic. Applying such a multiplier mechanically in an EU context risk **overestimating indirect and induced employment**, particularly in regions with tight labour markets and internationally fragmented value chains. As such, the SIA figure is best used as an **upper-bound reference or sensitivity case**, rather than a central assumption.

For a **core or central modelling assumption** under the EU Chips Act, a **more conservative multiplier** is warranted. **Benchmarks such as the UNIDO ⁽³⁹³⁾ manufacturing multiplier (around 2.2 additional jobs per direct job)** provide a lower bound that is consistent with open economies and globalised supply chains, where a significant share of indirect effects is captured outside the host region through imports and international value chains, although not specific for the semiconductor industry. A pragmatic approach is therefore to use UNIDO multiplier as a proxy for a lower bound of potential indirect and induced jobs per direct job, reflecting partial but not full localisation of spillovers.

Therefore, under the pessimistic scenario, the level of indirect jobs created is assumed to be:

- Lower end (UNIDO multiplier): $7,301 * 2.2 = 16,061$
- Upper end (downwards adjusted SIA multiplier): $7,301 * 5 = 36,503$

These two benchmarks delimit a plausible range for indirect employment effects in the EU context.

Revenue impacts

To estimate revenues, the model applies a proportional approach based on the current relationship between **EU wafer capacity** and **device-level revenue**. Using an estimated total EU capacity of **1.07 million wafers per month** and reported EU semiconductor device revenue of **EUR 50.5 billion**, an average revenue per wafer is derived and applied to the incremental capacity.

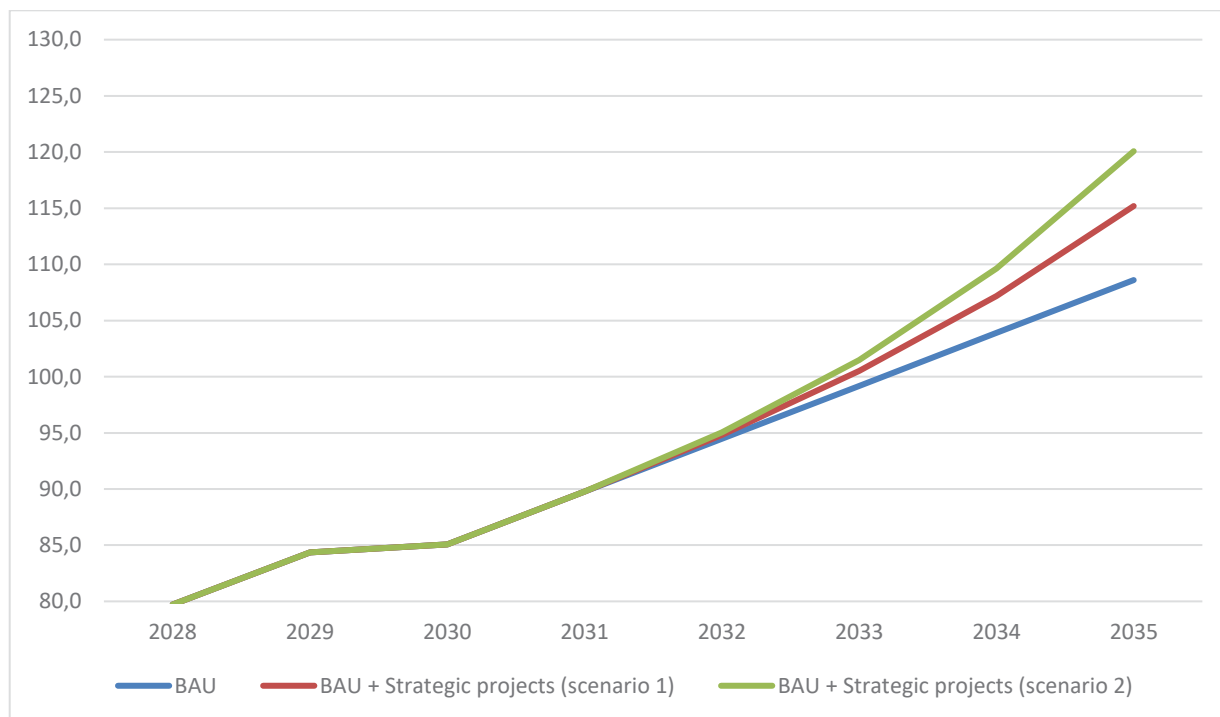
On this basis, the pessimistic scenario yields estimated additional annual revenue of approximately:

- **EUR 6.6 billion**

This outcome reflects the relatively low average selling prices associated with mature-node production, even at substantial volumes.

Figure 22. Projected revenues due to strategic projects. *Source: prepared by the authors.*

⁽³⁹³⁾ The multiplier effect of industrial jobs – United Nation Industrial Development Organisation (UNIDO)



Optimistic scenario: assuming emergence of leading-edge manufacturing

The second scenario assumes a **more strategic allocation of investment**, in which:

- **EUR 25 billion** (indicative cost of a leading-edge fab) is dedicated to the construction of a **cutting-edge logic facility**, and
- the remaining **EUR 15 billion** is invested in line with the current European wafer mix, using the same assumptions as in the pessimistic scenario.

According to the Joint Research Centre, drawing on BCG analysis ⁽³⁹⁴⁾, a state-of-the-art semiconductor fab of standard capacity requires roughly USD 20 billion for advanced logic or memory production, including land, buildings and equipment. Another relevant reference is the Rapidus project in Japan, which targets 2-nanometre production and is reported to involve total investment of around USD 36 billion (approximately EUR 30 billion) ⁽³⁹⁵⁾, covering construction, equipment, and extensive process development. That figure reflects significant upfront R&D expenditure, notably through Rapidus' strategic collaboration via NanoIC pilot line hosted by imec ⁽³⁹⁶⁾. Given Europe's existing access to advanced research and pilot-line infrastructure through imec and related ecosystems, a lower all-in cost of EUR 25 billion for a comparable European fab is considered a reasonable assumption.

This scenario reflects a deliberate policy choice to use public support to **alter the technological composition** of EU semiconductor manufacturing, rather than only expanding existing segments.

Leading-edge fab assumptions:

⁽³⁹⁴⁾ Bonnet, P., Ciani, A., Molnar, J., & Nardo, M. (2025). *EU's strengths and weaknesses in the global semiconductor sector* (EUR 40253 EN). Luxembourg: Publications Office of the European Union. <https://doi.org/10.2760/6302476>

⁽³⁹⁵⁾ <https://www.electronicweekly.com/news/business/rapidus-picks-hokkaido-for-36bn-2nm-fab-2023-02/>

⁽³⁹⁶⁾ <https://www.imec-int.com/en/press/rapidus-japans-newly-founded-chip-manufacturer-joins-imecs-core-partner-program>

The leading-edge component is modelled using conservative assumptions drawn from recent greenfield announcements:

- **Direct employment: 2,000 jobs**, based on announced figures for comparable projects in the EU (e.g. ESMC).
- **Capacity: 25,000 wafers per month**, consistent with public announcements for new advanced fabs (e.g. Rapidus³⁹⁷).
- **Average wafer revenue: EUR 30,000 per wafer**, reflecting industry estimates for advanced-node foundry pricing (e.g. TSMC³⁹⁸)

These assumptions are indicative and reflect current industry benchmarks rather than firm contractual prices.

Combined impacts (leading-edge plus mature mix)

When combining the leading-edge investment with the remaining EUR 15 billion allocated to the current mix, the model estimates:

- **Total new direct jobs: 4,738**
- **Total new indirect jobs: 10,423 – 23,690**
- **Total new wafer capacity: 108,133 wafers per month**
- **Total additional annual revenue: EUR 11.5 billion**

Although total employment is lower than in the first scenario, this reflects the **higher capital intensity and automation** of leading-edge manufacturing rather than weaker economic performance.

Fiscal returns

We estimate the fiscal revenues generated once the new capacity is operational. Fiscal returns depend on the **additional value added** generated by ongoing production. To avoid overstating fiscal impacts by applying tax rates to turnover, the analysis converts additional semiconductor revenues into **additional gross value added (GVA)** using an empirically grounded value-added share.

Using OECD STAN data for EU Member States (ISIC Rev.4 **C26: manufacture of computer, electronic and optical products**) over 2020–2023, **the ratio of Value added to Output averages 34%**. This provides a transparent and robust benchmark for converting additional device revenues into additional value added. Accordingly, additional operational value added is estimated as:

Additional GVA = 0.34 × additional annual device revenue

This step ensures consistency with national accounts concepts and avoids double counting, as only the domestically generated component of revenue is treated as the relevant economic base for fiscal analysis.

⁽³⁹⁷⁾ <https://www.digitimes.com/news/a20250718PD228/rapidus-production-2nm-2027-chips.html#:~:text=Toward%20a%20commercial%20offering,Mayor%20Ryuichi%20Yokota%20of%20Chitose>.

⁽³⁹⁸⁾ <https://bits-chips.com/article/tsmc-to-raise-advanced-process-prices-by-up-to-10-percent/?utm>

Based on the data provided in JRC (2025) ⁽³⁹⁹⁾ and OECD Tax Revenue Database ⁽⁴⁰⁰⁾ we know that an average share of value added captured as fiscal revenue is between 16% - 17% (assume 16.5% as a central point). This means that an annual fiscal return of:

- In pessimistic case: annual direct tax revenue would be around EUR 380 million;
- In optimistic case: annual direct tax revenue would be around EUR 662 million.

6. INNOVATION-ORIENTED PUBLIC PROCUREMENT AND FIRM INNOVATION OUTCOMES: EVIDENCE FROM THE LITERATURE

A growing empirical literature shows that public procurement can function as an effective **demand-side innovation instrument**, particularly when public buyers act as technologically sophisticated lead customers and require first-of-a-kind or non-off-the-shelf solutions. In such contexts, procurement influences firm behaviour not primarily through financial transfers, but by exposing suppliers to advanced technical requirements, intensive buyer–supplier interaction, and strong signalling effects towards downstream markets.

Evidence from procurement by large research infrastructures illustrates this mechanism clearly. Firm-level econometric analysis of CERN procurement shows that suppliers awarded CERN contracts experience a statistically significant increase in their likelihood of becoming innovators, with estimated effects in the order of around **10–20 percentage points** relative to otherwise comparable firms. The underlying channel operates through capability upgrading and learning-by-doing induced by demanding specifications, co-development processes, and reputational benefits associated with supplying a globally recognised scientific buyer. These effects are particularly salient for firms close to an innovation threshold, suggesting that innovation-oriented procurement can help firms cross barriers related to certification, technical validation, and market credibility ⁽⁴⁰¹⁾.

Complementary large-sample evidence confirms that public procurement is associated with measurable innovation outcomes at firm level. Using Flash Eurobarometer data covering **28 EU Member States, Switzerland, and the US**, and a sample of **6,719 innovative firms** observed between **2011 and 2014**, econometric analysis combining cross-sectional regression with propensity score matching finds that participation in public procurement significantly increases the probability of innovation. Specifically, procurement participation raises the likelihood of introducing **product innovation by 10.6 percentage points in goods and 12.4 percentage points in services**, while supply-side R&D policy measures show no statistically significant effect on product innovation in either sector. For **process innovation**, procurement increases adoption probability by **6.3 percentage points**, while public R&D support raises the likelihood of process innovation by **7.2 percentage points**, indicating a degree of complementarity between demand-side and supply-side instruments for production upgrading ⁽⁴⁰²⁾.

⁽³⁹⁹⁾ Bonnet, P., Ciani, A., Molnar, J., & Nardo, M. (2025). *EU's strengths and weaknesses in the global semiconductor sector* (EUR 40253 EN). Luxembourg: Publications Office of the European Union. <https://doi.org/10.2760/6302476>

⁽⁴⁰⁰⁾ *OECD Tax Revenue Statistics: Comparative Tables and Tax Revenue Database (Edition 2024)*. Paris: OECD Publishing. Available at <https://stats.oecd.org/Index.aspx?DataSetCode=REV>

⁽⁴⁰¹⁾ Andrea Bastianin, Paolo Castelnovo, Lorenzo Zirulia, Overcoming the innovation threshold through innovative public procurement: evidence from CERN, *Industrial and Corporate Change*, Volume 34, Issue 5, October 2025, Pages 871–900, <https://doi.org/10.1093/icc/dtaf004>

⁽⁴⁰²⁾ Dragana Radicic, Effectiveness of public procurement of innovation versus supply-side innovation measures in manufacturing and service sectors, *Science and Public Policy*, Volume 46, Issue 5, October 2019, Pages 732–746, <https://doi.org/10.1093/scipol/scz026>

Beyond innovation outcomes, recent evidence also highlights broader economic effects of public procurement that are relevant for high-capital-intensity sectors. Budrys (2025) ⁽⁴⁰³⁾, using a novel dataset linking US federal procurement data with firm financials, stock market information, analyst forecasts, and credit default swaps, identifies competitive procurement awards as largely unanticipated firm-level demand shocks. The results show that winning a procurement contract leads to persistent increases in sales and profits over several years, with sales rising by around 0.20 dollars per dollar of government obligations on impact and peaking at approximately 0.50 dollars after nine quarters, while profits increase by about 0.10 dollars per dollar of obligations, corresponding to a 4–5 percentage point increase in profitability. Procurement also stimulates investment, with capital expenditure increasing cumulatively by around 0.21 dollars per dollar of obligations over a three-year horizon, indicating medium-term capacity expansion rather than short-term scaling alone. Importantly, procurement contracts generate a risk-mitigation effect, reducing perceived uncertainty and default risk, particularly during periods of tight financial conditions: realised stock-return volatility declines by up to 0.5–1%, analyst forecast dispersion falls by around 4–5%, and credit default swap spreads decline by up to 5% following contract awards. Overall, these findings suggest that public procurement can act not only as a source of demand, but also as a stabilising mechanism that improves firms’ resilience and investment incentives, with clear relevance for sectors such as semiconductors characterised by large fixed costs and long investment cycles.

The literature suggests that innovation-oriented public procurement can influence firm behaviour through multiple channels: stimulating product and process innovation, supporting capability upgrading, improving revenue stability, and reducing risk. These mechanisms are highly relevant for the **EU semiconductor ecosystem**, which is characterised by high entry barriers, long qualification cycles, large sunk costs, and strong dependence on reference customers. In this context, public procurement under the EU Chips Act could complement supply-side measures by creating early, credible demand for strategically important technologies, such as trusted chips, advanced packaging solutions, or specialised components for defence, space, health, and critical infrastructure. By acting as a technologically demanding lead customer, the public sector could help European semiconductor firms and suppliers cross innovation and commercialisation thresholds, reinforce the effectiveness of R&D and state aid instruments, and contribute to longer-term resilience and competitiveness of the EU Chips industry.

⁽⁴⁰³⁾ Budrys, Z. (2025). *Consumer of last resort: Government procurement, firm-level evidence and the macroeconomy* (Working Paper). Retrieved from https://zymantasbudrys.com/wp-content/uploads/2022/10/ZymantasBudrys_JMP_LastConsumer.pdf

ANNEX 5: COMPETITIVENESS CHECK

1. OVERVIEW OF IMPACTS ON COMPETITIVENESS

Dimensions of Competitiveness	Impact of the initiative (++ / + / 0 / - / -- / n.a.)	References to sub-sections of the main report or annexes
Cost and price competitiveness	+	Discussed in Section 6.2.1 which describes reductions in investment risk, lower capital costs via EU co-funding, faster permitting, improved utilisation, and pricing stability
International competitiveness	++	Discussed in Section 6.2.1 which sets out Strategic Projects, sovereign manufacturing capacity, boutique leading-edge foundry example, cross-border clustering, and resilience gains.
Capacity to innovate	++	Discussed in Section 6.2.16 which describes how Strategic Projects enable industrial deployment of publicly funded research, how innovation procurement and thematic grand challenges stimulate high-risk technological development, and how strengthened design capabilities support long-term innovation.
SME competitiveness	++	Discussed in Section 6.2.1.7 which describes impact of incentives for stronger demand pull, anchor customers via innovation procurement, improved access to manufacturing and design capabilities.

2. SYNTHETIC ASSESSMENT

Policy Option 2 (“Strategic sovereignty”) is expected to have strong overall positive impacts on the competitiveness of the European semiconductor ecosystem, building on and surpassing the effects of Policy Option 1. These impacts derive from Strategic Projects, targeted demand-side instruments, enhanced supply chain transparency, and combined horizontal measures (skills, faster permitting procedures, Semiconductor Regions of Excellence). The initiative delivers competitiveness effects across all four dimensions as follows:

Cost and price competitiveness (+) improves moderately, driven by reduced investment risk, lower capital costs through EU co-funding, and more predictable utilisation enabled by innovation procurement. Structural cost disadvantages such as energy and labour costs remain, limiting the scale of improvements.

International competitiveness (++) strengthens substantially. Strategic Projects expand Europe's manufacturing and design capabilities, reduce dependencies on a small number of non-EU suppliers, and support the emergence of advanced semiconductor manufacturing capacity, including for AI chips. The balanced reinforcement approach supported by the European Competitiveness Fund ensures that both leading-edge and upstream segments can be strengthened, positioning the EU more strongly in global markets.

Capacity to innovate (++) is significantly enhanced through measures that support industrial deployment of research, strengthen design capabilities, and stimulate high-risk technological development via innovation procurement and thematic challenges. These mechanisms broaden opportunities for innovation and increase Europe's ability to compete in next-generation semiconductor technologies.

SME competitiveness (++) is expected to improve strongly. Strategic Projects and demand-side measures create new market opportunities for SMEs, particularly fabless design firms and specialised suppliers. Exemptions from mandatory reporting and simplification measures under REFIT reduce administrative burdens and support SME scaling.

3. COMPETITIVE POSITION OF THE MOST AFFECTED SECTORS

Semiconductor manufacturing, advanced packaging and chip design segments of the semiconductor value chain benefit directly. Strategic Projects strengthen Europe's capacity across leading-edge manufacturing, mature-node production, advanced packaging and design capabilities. Enhanced scale, improved investment certainty and stronger value-chain integration increase global competitiveness and reduce vulnerabilities to foreign supply disruptions.

Fabless design firms and semiconductor SMEs also experience substantial gains. Increased demand for specialised inputs, early revenue opportunities through innovation procurement, and access to advanced manufacturing and prototyping facilities improve the market position of SMEs. Exemptions from mandatory reporting obligations and streamlined procedures further support development and scaling.

Upstream suppliers, including equipment manufacturers, materials providers and speciality chemical firms, benefit from increased demand associated with new Strategic Projects and deeper integration across the European value chain. Predictable investment flows reduce uncertainty and encourage further expansion of upstream capacity within the Union.

Downstream user industries such as automotive, industrial equipment, telecommunications, cloud/AI infrastructure and defence gain from improved supply stability and resilience. Reduced exposure to global semiconductor disruptions strengthens the competitiveness of these sectors, which were heavily affected during past shortages. The availability of advanced and sovereign semiconductor capacity supports technological upgrading and adoption of AI-enabled systems.

ANNEX 6: OVERVIEW OF IMPACTS ON SMEs

Relevance for SMEs
Based on the SME filter and the ISG discussion, this initiative is relevant/highly relevant for SMEs ⁴⁰⁴
(1) IDENTIFICATION OF AFFECTED BUSINESSES AND ASSESSMENT OF RELEVANCE
Are SMEs directly affected?
The semiconductor value chain in Europe is characterised by a high concentration of small and medium-sized enterprises, particularly in design, specialised manufacturing services and upstream supply segments. Policy Option 2 introduces measures such as Strategic Projects, the broadened scope of First-of-a-Kind support, and innovation procurement that directly involve these SMEs as project beneficiaries, suppliers, or suppliers for the increased demand for advanced semiconductor technologies. Directly affected SMEs operate primarily in the following sectors: • Semiconductor design and IP services, including fabless design houses, which in Europe consist almost entirely of SMEs and are explicitly targeted through Strategic Projects and innovation procurement. • Specialised semiconductor supply-chain segments, such as equipment suppliers, advanced materials and chemicals producers, and niche tool manufacturers, which provide critical inputs to potential Strategic Projects and benefit from value-chain strengthening measures. • Advanced packaging, testing and related specialised manufacturing services, where many actors are SMEs supplying low-volume or high-reliability solutions that are with scope of Strategic Projects. • Semiconductor R&D service providers and pilot-line operators, including SMEs offering prototyping, design enablement and verification services linked to the deployment of Chips Act pilot lines. SMEs in these segments are therefore directly within scope of the preferred option, either as beneficiaries of new market opportunities or as participants in supported projects.
Estimated number of directly affected SMEs
Based on the quantitative mapping of firms across the European semiconductor value chain, the initiative is expected to directly affect a substantial share of the 1,481 companies identified in the ecosystem. As shown in the sector distribution (Chemicals and gases;

⁽⁴⁰⁴⁾ <https://ec.europa.eu/docsroom/documents/63274>

materials; equipment; wafers; EDA; fabless; IDM; manufacturing; OSAT; PCB; services; end users), SMEs constitute approximately 69% of all firms active in the European semiconductor value-chain ⁽⁴⁰⁵⁾.

This corresponds to around 1,020 directly affected SMEs across the Union.

Estimated number of employees in directly affected SMEs

Using the mapping of 1,481 companies across semiconductor-relevant value-chain segments, of which approximately 1,020 are SMEs (69%), it is possible to estimate the number of employees in SMEs directly affected by the preferred option (Policy Option 2).

While official, segment-specific SME employment statistics are not available at EU level, we assume that the average numbers of employees working in European SMEs are the following:

- 15–30 employees in specialised materials SMEs;
- 30–80 employees in fabless design and EDA SMEs;
- 50–120 employees in equipment-supplier SMEs;
- 40–100 employees in packaging, testing, prototyping and manufacturing-service SMEs;
- 25–50 employees in semiconductor-related service and support SMEs.

Applying these conservative ranges to the SME distribution across segments results in an estimated 45,000–65,000 employees working in SMEs directly and indirectly affected by the preferred option.

(2) CONSULTATION OF SME STAKEHOLDERS

How has the input from the SME community been taken into consideration?

Inputs were gathered through multiple channels, including an Open Public Consultation (OPC) (103 responses, of which 21% were small enterprises and 22% medium enterprises). A Call for Evidence (209 responses, including 16% small and 14% micro enterprises), targeted surveys (64 respondents), expert interviews (14 stakeholders), and 17 thematic workshops including a dedicated SMEs and start-ups workshop.

The consultation strategy achieved robust representation from the SME ecosystem. Smaller entities accounted for **43% of respondents to the Open Public Consultation, 48% of the Call for Evidence, and 60% of private sector respondents** in the targeted surveys. These quantitative inputs were complemented by qualitative insights gathered through interviews with investors and industry associations, as well as a dedicated workshop for SMEs and start-ups.

The design of Policy Option 2 was significantly shaped by this feedback. The input specifically addressed operational barriers, the scope of support, and the mitigation of administrative

⁽⁴⁰⁵⁾ Survey data collected by DG CNECT from Member States in the context of the Chips Act Pillar III mapping and elaborated by the JRC.

burdens.

First, regarding **operational barriers**, the consultation revealed that the mechanisms to access support were not fully understood. Although targeted survey results showed that 70% of respondents indicated clarity on the overall goals of the initiative, **none of the industry users surveyed reported clarity on the specific application procedures**. In the OPC, fabless companies identified limited access to venture capital as their most critical obstacle (78%), followed by the high cost of Electronic Design Automation (EDA) tools (67%). Interview and workshop participants described pilot line access as unclear and costly for early-stage innovators. This evidence justified the inclusion of measures in Policy Option 2 to streamline application procedures and accelerate the operationalisation of the Design Platform and competence centres.

Second, regarding the **scope of support**, stakeholders from the PCB, equipment, and chip design sectors argued that the original “First-of-a-Kind” (FOAK) criteria favoured large integrated manufacturers. Submissions to the Call for Evidence from business associations specifically called for broader eligibility to include advanced packaging and design. In direct response to this input, Policy Option 2 includes an expanded FOAK definition that explicitly covers advanced packaging and design. These are segments where European SMEs hold significant potential yet face scaling challenges.

Third, the proposal addresses SME concerns regarding **administrative burden**. In the targeted surveys, support for the monitoring coordination mechanisms was notably lower among supply chain stakeholders (62%) compared to national authorities (88%). Interviewees emphasised that complex procedures made it challenging for smaller firms to benefit without external consultancy support. Consequently, the revised monitoring mechanism maintains a strict exemption for SMEs from mandatory information requests.

Are SMEs’ views different from those of large businesses?

The consultation data reveals distinct divergences between SMEs and large enterprises when it comes to investment priorities, sensitivity to administrative burden, and the preferred scope of support.

The primary divergence concerns **investment priorities**. For SMEs, particularly fabless companies, survival depends on access to finance and shared infrastructure. **OPC** data shows that **78%** of these firms cited limited access to risk capital as a critical barrier. Conversely, large foundry and integrated device manufacturers (IDMs) responding to the **OPC** rated the existing FoaK framework as satisfactory or neutral (44%), focusing their feedback primarily on approval timelines rather than funding availability. **Interview** stakeholders confirmed this, noting that while the EIC’s Chips Fund was effective for deep-tech start-ups, large manufacturers focused on broader framework conditions.

A second major difference concerns **sensitivity to governance and burden**. SMEs and research organisations (RTOs) expressed significantly higher scepticism regarding the effectiveness of governance mechanisms compared to large firms. In a targeted survey, RTOs reported the lowest levels of positive effects from the intervention (35-41%) and rated administrative efficiency as “very ineffective” (18-29%), nearly double the rate of national authorities. This contrasts with the views of large incumbents, who typically possess dedicated compliance

departments to navigate complex requirements.

Finally, views differed on the **targeted scope of EU intervention**. In the OPC, large end-user industries and IDMs overwhelmingly supported subsidies for building large-scale manufacturing facilities (**89% support**). In contrast, input from the Call for Evidence and workshops shows that SMEs and stakeholders in the equipment and design sectors argued that the architecture was misaligned with their needs.

(3) ASSESSMENT OF IMPACTS ON SMEs ⁽⁴⁰⁶⁾

What are the estimated direct costs for SMEs of the preferred policy option?

Qualitative assessment

Direct costs for SMEs under Policy Option 2 are **limited and proportionate**, for several reasons:

1. .
2. **Participation in Strategic Projects and innovation procurement is voluntary** and does not impose reporting obligations on SMEs.
SMEs incur administrative costs only if they choose to participate, and these costs are standard for R&I or public-procurement participation (proposal preparation, reporting, contractual obligations).
3. **No regulatory costs are introduced that require SMEs to adapt processes, meet new standards, or undertake mandatory investments.**
4. **No changes to State aid conditions impose compliance duties on SMEs**, because Strategic Projects are designed as co-funded investment instruments, not regulatory obligations.

To sum up, **the preferred option does not introduce new operational costs for SMEs.**

Quantitative assessment

Since SMEs are exempt from mandatory data-reporting obligations:

- **Direct compliance burden = €0** (no recurring reporting or data-submission duties).
- For SMEs participating voluntarily in Strategic Projects or innovation procurement, administrative costs are limited to:
 - o Proposal preparation costs
 - o Project reporting obligations

These costs are **standard and voluntary**, not imposed by legislation, and therefore **not counted as regulatory burden** under Better Regulation guidelines.

What are the estimated direct benefits/cost savings for SMEs of the preferred policy option ⁽⁴⁰⁷⁾?

⁽⁴⁰⁶⁾ The costs and benefits data in this annex are consistent with the data in annex 3. The preferred option includes the mitigating measures listed in section 4.

Qualitative assessment

SMEs will likely benefit significantly from the preferred option, through:

1. **Increased demand and market opportunities**, especially for fabless design SMEs, manufacturing equipment SMEs, specialist materials suppliers, OSAT SMEs, and R&D service providers. Strategic Projects create stable, long-term demand for specialised SME inputs.
2. **Innovation procurement**, which provides:
 - o early revenue streams,
 - o anchor customers,
 - o reduced commercialisation risk,
 - o enhanced technology validation.
3. **Improved access to advanced design, prototyping and packaging facilities**, which reduces SMEs' reliance on non-EU infrastructure and lowers development costs.
4. **Reduced uncertainty and disruption-related costs** due to improved supply chain resilience and earlier visibility of risks (via the Business-to-Business Semiconductor Supply Chain Platform). SMEs were disproportionately harmed by recent shortages since 2020; improved monitoring reduces production interruptions and lost revenue.

Quantitative assessment

The Impact Assessment presents **no quantified SME-specific benefits**, and therefore no numerical estimates are included. Benefits remain **qualitative in nature**, based on the structural improvements described in the report.

What are the indirect impacts of this initiative on SMEs?

Indirect impacts on SMEs in downstream sectors (automotive suppliers, industrial automation, ICT hardware, telecoms, robotics, medical devices) are expected to be **positive**, due to:

- greater semiconductor availability,
- reduced exposure to global supply chain shocks,
- improved foresight,
- increased access to advanced chips including for AI and edge computing.

These sectors contain large numbers of SMEs that previously experienced significant disruption during semiconductor shortages, suggesting substantial indirect competitiveness gains.

(4) MINIMISING NEGATIVE IMPACTS ON SMES

⁽⁴⁰⁷⁾ The direct benefits for SMEs can also be cost savings.

Are SMEs disproportionately affected compared to large companies?
SMEs are not disproportionately affected under the preferred option.
Have mitigating measures been included in the preferred option/proposal?
No mitigation measures are required since SMEs are not disproportionately affected by the preferred option . Instead, the initiative includes several features that proactively promote SME participation and ensure that the regulatory framework remains proportionate for smaller firms. These features include the possibility of participation in Strategic Projects and innovation procurement. The preferred option also enhances SMEs’ access to advanced design facilities, prototyping and potentially small-lot manufacturing capacities, and strengthens supply -chain resilience, which particularly benefits SMEs given their higher vulnerability to disruptions.

CONTRIBUTION TO THE 35% BURDEN REDUCTION TARGET FOR SMEs
Are there any administrative cost savings relevant for the 35% burden reduction target for SMEs?
The preferred option introduces several simplification measures that generate administrative cost savings for SMEs and contribute to the EU’s 35% burden-reduction target. The establishment of more streamlined and predictable procedures under the revised Chips Act, including clearer pathways for participation in Strategic Projects and innovation procurement, reduces administrative complexity for SMEs.



EUROPEAN
COMMISSION

Brussels, 3.6.2026
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PART 3/3

COMMISSION STAFF WORKING DOCUMENT

IMPACT ASSESSMENT REPORT

Accompanying the document

**Proposal for a Regulation of the European Parliament and of the Council
on a framework of measures for strengthening Europe's semiconductor ecosystem
repealing Regulation (EU) 2023/1782 (Chips Act 2.0)**

{COM(2026) 504 final} - {SEC(2026) 504 final} - {SWD(2026) 505 final}

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1. INTRODUCTION

1.1. Purpose and scope of the evaluation/fitness check

Adopted in September 2023, regulation (EU) 2023/1781 establishing a framework of measures for strengthening Europe’s semiconductor ecosystem (“**Chips Act**” or “the Regulation”) represents a cornerstone initiative to reinforce the Union’s semiconductor ecosystem by reducing dependencies, enhancing digital sovereignty, stimulating investment, strengthening the capabilities, security, adaptability and resilience of the Union’s semiconductor supply chain, and increasing cooperation in the domain among the Member States, the Commission, and international strategic partners.

Since then, the rapid digital transformation of Europe’s economy – driven by the expansion of artificial intelligence (AI), cloud and edge computing, and connected devices – has intensified the demand for secure, high-performance semiconductors and exposed new vulnerabilities in global supply chains. Recent geopolitical tensions have underscored the strategic importance of ensuring Europe’s capacity to design and produce advanced semiconductors domestically, positioning semiconductors as a strategic industry for other strategic (user) industries. In this context, the Chips Act has become a central pillar of the EU’s strategy to enhance technological sovereignty, resilience, and security.

In accordance with Article 40 of the Chips Act Regulation, the European Commission (hereafter – the Commission) must submit a first report on the evaluation and review of the Regulation to the European Parliament and to the Council by 20 September 2026. Therefore, the purpose of the evaluation was to produce a **critical, unbiased, and evidence-based judgement of the progress of the Chips Act and its ability to strengthen the Union’s semiconductor ecosystem**.

In accordance with the Better Regulation Guidelines, the evaluation aims to measure to what extent the legislation is **effective, efficient, relevant, coherent, and brings clear EU added value**. It covers the **three pillars of the Chips Act** (The Chips for Europe Initiative, security of supply, and monitoring and crisis response), and cross-pillar elements.

The evaluation examines **the impact of the Chips Act** on the economy, governance and social factors, alongside the impact assessment for this initiative (where an in-depth impact assessment of each policy option is provided). It also identifies and quantifies **the costs and benefits of the Chips Act** under each Pillar. Finally, the evaluation outlines **the lessons learned** from its implementation and highlights persisting and emerging issues affecting the Regulation’s functioning.

The evaluation focuses on the period starting from the entry into force of the Chips Act on **21 September 2023 until end of November 2025** ⁽¹⁾. Depending on the results from the evaluation of the functioning of the Chips Act and an impact assessment, the Commission may propose measures aimed at possible adaptations that ensure the Chips Act remains fit for purpose in light of changing market, technological, and geopolitical realities.

⁽¹⁾ November 2025 was set as the cut-off date since this was the last time data collection was conducted for the report.

This staff working document describes the evaluation, how it was carried out, and its main findings. The report, structured in alignment with the Better Regulation Guidelines of the Commission, covers the following chapters and annexes:

- Section 1 introduces the evaluation and its methods;
- Section 2 presents the background to the intervention and its expected outcomes;
- Section 3 summarises the state of play in implementing the programme;
- Section 4 provides answers to the evaluation questions;
- Section 5 presents the evaluation results, conclusions and lessons learned;
- Annex I: evaluation matrix
- Annex II: main points of comparison
- Annex III: cost-benefit analysis

1.2. Methodology

The report draws on **sound evaluation methods** and **evidence from across the EU Member States**, gathered through stakeholder consultation, case studies, cost-benefit analysis, and desk research, as well as positions and findings from the European Parliament, the Council, and the European Semiconductor Board (ESB). On 5 September 2025, the Commission launched an **open public consultation** and a **call for evidence** on the evaluation and review of the Chips Act, with a feedback period of 12 weeks. The open public consultation was **complemented by an external study** ⁽²⁾, the contractors of which carried out targeted surveys and interviews, organised dedicated workshops, and provided input to the evaluation and drafting of the impact assessment. In addition, the Commission organised a number of targeted consultations and workshops with different types of stakeholders (e.g., Member States of the Chips JU's Public Authorities Board, industry associations, companies, RTOs, etc.) in the second half of 2025.

The consultation activities aimed at collecting the views, positions, and findings of:

- Industry stakeholders across the semiconductor value chain (IDMs, fabless companies, design houses, equipment manufacturers, suppliers);
- Industrial users of semiconductors in sectors such as automotive, telecom, healthcare, energy, industrial robotics and manufacturing, defence, and security;
- EU Member States represented in the European Semiconductor Board (ESB);
- The European Parliament ⁽³⁾;
- The Council of the European Union ⁽⁴⁾;
- National competent authorities, including semiconductor-relevant authorities;
- EU bodies such as the Chips JU Office, EISMEA, EIB, and EIF;
- Start-ups, SMEs, and scale-ups;
- Research and Technology Organisations, academia, and scientific associations;

⁽²⁾ An external study carried out by PPMI and partners supported the Commission during the evaluation and impact assessment process. The study kicked off in September 2025 and should be finalised by April 2026. The final report of the study was not yet submitted at the time of writing this report.

⁽³⁾ European Parliament resolution on European technological sovereignty and digital infrastructure (2025/2007(INI)), 11 June 2025.

⁽⁴⁾ Declaration of the Semicon Coalition calling for a revised EU Chips Act in order to strengthen and revitalize Europe's position in the global semiconductor industry, 29 September 2025.

- Trade and industry associations;
- Investors, including venture capital and private equity;
- NGOs, think tanks, and other civil society organisations;
- Independent experts and consultants.

Table 1. Overview of consultation activities

Activity type	Method	Number
Workshops	Thematic workshops	17 workshops
Public Consultations	Open Public Consultation (OPC)	103 replies
	Call for Evidence (CfE)	209 replies
Targeted surveys	National authorities survey	24 responses
	RTO & design survey	17 responses
	Supply chain survey	16 responses
	Industry users survey	7 responses
	Total surveys	64 responses
Interviews	Expert interviews	17 interviews

Overall, the evaluation of the Chips Act provides robust evaluation findings built on the analysis of quantitative and qualitative data collected through desk research, stakeholder consultation activities and case studies. However, a few limitations of the evaluation, while rather marginal and mitigated by the evaluation team as explained below, should be mentioned.

First, the evaluation mostly considers **the achievement of outputs and short-term outcomes**, since the Chips Act has only operated for a few years, and some initiatives are still in the early phase of implementation. This challenge was mitigated by combining the stakeholders' positions and opinions on achieving the intended results and impacts with the assessment of impacts of the Chips Act 2.0 in the impact assessment report.

Second, because initial stakeholder participation in the OPC and survey was somewhat low, **additional targeted consultations were incorporated into the consultation plan.** These included thematic workshops with various stakeholder groups. Following the increase in responses to the OPC and survey, the final results of consultation activities reflect a well-balanced mix of quantitative and qualitative, as well as retrospective and prospective insights.

To ensure terminological consistency and clarity throughout this report, a comprehensive **glossary** of key terms has been developed based on official EU policy documents, specifically Regulation (EU) 2023/1781 (the Chips Act) ⁽⁵⁾. This glossary serves as the definitional framework for analysing Europe's semiconductor strategy and its implications for technological sovereignty. All terms used in the analysis adhere to these official definitions unless otherwise specified. The glossary is found under the Impact Assessment.

(⁵) <https://eur-lex.europa.eu/legal-content/EN/TXT/?uri=CELEX:32023R1781>.

2. WHAT WAS THE EXPECTED OUTCOME OF THE INTERVENTION?

2.1. Description of the intervention and its objectives

This section presents the **intervention logic** underpinning the Chips Act, and the core problems it aimed to tackle. The intervention logic highlights the linkages between the needs, activities and expected impacts. It consists of a logical chain, whose success depends *inter alia* on the timing of the implemented activities, level of support provided by industry, the Member States, and the Union, and the role of external actors. The final impacts are largely beyond the direct control of the Commission.

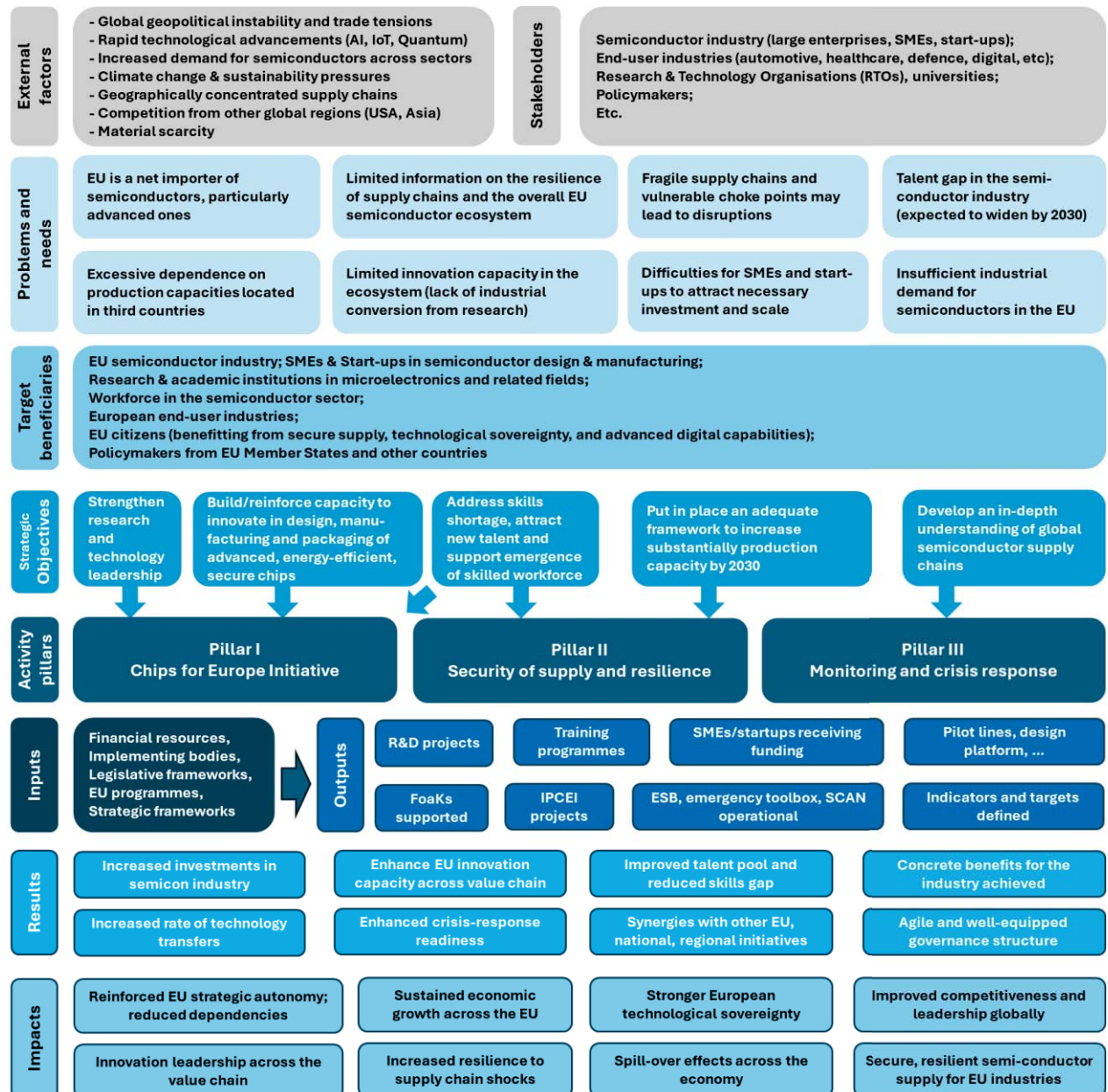


Figure 1. Intervention logic

The causal chain includes the following specific elements:

- **External factors:** overarching global conditions that influence the policy environment;
- **Needs (or problems)** addressed by the Chips Act;
- **Stakeholders:** actors with an interest in or affected by the policy;
- **Strategic objectives** of the Chips Act;
- Eligible **actions** of the Chips Act (organised in pillars);
- **Inputs:** the Chips Act's financial and administrative resources;
- **Outputs:** tangible and measurable products and services of different types directly produced by implementing the activities of the Chips Act pillars;
- **Results:** short- and medium-term results, in terms of behaviour or practice of the target group(s), organisational or policy changes;
- **Impacts:** long-term institutional and policy changes that the programme's implementation is expected to contribute to.

The elements of the intervention logic listed above link to **the evaluation criteria in focus** in the evaluation (effectiveness, efficiency, relevance, coherence and EU-added value). For instance, while effectiveness is concerned with the achievement of objectives, expected outputs, outcomes and impacts, relevance is concerned with the match between objectives, inputs and actions with the needs of the stakeholders. More information on the methods underpinning the data collection and analysis of the evaluation can be found in the Synopsis Report.

2.1.1. Context of the intervention

The Chips Act constitutes **the EU's strategic response to critical vulnerabilities** exposed in the global semiconductor supply chain as a result of the COVID-19 pandemic and intensifying subsidy-driven competition with third countries ⁽⁶⁾. The semiconductor sector faced a series of shocks due to the COVID19-related shutdowns of manufacturing facilities, workforce disruptions, and shipping delays since early 2020. A shortage of semiconductors in the EU disrupted industrial activity, with the automotive sector experiencing production cuts exceeding 30%, and Germany's car output falling by 34% in 2021 compared to 2019, reaching levels last seen in 1975 ⁽⁷⁾. The crisis extended beyond automotive manufacturing, affecting healthcare equipment, renewable energy installations, and defence systems, revealing the risks of Europe's dependency on external suppliers concentrated primarily in East Asia ⁽⁸⁾. The semiconductor market, valued at over USD 555 billion in 2021 and projected to exceed USD 1.3 trillion by 2030 ⁽⁹⁾, had become central to economic competitiveness and national security. Europe's strategic position was becoming precarious: **companies in the EU accounted for only 9% of global semiconductor production by headquarter location**, although the region

⁽⁶⁾ SWD(2022) 147, *A Chips Act for Europe*, European Commission, Staff Working Document, Brussels, 11 May 2022.

⁽⁷⁾ Verband der Automobilindustrie, https://en.vda.de/en/press/press-releases/220105_German-car-market-2021--recovery-slowed-down.html.

⁽⁸⁾ Iggo, C., and T. Riley, 'Why Semiconductors Have Become a Geopolitical Issue – and What It Means for Investors', AXA IM Corporate, 2022. <https://www.axa-im.com/investment-institute/investment-themes/technology/why-semiconductors-have-become-geopolitical-issue-and-what-it-means-investors>.

⁽⁹⁾ SEMI "Why AI will propel semiconductor market to \$1 trillion and achieve 1.0 nm by 2030", November 20, 2025 <https://www.semi.org/sites/semi.org/files/2024-11/MS-SEMIWEB11.2024.pdf>.

represented 20% of the worldwide end-user market, resulting in a EUR 19.5 billion trade deficit in 2021 ⁽¹⁰⁾.

The EU determined that **decisive, coordinated intervention was essential** to address structural dependencies in its semiconductor ecosystem and to support the industry. Member States required significant capacity to strengthen innovation systems, attract investments, and reduce external dependencies that threatened both economic resilience and technological sovereignty ⁽¹¹⁾. Meanwhile, **coordinated action at EU level was necessary to address Europe's declining competitive position in semiconductors**, as other major economies deployed unprecedented state subsidies to strengthen domestic manufacturing capabilities. Previous crises had shown that concentrated semiconductor production in a few regions created vulnerabilities across multiple sectors ⁽¹²⁾. Europe's **global value chain market share** (9.9% in 2019, 9.3% in 2020, 8.9% in 2021) ⁽¹³⁾ was insufficient to guarantee supply security. Without substantial investments in research, manufacturing capacity, and crisis response mechanisms, Europe would remain structurally vulnerable. The Chips Act emerged during a period of **strong focus on green and digital transitions**, and amid growing European consensus on the need to strengthen the region's **economic competitiveness and reverse declining industrial capacity**. The September 2024 Draghi report would later articulate these concerns comprehensively, calling for urgent industrial renewal ⁽¹⁴⁾.

2.1.2. Strategic Objectives behind the Chips Act

Given the **central role that chips play in the digital economy**, their geopolitical dimension and the current strong concentration in production capacity, the Union had to urgently reinforce its semiconductor ecosystem, increasing its resilience as well as security of supply and reducing its external dependencies. Europe would have to mobilise an unprecedented level of investment given the high positive spill-over effects the sector has across the economy and many areas of public interest. Europe would have to mobilise all its talents and assets. The overall level of policy-driven investment in support of the EU Chips Act was estimated to be in excess of **EUR 43 billion** up to 2030⁽¹⁵⁾.

While Europe was leading in research with important organisations across the continent, it would have to close the “gap from the lab to the fab” by leveraging its strengths in (i) equipment and materials, (ii) systems solutions and systems integration, (iii) strong presence in high-growth market segments like automotive, medtech, communications, energy and machinery, and (iv) research and academic excellence, where technology

⁽¹⁰⁾ European Commission, ISDB, Comext, cited in the Staff Working Document (see footnote 6) under Figure 16.

⁽¹¹⁾ SWD(2022) 147, *A Chips Act for Europe*, European Commission, Staff Working Document, Brussels, 11 May 2022.

⁽¹²⁾ Ragonnaud, G., *The EU Chips Act: Securing Europe's Supply of Semiconductors*, European Parliamentary Research Service, PE 733.596, European Parliament, June 2023.

⁽¹³⁾ Contract: CNECT/2022/MVP/0084, *Semiconductors market data by feature size, sector and region*, IDC, September 2025.

⁽¹⁴⁾ Draghi, M., *The future of European competitiveness: A competitiveness strategy for Europe*. Brussels, 2024.

⁽¹⁵⁾ COM(2022) 45, *A Chips Act for Europe*, Communication from the Commission to the European Parliament, the Council, the European Economic and Social Committee and the Committee of the Regions. Brussels, 8 February 2022.

capacities should be further reinforced. Successful outcomes crucially depend on joint efforts and close collaboration of all sides – industry along the value chain, public sector and research organisations ⁽¹⁶⁾.

To fulfil the above, the Chips Act strategy was articulated around the following five strategic objectives:

- First (Strategic Objective 1 (SO1)), Europe should **strengthen its research and technology leadership**. This was an imperative to preserve Europe’s current assets in several break-through technologies, including in equipment manufacturing and advanced materials, needed to build next-generation production facilities serving all its sectors.
- Second (SO2), **Europe must strengthen its capacity to innovate in the design, manufacturing and packaging of advanced, energy-efficient and secure chips**, and translate these innovations into manufactured products. This was key to ensuring long-term supply for industry and the public sector and to driving wider economic innovation. Achieving this would require major investment in pilot lines and in advanced design, testing and experimentation facilities. These world-class pilot lines—open to all supply-chain actors on non-discriminatory terms—would position Europe as a strong global partner and support deeper international cooperation.
- Third (SO3), **Europe must establish a framework to substantially expand its chip production capacity by 2030**. With the market expected to double, Europe must quadruple output to meet its goals. This was not only about volume: Europe must also be able to produce advanced chips, meet user needs, enter markets where it was absent, and account for environmental impacts. Strengthening security of supply, especially for public-safety-critical sectors, would be essential. Achieving this would require attracting major investments (both EU and non-EU) into production facilities and creating the right conditions for large-scale private investment.
- Fourth (SO4), Europe should **address the acute skills shortage, attract new talent and support the emergence of a skilled workforce**, as shortages were limiting efforts aimed at strengthening the ecosystem.
- Fifth (SO5), Europe should **develop an in-depth understanding of global semiconductor supply chains** to monitor its functioning, understand future trends, anticipate disruptions, build international partnerships based on more balanced capabilities and mutual interest, react in time to prevent international supply chains from breaking down, and enable the EU to take appropriate measures when necessary.

2.1.3. Activities and pillars

To achieve the Strategic Objectives, the Regulation established **a comprehensive framework built on three pillars**:

- The first pillar, **the Chips for Europe Initiative**, is about **Europe’s research policy** in the semiconductor field. It focuses on capacity building and research and innovation support to strengthen design, manufacturing and systems integration capabilities across the Union’s semiconductor value chain.

⁽¹⁶⁾ Ibidem

- The second pillar is about developing a European **industrial policy** in semiconductors aiming for **security of supply and resilience**, which would attract investments by providing criteria to recognise and support integrated production facilities (IPFs) and open EU foundries (OEFs) that are first-of-a-kind (FoaK) facilities.
- The third pillar is about **crisis management**. It establishes a coordination mechanism between the Member States and the Commission for **monitoring and crisis response**, enabling the Union to map and monitor the semiconductor sector while preparing for and responding to potential chip shortages.

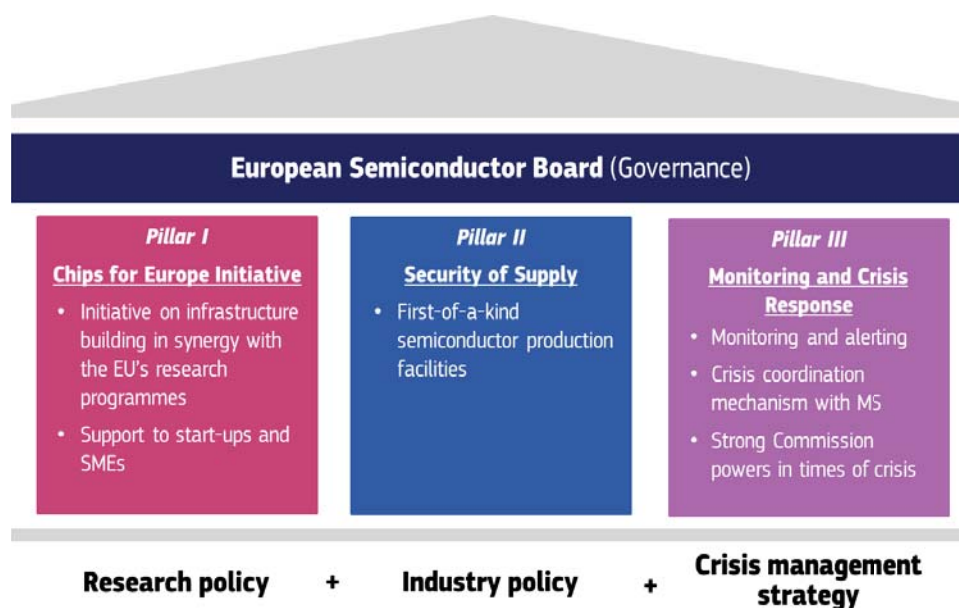


Figure 2. Pillars of the Chips Act

2.1.3.1. Pillar I - The Chips for Europe Initiative

The first pillar, the **Chips for Europe Initiative**, plays a central role in building technological capacity. While contributing to the green and digital transitions, the Initiative aims to **achieve capacity-building and support related research and innovation**. The first pillar provides the tools and instruments to address the above-mentioned Strategic Objectives 1), 2) and 4).

The capacities developed under the Chips for Europe Initiative are designed to strengthen the maturity, connectivity and resilience of the European semiconductor ecosystem and to accelerate the transfer of innovation from research to industrial deployment. State-of-the-art **pilot lines** offer shared, industrial-scale environments where new technologies can be tested, validated and prepared for production, reducing the risks associated with scaling up research results, and supporting the transition from laboratory prototypes to manufacturing-ready processes. The **design platform** focuses on reinforcing Europe's capabilities in chip design, helping to reduce dependence on non-EU tools and enabling companies (particularly SMEs and start-ups) to develop more complex and system-level products. **Competence centres** act as entry points to expertise, training and technology support, anchoring knowledge in regional ecosystems, and facilitating access to infrastructure and skills across Member States. **Quantum chip pilots** prepare Europe for emerging computing and sensing technologies by creating pathways from frontier

research to manufacturable components, while the **Chips Fund** complements these infrastructures by improving access to risk finance and scale-up capital. The rationale and intended outcomes of each component of the Initiative are set out below.

Pilot lines

The Initiative supports the enhancement of existing and development of new advanced **pilot lines** on cutting-edge and next-generation semiconductor technologies for industry to **test, experiment and validate** semiconductor technologies and system design concepts at high technology readiness levels.

The pilot line technology areas were chosen to close Europe's most critical semiconductor gaps while building on existing strengths, securing long-term competitiveness, security of supply, and industrial resilience. **Sub-2 nm logic** was prioritised to anchor Europe in the advanced nodes that power AI, HPC, data centres and next-generation communications, domains where Europe previously lacked manufacturing capacity and risked technological lock-out. **FD-SOI** capitalises on a field where Europe already leads, delivering low-power, high-reliability chips for automotive, mobility, industrial automation, and Internet of Things without depending on the most advanced nodes. **Advanced packaging and heterogeneous integration** were selected because future performance gains hinge on system-level integration; Europe faced a strategic weakness in packaging but also a major opportunity to lead in chiplets, 3D stacking, and the co-integration of logic, memory, sensing, and connectivity. **Wide-bandgap materials** (such as SiC and GaN) match Europe's strengths in power electronics and are vital for the energy transition, electric mobility, renewable infrastructure, and high-efficiency industrial systems. **Photonic integrated circuits** were included because of their growing importance for high-bandwidth, low-power data transmission, sensing and advanced computing architectures in telecoms and data centres. Together, these technologies will shape future industrial competitiveness, sustainability, and digital sovereignty, while reducing Europe's exposure to strategic dependencies.

Design platform

The Initiative sought to **strengthen Europe's design capacity** by creating a Union-wide virtual design platform connecting design houses, start-ups, SMEs, IP and tool suppliers, and research organisations. This shared environment would enable virtual prototyping and coordinated technology development.

Design is where around half of semiconductor value added and R&D spending occurs. Fabless firms dominate this phase, growing 2.7× from 2011–2021 compared with 63% for IDMs. Yet Europe captures only about 1% of global fabless revenues, with most EU design activity in IDMs and focused on lower-margin mature-node products. **Europe's weak position reflects structural barriers:** extremely high costs for advanced-node tools, IP and engineering talent, limited deep-tech finance, and a fragmented base of small design teams. Addressing these obstacles is essential to give European firms a viable path into higher-value segments of the chip industry.

The Chips Act therefore created the **Design Platform**, a cloud-based EU-wide environment offering shared access to design tools, IP libraries, PDKs and expert support. It aims to expand design capacity, lower entry barriers for start-ups and SMEs, link design to pilot lines and foundries, enable collaboration on new IP and methodologies, and strengthen skills through national competence centres. As the

strategic backbone of the Chips for Europe Initiative, the platform provides a one-stop entry point into the ecosystem, guiding users from design to prototyping and manufacturing, and uniting research, education, and industry. Its ultimate goal is to foster a new generation of European fabless start-ups, a crucial endeavour because these companies capture the highest value in the semiconductor value chain, drive innovation in fast-growing markets, and reduce Europe's dependence on foreign design ecosystems.

Quantum chips

To recognise the **strategic importance of quantum computing**, the Initiative aimed to accelerate development of quantum chips and associated technologies, including those based on semiconductor material or integrated with photonics. Dedicated actions include design libraries for quantum chips, pilot lines for building quantum chips, and facilities for testing and validating quantum chips produced by the pilot lines. The aim is to provide European researchers, start-ups and industry with reliable access to facilities capable of producing and validating the main quantum chip technologies ⁽¹⁷⁾.

Quantum technologies represent a **frontier technology** domain where semiconductor manufacturing capabilities will determine future competitive positioning. Quantum computing systems fundamentally rely on specialised quantum chips that require advanced semiconductor fabrication, cryogenic electronics, integrated photonics, and novel packaging solutions. The Chips Act's inclusion of quantum chips addresses the strategic imperative to establish European capabilities at the intersection of quantum technologies and semiconductor manufacturing. This early-stage intervention recognises that quantum computing, quantum communication, and quantum sensing applications all depend on semiconductor-based components, making quantum chip development integral to both semiconductor industrial strategy and quantum technology development.

Competence centres

Beyond infrastructure, the Initiative also addressed the Union's skills gap by enabling each Member State to establish **at least one semiconductor competence centre** in their territories. These centres constitute a central pillar of the Chips for Europe Initiative, providing structured access to technical expertise, testing facilities, and advisory services, and enabling companies (particularly SMEs and start-ups) to strengthen their design capabilities, experiment with new technologies, and develop specialised skills.

Acting as **national/regional entry points** to the European semiconductor ecosystem, competence centres facilitate knowledge and technology transfer, support the uptake of innovation, help connect stakeholders with technology infrastructures, and inform about funding opportunities. Competence centres also support access to publicly funded infrastructures, including pilot lines, testing facilities, and other competence centres.

Moreover, competence centres are tasked with supporting **skills development**, including by fostering cooperation with higher education and vocational training providers, and by enhancing the visibility and attractiveness of the semiconductor sector.

(17) <https://digital-strategy.ec.europa.eu/en/factpages/european-chips-act-chips-europe-initiative>

Chips Fund

Finally, the Commission established a dedicated semiconductor **investment facility** as part of the Initiative. Referred to collectively as the '**Chips Fund**', it provides both equity and debt financing, including through a blending facility under the InvestEU Fund established by Regulation (EU) 2021/523, in cooperation with the European Investment Bank Group and other implementing partners.

The Chips Fund is intended to complement public investment in research and infrastructure by improving **access to finance for start-ups, SMEs, and scale-ups** across the semiconductor value chain. By facilitating the mobilisation of private capital and offering financing instruments adapted to different stages of company growth, the Fund supports the commercialisation of innovation and the scaling of promising technologies. In doing so, it helps **translate advances made under the Initiative into viable business activity** and contributes to the development of a more dynamic and resilient European semiconductor ecosystem.

2.1.3.2. Pillar II - Security of supply and resilience

Pillar II was conceived as the '**industrial backbone**' of the **Chips Act**, responding to a structural weakness in Europe's semiconductor policy framework that predated the Regulation. For many years, the cost of advanced semiconductor manufacturing had increased sharply, making new fabrication projects highly capital-intensive and financially risky. In a global context where major competitors were increasingly supporting fabs through large public subsidies, firms lacked comparable instruments to de-risk investment and commit to production capacity in the Union. As a result, Europe's investment in state-of-the-art manufacturing continued to lag behind Asia and the United States, and its share of global semiconductor capital expenditure declined to around 4% and stagnated for over a decade, with only limited authorised State aid ⁽¹⁸⁾. Pillar II was therefore designed to introduce a **dedicated framework for enabling and attracting manufacturing investment**, by creating legal certainty for public support to First-of-a-kind (FOAK) facilities.

Its objective was not only to **increase manufacturing capacity** but also to restore Europe's credibility as an **investment destination** in a highly competitive global market. To this end, Pillar II established criteria to recognise and support **Integrated Production Facilities (IPF) and Open EU Foundries (OEF)** that are FOAK facilities and that fostered the security of supply and the resilience of the Union's semiconductor ecosystem. These facilities are pioneering and innovative manufacturing plants that do not yet exist in Europe. They may obtain the status of either an IPF – a vertically integrated site engaged in chip design, front-end manufacturing, equipment production, and back-end services – or an OEF, which allocates a defined share of its production capacity to manufacturing chips for external customers. The Regulation designated these facilities as being in the public interest, allowing Member States to apply support measures and provide administrative support in national permit-granting procedures.

The second pillar provides the tools and instruments to address the above-mentioned Strategic Objectives 3) and 4).

⁽¹⁸⁾ ECA special report 12/2025 – para. 44 - https://www.eca.europa.eu/ECAPublications/SR-2025-12/SR-2025-12_EN.pdf

2.1.3.3. Pillar III - Monitoring and crisis response

Pillar III was introduced to address the absence of any structured EU-level mechanism for **anticipating semiconductor shortages and coordinating responses** to major supply disruptions. Before the Chips Act, monitoring of the sector was fragmented across Member States and institutions, and crisis responses depended largely on national measures taken in isolation. Pillar III therefore created via the European Semiconductor Board a **permanent framework for joint mapping, monitoring and information exchange** between the Commission and Member States.

The architecture was designed not only to improve situational awareness but also to provide a **coordinated toolbox** in the event of crises, including targeted information requests, prioritisation of orders for critical sectors, and joint purchasing. The importance of this pillar has increased in a context of **intensified geopolitical tension, reshaped global value chains** and growing recognition of **semiconductors as a strategic asset**. By shifting from reactive crisis management to structured preparedness, Pillar III strengthens the EU's resilience, its capacity to anticipate vulnerabilities and respond collectively.

The third pillar provides the tools and instruments to address the above-mentioned Strategic Objective 5).

2.1.4. Inputs to the Chips Act

The Chips for Europe Initiative was supported by **funding from Horizon Europe and the Digital Europe Programme**, for a maximum indicative amount of EUR 1.725 billion and EUR 1.575 billion respectively, totalling EUR 3.3 billion. Except for the Chips Fund, the implementation of the Chips for Europe Initiative was entrusted to the Chips Joint Undertaking established by Council Regulation (EU) 2023/1782 of 25 July 2023, amending Regulation (EU) 2021/2085.

The implementation of the Chips Act involved **close coordination between the Union, Member States, and the private sector**. The **European Semiconductor Board**, composed of representatives of the Member States and chaired by the Commission, was established to facilitate a smooth, effective and harmonised implementation of the Regulation, cooperation, and the exchange of information. The monitoring and crisis response mechanism was implemented through administrative and coordination structures, primarily the ESB, rather than through dedicated funding programmes.

2.1.5. Expected outputs, results, and impacts

The evaluation of the EU Chips Act examines whether its instruments are appropriate and whether the implementation of activities and **outputs** has led to the expected **results** and **impacts**. Results reflect medium-term changes stemming from the Act's outputs, while impacts represent the longer-term transformations it seeks to achieve. Just over two years after entry into force, early results show initial progress toward the Act's objectives. These are the immediate consequences of the first implementation phases. While outputs and short-term results are largely within the control of implementing authorities, longer-term results and impacts are shaped by external factors such as geopolitical instability, trade tensions, rapid technological change, rising demand, material scarcity, and global competition.

Across its three pillars, the Act has generated several **outputs** and short- and medium-term **results**:

- Pillar I aimed to deliver interconnected results in investment, innovation capacity, skills, collaboration and governance. Increased investment was expected as public funds leveraged private capital. The Act sought to expand the talent pool and address skills gaps through training and education initiatives (while recognising Member State competences). Benefits for industry included improved stakeholder collaboration, better access to funding, and higher rates of technology transfer to accelerate innovation.
- Pillar II delivered outputs through FOAK facility recognition and State aid approvals, leading to a number of supported facilities and contributing to enhanced EU capacity across the value chain via advanced manufacturing capabilities.
- Pillar III established coordination mechanisms for mapping and monitoring the semiconductor ecosystem, including the ESB, emergency toolbox, and SCAN methodology. These were expected to improve global supply chain monitoring, visibility and preparedness, and create synergies with EU, national and regional initiatives, strengthening governance across the semiconductor landscape.

Impacts represent the fundamental long-term changes the Act aims to achieve. They measure progress toward strategic objectives and often materialise only after initial results interact with wider policies and market forces. Causal links are less direct due to external influences. The Act's primary expected **long-term impact** is a strengthened, more resilient Union-level semiconductor ecosystem, with increased domestic production reducing dependence on third countries and enhancing Europe's economic security. A second expected impact is contributing to the EU's target of reaching 20% global semiconductor market share by 2030 under the Digital Decade Policy Programme, solidifying Europe as a major player. Ultimately, the Act aims to foster innovation leadership and sustained growth by building a competitive ecosystem that supports the Digital Decade, the Green Deal, and a more prosperous, technologically secure Europe.

2.2. Points of comparison

The evaluation attempts to **capture progress** in the implementation of the Chips Act and the **changes observed** as a result of its implementation.

Annex II of the Chips Act sets out measurable indicators to monitor the implementation and report on the progress towards the achievement of operational objectives. The performance of the intervention can be measured against the process on these indicators over time, as well as core outputs, combined with a selection of indicators on expected results and impacts – as highlighted in the intervention logic and evaluation matrix (see Annex I – Evaluation matrix).

The main points of comparison are:

- The situation before the intervention (2021);
- The situation during the evaluation of the Chips Act (using monitoring data, evaluation and impact assessment findings, 2025).

Please refer to Annex II – Main points of comparison.

3. HOW HAS THE SITUATION EVOLVED OVER THE EVALUATION PERIOD?

3.1. The implementation of the Chips Act

3.1.1. Pillar I

Pillar I ⁽¹⁹⁾ (see Section 2.1.3.1) focuses on supporting technological capacity building and innovation in the Union, boosting research and development (R&D), strengthening Europe's research and technology leadership, and accelerating the transition from research to industrial-scale production ('*bridging the gap from lab to fab*').

With the exception of the Chips Fund (which is being implemented by the European Innovation Council and InvestEU), the Initiative is implemented through the **Chips Joint Undertaking (Chips JU)** ⁽²⁰⁾, previously known as the Key Digital Technologies Joint Undertaking ⁽²¹⁾. The Union contributes up to EUR 4.175 billion from the Digital Europe Programme (DEP) and the Horizon Europe (HE) programme to the budget of the Chips JU between 2021 and 2027, including EUR 2.875 billion for the Chips for Europe Initiative. Union funding is commensurately matched by Member States and associated countries (participating states). Industry contributes an amount of at least EUR 2.5 billion. On the other hand, the Chips Fund is funded with an amount of EUR 425 million from the Union's budget which is expected to trigger a total amount of around EUR 2.1 billion EU investment and leveraged equity support.

Two years after its entry into force, **more than 85% of the Initiative's budget has already been committed** in order to connect top-tier research with industrial applications ⁽²²⁾. Because of the complexity of the Initiative's various components, certain activities have progressed faster than others. For example, while competence centres are operational and five pilot lines are starting operations, the design platform is expected to become fully operational in the second half of 2026.

Below, the status of implementation of each operational objective is presented in detail.

Pilot lines

As explained in Section 2.1.3.1, the **pilot lines** are intended to serve as platforms for European research and development with an industrial perspective to bridge the gap between the Union's advanced research and innovation capabilities and their industrial exploitation ⁽²³⁾.

In the beginning of December 2023, barely two months after the Chips Act's entry into force, the **first four calls for pilot lines** were launched by the Chips JU. While the pilot lines are currently operational to varying extents, more equipment, machinery, and tools are being added to increase the capability and capacity of the pilot lines. Some parts incur delays, typically linked to delays in the procurement of tools and equipment. In any case, the Commission expects full capacity to be achieved by the end of 2026. In July 2024,

⁽¹⁹⁾ <https://digital-strategy.ec.europa.eu/en/factpages/european-chips-act-chips-europe-initiative>

⁽²⁰⁾ <https://www.chips-ju.europa.eu/>

⁽²¹⁾ <https://digital-strategy.ec.europa.eu/en/factpages/european-chips-act-chips-europe-initiative>

⁽²²⁾ <https://digital-strategy.ec.europa.eu/en/news/european-chips-act-update-latest-milestones>

⁽²³⁾ <https://digital-strategy.ec.europa.eu/en/factpages/european-chips-act-chips-europe-initiative>

the Chips JU launched a **call for a fifth pilot line** on photonics which would see its first operation by the end of 2025 and achieve full capacity also by the end of 2026.

In line with the technology areas laid down in the Chips Act ⁽²⁴⁾, the Chips JU launched calls for pilot lines supported with a total of EUR 3.7 billion public funding ⁽²⁵⁾ that focus on five key areas (see Section 2.1.3.1):

Pilot line	Name	Coordinator	EU funding (in EUR million)	National funding (in EUR million)
Leading edge nodes	NanoIC	IMEC (BE)	700.0	700.0
FDSOI	FAMES	CEA-Leti (FR)	414.7	414.7
Heterogeneous integration	APECS	Fraunhofer (DE)	366.4	366.4
Wide-bandgap materials	WBG	CNR (IT)	160.2	191.0
Photonics	PIXEurope	ICFO (ES)	189.9	189.9
Total			1,831.2	1,862.1

In addition to these pilot lines, a dedicated **Accelerator for Advanced Strained SOI Substrates (sSOI Accelerator)** was introduced in the Chips JU’s 2025 work programme with an EU contribution of EUR 30 million. The topic aims to establish a European supply of strained silicon-on-insulator wafers, enabling 7 nm fully-depleted SOI technology by 2030 ⁽²⁶⁾. Selection decisions will be made in Q1 2026.

Moreover, on 15 November 2025, the Chips JU launched a EUR 50 million call on “**Lab to Fab Accelerators**” for advanced packaging and heterogeneous integration and a corresponding EUR 2 million *Coordination and Support Action* to boost cooperation for industrial implementation of advanced packaging of chiplets and heterogeneous integration in Europe. The aim of these two calls is to achieve a **rapid uptake by European industry of the technologies developed under the pilot lines**, in particular technologies related to advanced packaging.

Design platform

Setting up the Design Platform (see Section 2.1.3.1) is particularly complex because it involves a wide range of actors (Platform Coordination Team (PCT), Design Enablement Teams (DETs), cloud providers, Electronic Design Automation (EDA) vendors and IP providers) and follows sequential implementation steps. These run from appointing the PCT and defining specifications to launching subsequent calls and the tender for the central cloud platform, making it slower to establish than other Initiative components. Funded under DEP and HE, the platform is structured through seven interlinked calls.

A PCT is now in place to operate the platform, host the central cloud infrastructure and coordinate user support services. DETs have also been selected to provide tailored, end-to-end support for users throughout the chip development process. A tender is currently open for the central cloud infrastructure, which will host IP, pilot-line Process Design

⁽²⁴⁾ Chips Act, Article 5 and Annex I

⁽²⁵⁾ <https://digital-strategy.ec.europa.eu/en/news/chips-europe-initiative-milestone-event-first-pilot-lines>

⁽²⁶⁾ https://www.chips-ju.europa.eu/Appendix6_I.pdf

Kits and open-source EDA tools. Another call is open to administer grants for start-ups and SMEs using the platform.

As part of the broader objective to support design, the Design Platform is complemented by other initiatives aiming to cultivate design related competences in Europe. There is support for open-source EDA tools development and for the EuroPractice services that provide over 600 European universities with access to EDA tools for training at nominal costs as well as access to fabrication from leading foundries.

Quantum chips

The Chips for Europe Initiative also focuses on the specific needs of chips exploiting quantum effects, i.e., quantum chips (see Section 2.1.3.1). This is a sector in which the EU remains competitive ⁽²⁷⁾. This is confirmed by a recent JRC report that concludes that overall, the EU is well-positioned to play a key role in the development of quantum technologies, with its strong research and innovation ecosystem, and significant investments in the sector ⁽²⁸⁾. The aim is to provide European researchers, start-ups, and industry with reliable access to facilities capable of producing and validating the main quantum chip technologies.

In September 2024, the Chips JU launched two calls that led to the establishment of Framework Partnership Agreements launching six pilot lines, **one for each of the leading European technology platforms: superconducting, spin, photonic, diamond, neutral-atom, and trapped-ion chips**. In July 2025, the selected consortia were invited to submit Specific Grant Agreement proposals, each with an indicative EU contribution of EUR 25 million, to be matched by participating states ⁽²⁹⁾. These SGAs cover the first three to four years of implementation under each FPA. Their work focuses on setting up stable pilot-scale fabrication processes, integrating testing and experimentation facilities, developing early industrialisation roadmaps, and laying the groundwork for future scaling. These steps mark the initial phase of a broader EUR 200 million EU investment matched by participating states in quantum chip development foreseen under the Chips Act until 2027 ⁽³⁰⁾.

⁽²⁷⁾ ZVEI, [https://www.zvei.org/en/press-media/publications/towards-a-european-chips-act-20; DigitalEurope, Chips Act 2.0: From emergency response to strategic industry development - DIGITALEUROPE](https://www.zvei.org/en/press-media/publications/towards-a-european-chips-act-20;DigitalEurope, Chips Act 2.0: From emergency response to strategic industry development - DIGITALEUROPE)

⁽²⁸⁾ <https://publications.jrc.ec.europa.eu/repository/handle/JRC141050>

⁽²⁹⁾ https://www.chips-ju.europa.eu/Appendix6_I.pdf

⁽³⁰⁾ <https://digital-strategy.ec.europa.eu/en/news/european-chips-act-update-latest-milestones>

Pilot line	Name	Coordinator	EU funding (in EUR million)	National funding (in EUR million)
Superconducting	SUPREME	VTT (FI)	25.0	24.2
Spin	SPINS	IMEC (BE)	24.8	23.2
Photonic	P4Q	University of Twente (NL)	24.9	26.6
Diamond	DIREQT	CNR (IT)	25.0	24.5
Neutral-atom	Q-PLANET	PASCAL (FR)	25.0	21.8
Trapped-ion	CHAMP-ION	SAL (AT)	25.0	20.7
Total			149.7	141.1

Competence centres

Competence centres in semiconductors (see Section 2.1.3.1) play an **essential role in the Initiative**. The centres provide access to technical expertise and experimentation in the area of semiconductors, helping companies – SMEs in particular – to approach and improve design capabilities and developing skills.

As of end of 2025, following two Chips JU calls, competence centres have been established in all Member States, as well as in Norway. For these calls, the Union made available for each competence centre up to EUR 1 million per year, per country, for a 4-year period, while participating states made a matching contribution. In addition, a *Coordination and Support Action (CSA)* was launched to set up and coordinate the work of the national competence centres.

Skills

Competence centres have the mandate to support skills development, including networking higher education and vocational training opportunities, and promoting the sector's visibility and attractiveness. The CSA in charge to set up the network of competence centres has launched a **Training and Skills Development** focus group which drives collaboration among the centres to roll out education and upskilling initiatives, to create training concepts, and to provide specific training and access to the design platform and pilot lines.

The Union of Skills calls for a reinforced **Pact for Skills** where Large-Scale Partnerships will support the development of sector-specific solutions; it will tackle the fragmentation of initiatives and improve linkages between them, such as the EU Skills Academies, European Alliance for Apprenticeships, the Centres of Vocational Excellence and European Universities alliances. Improvements will be made to cross-sectoral synergies among Pact members, knowledge and resource sharing along the value chain (e.g. skills intelligence, occupational profiles, curricula, training modules). The existing **microelectronics partnership** is already providing upskilling and reskilling opportunities in the sector. Through its activities, it promotes upskilling and reskilling of 50% of the workforce each year by 2030 across the industry.

Under the **Union of Skills**, the STEM Education Strategic Plan aims to strengthen the talent pipeline in STEM sectors from early education through lifelong learning. The Plan's actions target schools (including through the establishment of STEM Education Centres), higher education institutions (including through the establishment of European

Degrees in Engineering), companies (including through the creation of STEM Skills Foundries) and girls and women (including through the initiative ‘Girls Go STEM’). A Commission expert group ‘STEAM Executive Panel’ will provide advice and recommendations to the Commission on how to strengthen academia-business collaboration.

Another skills related action is the **European Chips Skills Academy (ECSA)**, a four-year European Blueprint project funded under Erasmus+ and kicked off in October 2023. It brings together a wide range of key players in the microelectronics ecosystem and opens new opportunities for collaboration between industrial leaders and educational institutions at all levels (secondary school, VET providers, and higher education). It has been focusing on mapping the skills needs and demand by industry, developing innovative strategic approaches and collaboration between education and businesses, and bridging its gap with VET and higher education ⁽³¹⁾.

Moreover, the Chips JU 2026 work programme contains three topics on talent development, worth EUR 45 million, which will support and complement initiatives by the competence centres on higher education, vocational training, and hands-on activities for students and workers. **These 2026 topics and the Competence centres’ activities support the wider Commission’s strategy on skills** and build on some recent initiatives launched by the Commission, such as the calls of the 2022, 2023 and 2024 DEP Work Programmes (EUR ~28 million), ongoing projects under Erasmus+ such as the above-mentioned European Chips Skills Academy (EUR ~4 million) and the European Chips Diversity Alliance (EUR ~1.5 million) ⁽³²⁾, the Industrial Alliance on Processors and Semiconductor Technologies ⁽³³⁾ and notably its working group on skills ⁽³⁴⁾, and the Chips Academy call foreseen by the current DEP Work Programme in 2027 (EUR ~10 million).

Chips Fund

The Chips Fund aims to improve access to capital for start-ups, scale-ups, SMEs, and other companies in the semiconductor value chain. It is currently implemented through two thematic investment facilities:

- European Innovation Council’s Accelerator programme, with Horizon Europe funding in blended grant and equity for high-risk, deep-tech startups.
- InvestEU Fund, managed by the European Investment Fund (EIF), with a guarantee from DEP, for intermediated equity investments ranging from seed to growth stage.

Under the Chips Fund, the **European Innovation Council (EIC)** has launched a dedicated **Accelerator Challenge on Semiconductor and Quantum Technologies** in its 2023 and 2024 work programmes, through which 24 highly innovative startups were selected and awarded a total of EUR 62 million in grants and EUR 238 million in

⁽³¹⁾ <https://chipsacademy.eu/>

⁽³²⁾ <https://diversityinchips.eu/>

⁽³³⁾ https://single-market-economy.ec.europa.eu/industry/industrial-alliances/industrial-alliance-processors-and-semiconductor-technologies_en

⁽³⁴⁾ <https://allpros.eu/thematic-working-groups/working-group-skills>

recommended equity investment from the EIB, and mobilising further private capital. **The EUR 300 million available budget was fully deployed in just two years.**

Beyond this thematic window, semiconductor, photonics and quantum chip companies continue to be eligible under the **open EIC Accelerator call**, where they compete with applicants from all fields; it is estimated that between 2020 and 2025 an additional EUR 500 million in grants and equity were allocated to beneficiaries from these domains through the open calls.

Complementing this, from 2025 the **Strategic Technologies for Europe Platform (STEP) programme** has been implemented with a call targeting deep-tech scale-ups in digital, deep tech, clean tech, and biotech, with a budget of EUR 300 million per year. Semiconductor and quantum scale-ups are explicitly included, and eight such companies have already been selected for a total recommended equity investment of EUR 180 million, that would address the chronic lack of scale-up capital for deep-tech semiconductor firms in Europe.

On the **InvestEU** leg of the Chips Fund, the Commission provides a EUR 125 million guarantee, matched by EIF resources and implemented by the EIF as an intermediated fund through a thematic investment facility on “Semiconductor chips and technologies”. The final selection of portfolio companies is carried out by financial partners (venture capital funds) selected by the EIF. To date, four financial partners have been selected and EUR 68 million in funds have been signed or approved with them, with two additional partners currently in the due diligence pipeline, resulting so far in 31 companies from early to growth stage having received EUR 116 million equity investment.

European Chips Infrastructure Consortium – ECIC

For the purpose of implementing actions funded under the Chips for Europe Initiative, Article 7 of the Chips Act introduces the possibility for consortia to establish a legal entity in the form of a **European Chips Infrastructure Consortium (ECIC)**. The main benefit of an ECIC is the fact that it has legal personality (and hence, legal capacity in all Member States). This means, for instance, that compared to some other instruments, its duration extends beyond the lifetime of a given Multiannual Financial Framework, granting an ECIC certain stability. Moreover, an ECIC whose membership would not include private entities would be recognised as an international body, which could have certain VAT advantages. While ECICs could implement any action under the Initiative, they were mainly meant to implement pilot lines or the design platform.

Since the Chips Act’s entry into force, **the Commission did not receive any application to set up an ECIC**. The initiative to set up an ECIC belongs to the coordinator of a potential consortium. For instance, the consortia that are implementing the five pilot lines and the design platform opted for a traditional project consortium structure.

3.1.2. Pillar II

Pillar II is aimed at attracting significant public and private investments in innovative FOAK production facilities ⁽³⁵⁾ that may be granted the **status of IPF or OEF** (see Section 2.1.3.2). Benefits of such status include administrative support in national

⁽³⁵⁾ Chips Act, articles 13-18.

permit-granting procedures, and prioritised access to pilot lines. At the same time, where a semiconductor crisis stage is activated by the Council (Article 23 Chips Act), the Commission is enabled to require IPF and OEF facilities to accept and prioritise an order of crisis relevant products ('priority-rated order'). **Nevertheless, both the activation of the crisis stage and the application of priority-rated orders have not been used so far.** They are 'last resort' measures subject to very specific criteria and conditions that ensure that they are necessary and proportional.

FOAK facilities

Although applying for the status of IPF or OEF is not mandatory and requires a separate procedure from the State aid assessment, these two procedures and the respective assessments are typically conducted in parallel, where possible ⁽³⁶⁾⁽³⁷⁾. The application process and eligibility criteria for applications are outlined in the guidance prepared by the Commission ⁽³⁸⁾.

While **several projects are still under development**, the Commission has already approved **eleven State aid decisions on FOAK semiconductor facilities** that represent a total public and private investment of over EUR 32 billion ⁽³⁹⁾. Out of these cases, the Commission has formally granted the status of IPF and OEF to four semiconductor projects ⁽⁴⁰⁾ in October 2025, while more are in the pipeline. The projects that received the status include OS4EU (ams OSRAM, Austria), ESMC (European Semiconductor Manufacturing Company, Germany), MEGAFAB-DD (Infineon Technologies Dresden, Germany), and Catania Campus (STMicroelectronics, Italy) ⁽⁴¹⁾.

Company	Location	Investment (in EUR billion)	Technology
STMicroelectronics	Catania (IT)	0.73	SiC wafer
STMicro & GlobalFoundries	Crolles (FR)	7.5	300-mm FD-SOI
STMicroelectronics	Catania (IT)	5	SiC devices
ESMC	Dresden (DE)	>10	CMOS, FinFET
Silicon Box	Novara (IT)	3.2	Advanced packaging
Infineon	Dresden (DE)	3.54	Discrete, analog/mixed signals
ams OSRAM	Premstätten (AT)	0.567	CMOS
Ephos	Milan (IT)	n.d.	glass-based photonic chips
onsemi	Rožnov (CZ)	1.64	SiC devices
GlobalFoundries	Dresden (DE)	n.d.	300-mm FD-SOI and BCD
X-Fab	Erfurt (DE)	n.d.	Advanced packaging

⁽³⁶⁾ <https://digital-strategy.ec.europa.eu/en/factpages/european-chips-act-security-supply-and-resilience>

⁽³⁷⁾ FOAK compliance and some obligations associated with IPF/OEF status are taken into account in the State aid assessment (cfr. Chips Act Communication, <https://eur-lex.europa.eu/legal-content/EN/TXT/?uri=celex:52022DC0045>)

⁽³⁸⁾ https://eur-lex.europa.eu/legal-content/EN/TXT/?uri=OJ:C_202404911

⁽³⁹⁾ <https://digital-strategy.ec.europa.eu/en/policies/european-chips-act>

⁽⁴⁰⁾ <https://digital-strategy.ec.europa.eu/en/news/milestone-strengthening-europes-semiconductor-manufacturing-capacity-under-chips-act-reached>

⁽⁴¹⁾ <https://digital-strategy.ec.europa.eu/en/library/commission-decisions-strengthening-europes-semiconductor-manufacturing-capacity-under-chips-act>

Total	>32

n.d. = not disclosed (yet)

These investments under Pillar II are complemented by an **Important Project of Common European Interest ('IPCEI')** on microelectronics and communication technologies, which supports research and development up to first industrial deployment across the value chain with over **EUR 20 billion** total public and private investment ⁽⁴²⁾. Moreover, a number of additional projects have been announced, are in preparation or in the decision process, with estimated value around EUR 25 billion. Taking all together, including support for the IPCEI on Microelectronics and Communication Technologies, so far, **the Chips Act has already catalysed more than EUR 80 billion in announced or planned investments in chip manufacturing capacity as well as related research and innovation investments**, thereby contributing to increasing the EU's market share globally.

Label of design centres of excellence

According to Article 17 of the Chips Act, the Commission may award a label of “design centre of excellence” to design centres established in the Union that significantly enhance the Union's capabilities in innovative chip design through their service offerings or through the development, promotion, and strengthening of design skills and capabilities. The procedure for applications and the requirements and conditions for the granting, monitoring, and withdrawal of the label should be set out by the Commission by means of delegated acts ⁽⁴³⁾. However, for the reasons explained under Section 4, at the point of this evaluation, the Commission did not adopt delegated acts on design centres of excellence.

3.1.3. Pillar III

Pillar III is dedicated to **enhancing cooperation between EU Member States and the European Commission** to anticipate future chips crises, and to address them through close coordination. To this end, the ESB is tasked with monitoring and crisis response activities, and with advising the Commission across all three pillars. The coordination mechanism consists of three components:

- **Monitoring:** strategic mapping; early-warning indicators; identification of key market actors; risk mitigation;
- **Crisis response:** alerts and preventive actions; activation of the crisis stage; emergency toolbox (including information gathering, priority-rated orders, and common purchasing);
- **Governance:** European Semiconductor Board.

The preparatory work started in 2022 with the Commission's Recommendation on a common Union toolbox to address semiconductor shortages and an EU mechanism for monitoring the semiconductor ecosystem ⁽⁴⁴⁾. A **European Semiconductor Expert Group** was established through which Member States implemented the

⁽⁴²⁾ https://ec.europa.eu/commission/presscorner/detail/en/ip_23_3087

⁽⁴³⁾ <https://digital-strategy.ec.europa.eu/en/factpages/european-chips-act-security-supply-and-resilience>

⁽⁴⁴⁾ Commission Recommendation (EU) 2022/210 of 8 February 2022 on a common Union toolbox to address semiconductor shortages and an EU mechanism for monitoring the semiconductor ecosystem

Recommendation. The formal work on the monitoring mechanism began once the Chips Act regulation had entered into force in September 2023, and the ESB was formally set up. The Commission signed a service contract in September 2025⁽⁴⁵⁾ to provide analytical, methodological, and administrative support to the Commission and the ESB in the implementation of Pillar III.

Monitoring

The Commission, in consultation with the ESB, **monitors the semiconductor value chain to identify possible disruptions**. This monitoring foresees a strategic mapping of the sector, including key products and critical infrastructures, main user industries, and key segments of the supply chains and dependencies; monitoring of early warning indicators; Member States' reporting on market trends; and best practices for preventive risk mitigation and increased transparency.

Regarding the status of implementation, the **key mapping and data collection** took place and the **analysis of supply chains** has been developed. Several key reports have been published to address these issues, including the JRC report "Semiconductors in the EU"⁽⁴⁶⁾, report "The EC consultation on the semiconductors' value chain"⁽⁴⁷⁾, report "Economic analysis of the EU and international semiconductor ecosystem"⁽⁴⁸⁾, and JRC report "EU's strengths and weaknesses in the global semiconductor sector"⁽⁴⁹⁾. Furthermore, the **SCAN monitoring system** was established, alongside the detailed monitoring methodology⁽⁵⁰⁾. The complete methodological toolbox proposed to monitor the semiconductor supply chain, including the SCAN methodology, was outlined in the following JRC reports: "Applying the SCAN methodology to the Semiconductor Supply Chain"⁽⁵¹⁾ and "A methodological toolbox to monitor the semiconductors' supply-chain"⁽⁵²⁾.

Moreover, in 2023, a **semiconductor alert system** was set up to allow stakeholders to report semiconductor supply chain disruptions. It helps the Commission to gather information needed to establish a precise assessment of risks and to quickly react to any potential crisis situation via the ESB⁽⁵³⁾.

Economic Security

⁽⁴⁵⁾ <https://ted.europa.eu/en/notice/-/detail/627092-2025>

⁽⁴⁶⁾ <https://publications.jrc.ec.europa.eu/repository/handle/JRC133850>

⁽⁴⁷⁾ <https://publications.jrc.ec.europa.eu/repository/handle/JRC133892>

⁽⁴⁸⁾ <https://icos-semiconductors.eu/uncategorized/economic-analysis-of-the-eu-and-international-semiconductor-ecosystem/>

⁽⁴⁹⁾ <https://publications.jrc.ec.europa.eu/repository/handle/JRC141323>

⁽⁵⁰⁾ The SCAN monitoring system is an internal system used by the Commission, which mainly tracks the product dependencies at EU and Member State level leveraging customs data. The methodological toolbox will be implemented via the service contract signed in September 2025 (by among others gathering supply chain data to frequently generate and monitor the proposed indicators).

⁽⁵¹⁾ <https://publications.jrc.ec.europa.eu/repository/handle/JRC133736>

⁽⁵²⁾ <https://publications.jrc.ec.europa.eu/repository/handle/JRC138921>

⁽⁵³⁾ <https://digital-strategy.ec.europa.eu/en/news/european-chips-act-commission-launches-pilot-system-monitor-semiconductor-supply-chain>

The **EU Economic Security Strategy** ⁽⁵⁴⁾ is a separate policy from the Chips Act, and therefore not in the scope of the evaluation. However, strong links organically emerged between the Strategy and the Chips Act, in particular with Pillar III. The Strategy mandated **joint Risk Assessments** with Member States on Advanced Semiconductor technologies ⁽⁵⁵⁾. A subgroup of the ESB was created to collect data, and to validate the draft reports before adoption by the plenary. A first report covered the **risks for the security of supply of advanced semiconductors linked to tensions in the Indo-Pacific**, and showed that a severe shortage or denial to access of semiconductors would have a significant impact for EU companies in essential sectors for the European economy, including the automotive, space and defence, and telecommunication sectors. A second report covered the risks of **semiconductor-manufacturing equipment technology leakage to third countries**. The main risks identified are a loss of market share and competitive edge, and erosion of the EU's technology leadership and indispensability.

Crisis response

Article 24 of the Chips Act establishes a **crisis response mechanism** (i.e., “emergency toolbox”) that the Commission may use when serious semiconductor supply-chain disruptions endanger the supply, repair or maintenance of essential products for critical sectors. The Commission may consult the ESB on preventive actions such as joint procurement and policy coordination within the EU and with third countries. If it considers a **crisis stage** necessary and proportionate, it may propose its activation to the Council. Once activated, the Commission increases coordination with the ESB and may apply one or more emergency tools. Annex IV of the Chips Act lists the critical sectors concerned, including energy, transport, banking and financial infrastructure, health, water and wastewater, digital infrastructure, public administration, space, food production and distribution, defence and security ⁽⁵⁶⁾.

At the point of this evaluation, a crisis has not been activated since the entry into force of the Chips Act. There have been examples of supply chain disruptions that however did not qualify as a crisis according to Article 23 of the Chips Act, for instance because they involved sectors not included in Annex IV. Moreover, in order to assess whether or not critical sectors are threatened, a swift review of available evidence is necessary, as the Nexperia case (see Section 4.1.1.3) made evident. In this case, the Commission created the **Task Force on Situational Analysis**, a subgroup of the ESB composed of a small number of experts volunteered by 8 Member States ⁽⁵⁷⁾. It assists the Commission in the collection and analysis of evidence regarding rapidly developing situations or imminent risks to economic security in the field of semiconductors, when coordinating 27 Members would be too slow. The Taskforce reports its finding to the ESB.

⁽⁵⁴⁾ <https://eur-lex.europa.eu/legal-content/EN/TXT/?uri=celex:52023JC0020>

⁽⁵⁵⁾ <https://digital-strategy.ec.europa.eu/en/news/commission-recommends-carrying-out-risk-assessments-four-critical-technology-areas-advanced>

⁽⁵⁶⁾ <https://digital-strategy.ec.europa.eu/en/factpages/european-chips-act-monitoring-and-crisis-response>. See also Annex IV of the Chips Act.

⁽⁵⁷⁾ <https://ec.europa.eu/transparency/expert-groups-register/screen/expert-groups/consult?lang=en&fromMainGroup=true&groupID=105752>

In case a crisis is activated, **Pillar III's toolbox includes three measures**: information gathering (Article 25), priority-rated orders (Article 26) and common purchasing (Article 27).

Under the first measure (**information gathering**), the Commission may request undertakings operating along the semiconductor supply chain to provide information about their production capabilities and capacities, as well as current primary disruptions. **This measure is ready for deployment.**

Under the second measure (**priority-rated orders – PROs**), a semiconductor company may be requested to accept and preferentially perform an order of crisis-relevant products for an individual beneficiary of a critical sector. **This measure is not yet ready for deployment**, because, on the one hand, facilities that may be subject to PROs will only be operational as of 2028. On the other hand, at the moment of finalising this evaluation report the Commission has not yet adopted the implementing act laying down the practical and operational arrangements for the functioning of PROs.

The third measure (**common purchasing**) allows the Commission, upon the request of two or more Member States, to act as a central purchasing body on behalf of all Member States willing to participate for their public procurement of crisis-relevant products. While this measure is **legally ready for deployment**, preparatory work is still ongoing internally in order for the Commission to be ready to take up the **role of central purchasing body**. This is due to the fact that common purchasing qualifies as public procurement from the Union and would therefore require preparation and coordination between different services in charge of technical, legal and budgetary aspects. A standard operating procedure is in preparation to define an appropriate workflow.

Governance – European Semiconductor Board

The governance mechanism of the Chips Act is ensured by the **ESB** ⁽⁵⁸⁾, which includes representatives of the Member States and is chaired by the Commission. **The ESB has been actively steering progress since November 2023**, coordinating national efforts and monitoring supply chain resilience. The ESB provides the Commission with advice, assistance, and recommendations across the three Pillars of action. It advises on the Chips for Europe Initiative to the PAB of the Chips JU (Pillar I); it is consulted for the decisions of the Commission to grant the status of IPF and OEF (Pillar II); and it is responsible for the monitoring and crisis response activities (Pillar III) ⁽⁵⁹⁾.

The ESB is fully operational. Since its inception it has held ten plenary meetings (two online and two physical meetings per year) advising the Commission on all Pillars; four meetings of its three subgroups ⁽⁶⁰⁾; and contributed to a written consultation and two risk assessments in the context of the Economic Security Strategy. The ESB also took part in a **simulation exercise on the preparedness for semiconductor supply chain**

⁽⁵⁸⁾ <https://ec.europa.eu/transparency/expert-groups-register/screen/expert-groups/consult?lang=en&groupID=3932>

⁽⁵⁹⁾ <https://digital-strategy.ec.europa.eu/en/factpages/european-chips-act-monitoring-and-crisis-response>

⁽⁶⁰⁾ Working Group on Semiconductor Economic Security; Working Group on Chips Act review; and Task Force on Situational Analysis.

disruptions, together with the Council Working Party on Competitiveness and Growth (Industry) ⁽⁶¹⁾, supported by the ChipDiplo consortium ⁽⁶²⁾.

The European Commission organised a **tabletop exercise on semiconductor supply chain disruptions** in Brussels on 24 November 2025, in order to improve Europe's preparedness to respond to a crisis under the EU Chips Act.

The ChipDiplo consortium, co-funded by the EU, facilitated the activity by developing a fictional but plausible scenario affecting global semiconductor manufacturing hubs, leading to disruptions in the supply chain. The exercise involved participants from all 27 Member States, sitting both in the European Semiconductor Board and in the Council Working Party on Competitiveness and Growth (Industry).

Players analysed the effects of a chips shortage on the European industry and in particular on critical sectors of the society and the economy such as energy, transport, health, digital infrastructure, space, security and defence – as defined in the Chips Act. Each Member State was briefed with country-specific information compiled by the Joint Research Centre and produced in the context of the supply chain mapping activities of the Chips Act. Together, participants explored options to mitigate the impact of the crisis, including mechanisms from the Chips Act's crisis toolbox.

The exercise clearly showed the importance for the EU to increase its preparedness and to invest to reduce its dependencies on third countries. It also showed that decision-makers need a mandate to collect precise and reliable data to properly assess supply chain disruptions, even in order to prevent a crisis from materialising.

3.2. Unexpected or unintended changes

Since the Chips Act was proposed in February 2022, an accelerated shift from multi-polarisation to disentanglement in global markets has taken place. The resulting **weaponisation of economic interdependencies** reveals vulnerabilities within European semiconductor supply chains, posing serious risks to European economic security and sovereignty.

Two weeks after the Chips Act was proposed, the **Russian full-scale invasion of Ukraine** on 24 February 2022 caused a tectonic shift in European politics. The war drove up energy prices in Europe which impacted the competitiveness of energy-intensive industries in Europe and harmed European competitiveness. At the same time, Ukraine's response fuelled innovation in the defence sector which showcased a need for trustworthy European semiconductors.

Shortly thereafter, **OpenAI launched ChatGPT**, a generative artificial intelligence chatbot with 800 million weekly active users. The launch became an inflection point for investments in the entire artificial intelligence stack. Software and hardware companies received unprecedented private investments and state subsidies in order for them to finance data centres and compete for talent. These investments spilled over into the semiconductor market sending companies' market capitalisations to unprecedented heights with Nvidia reaching \$5 trillion in October 2025. Additionally, state

⁽⁶¹⁾ <https://digital-strategy.ec.europa.eu/en/news/commission-and-member-states-rehearse-coordinated-response-semiconductor-supply-chain-shortages>

⁽⁶²⁾ <https://digital-strategy.ec.europa.eu/en/news/chipdiplo-consortium-selected-support-international-diplomacy-semiconductors>

interventions risk leading to distortions of the market level-playing field and result in overcapacities. This further increases the pressure on European competitiveness and threatens the established multipolar trade regime.

Simultaneously, a **race between the United States and China** to reach leadership in emerging technologies ensued. This intensified existing trade tensions and resulted in a tit-for-tat of tariffs, export controls and licence requirements. Especially, tensions around rare earth elements, for which China holds a monopoly, and semiconductor intellectual property introduced uncertainty to the European market and highlighted a need for increased economic security and sovereignty.

As a result of the outlined dynamics, countries started prioritising the **reshoring of production capabilities** which creates pressure on companies to take investment decisions that mitigate political risks. While this leaves Europe vulnerable to supply chain disruptions, it also shows the need for stable investment conditions. Europe can provide a reliable framework for investments, which is part of the reasons why Intel initially agreed to invest into manufacturing in Magdeburg, Germany (see case study in Section 4.1.1.2). However, in September 2024, Intel postponed and then later withdrew its plans, highlighting once again Europe's vulnerability.

In summary, since the Chips Act was proposed in 2022, **the world has shifted dramatically**. Initially, the semiconductor industry was marked by a severe shortage, impacting various sectors and highlighting the need for increased manufacturing capacity. However, as new facilities began to take shape, particularly in Asia and the United States, the industry saw an expansion in supply capabilities. At the same time, demand for semiconductors continues to grow, propelled by advancements in technology (especially AI) and the proliferation of digital devices. These shifts have created a more competitive landscape, emphasizing the urgency for the EU to bolster its domestic semiconductor manufacturing capabilities to remain competitive.

4. EVALUATION FINDINGS

4.1. To what extent was the intervention successful and why?

This section assesses the effectiveness, efficiency, and coherence of the Chips Act in line with the methodology foreseen under the Better Regulation Guidelines ⁽⁶³⁾.

4.1.1. Effectiveness

The effectiveness assessment evaluates how far the Chips Act has advanced competitiveness, innovation capacity, and resilience in the EU semiconductor ecosystem, and whether its expected causal chain has operated as intended. As outlined in Section 3, evidence shows **the Act has delivered many foundational outputs**, including over EUR 80 billion in public and private investments mobilised under Pillar II and the establishment of a Member State–Commission coordination mechanism under Pillar III via the ESB. These developments indicate that the organisational infrastructure needed to support Europe’s semiconductor ambitions is largely in place.

However, **translating these outputs into results and impacts will take more time**. The Act entered into force only in September 2023, and long development timelines for pilot lines, the design platform, and new fabs mean many capabilities remain early-stage. Structural barriers (such as skills shortages, lab-to-fab transition challenges, and limited demand-side mechanisms) also hinder uptake. Consequently, although the Chips Act has laid essential groundwork and mobilised the ecosystem ⁽⁶⁴⁾, progress towards its intended impacts (reduced dependencies and greater technological sovereignty) is still ongoing. OPC position papers validate these foundational achievements, with stakeholders consistently identifying Pillar I activities (pilot lines, competence centres, and start-up support) as having strengthened Europe’s innovation infrastructure and supported technological capacity building, citing concrete examples including support for start-ups and local benefits such as job creation ⁽⁶⁵⁾.

4.1.1.1. Pillar I

The effectiveness assessment of Pillar I examines progress in strengthening the EU’s semiconductor research, design, and innovation base. The Initiative introduced new EU-level instruments and structures; **without the Chips Act, support would likely have remained limited to the former KDT JU with fewer strategic priorities**. Mobilising vast national and EU resources has enabled pilot lines, competence centres across all Member States, and shared design and technology infrastructures together forming a long-term framework for advanced capabilities, including design and quantum technologies.

Although most impacts will materialise later, **these foundations significantly expand the EU’s capacity to support semiconductor innovation**. OPC results show that 89%

⁽⁶³⁾ European Commission – Better Regulation Guidelines and Toolbox (https://commission.europa.eu/law/law-making-process/better-regulation/better-regulation-guidelines-and-toolbox_en).

⁽⁶⁴⁾ ZVEI, <https://www.zvei.org/en/press-media/publications/towards-a-european-chips-act-20>

⁽⁶⁵⁾ Position papers submitted to the consolidated public consultation of the review of the Chips Act, September–November 2025. Stakeholders provided positive assessments of Pillar I’s contribution to innovation infrastructure. See also the Synopsis Report.

of respondents reported that the Initiative partially or fully meets its research and innovation objectives ⁽⁶⁶⁾. However, translating outputs into industrial results remains at an early stage: pilot lines are not yet fully operational, competence centres launched only in 2025, quantum pilot lines are being established, and the design platform will be operational in mid-2026. Thus, while foundational assets are in place, further completion, strengthening, and industrialisation are essential to achieve long-term competitiveness and reduced strategic dependencies.

Pilot lines

The five technology-specific pilot lines (see Section 2.1.3.1) under Pillar I have made **substantial progress toward building up technological capacities and advanced technology infrastructures**. The five pilot lines represent some of the most innovative technology infrastructures in the world, securing EUR 3.7 billion in total investment, comprising EUR 1.83 billion EU contribution matched by EUR 1.86 billion national co-funding (see Section 3.1.1).

From an institutional perspective, the pilot lines constitute a significant element within the evolving framework of European innovation governance. The joint co-ownership structures established between the Chips JU and participating Member States create **clear accountability mechanisms** that safeguard public investments whilst enabling collaborative research and innovation. National funding mobilisation achieved approximately 1:1 matching ratios with EU contributions (workshop 14).

Assessing whether pilot lines will effectively bridge the **research-to-industry (lab-to-fab) gap** is premature at this stage of implementation. Pilot lines are projected to reach full operational capacity by end-2026. This is a reasonable timeline given the technical complexity of procuring and installing advanced semiconductor manufacturing equipment. Yet, technology transfer is already underway in specific segments of the value chain. Equipment manufacturers and material suppliers are actively using pilot lines to validate and refine their technologies, creating early spillover effects even before full industrial-scale technology transfer to manufacturing facilities materialises. Workshop consultations emphasise that as pilot lines approach full operational status, priorities should focus on industrialisation of existing facilities to maximise industrial impact (workshop 14). OPC responses suggest that further industrialisation of pilot lines could be supported through State-aid framework reform (GBER revision) and sustained funding support, while end users highlighted the importance of market-driven orientation from the outset ⁽⁶⁷⁾.

Despite the early stage of implementation, OPC results show that 59% of respondents indicated that **the five selected pilot lines partially or fully support the transition from lab to fab** ⁽⁶⁸⁾. Notably, research and technology organisations – who are the

⁽⁶⁶⁾ Open Public Consultation survey (N=97), data reflecting the percentage of respondents selecting "Fully meets the objectives" or "Partially meets the objectives" (89 out of 97 responses: 76% partial + 13% fully). Question: To what extent does pillar 1 'Chips for Europe Initiative' of the Chips Act deliver on its objectives?

⁽⁶⁷⁾ Open-ended responses to the consolidated public consultation of the review of the Chips Act, September–November 2025. Stakeholders provided qualitative suggestions for pilot line industrialisation through State aid framework reforms.

⁽⁶⁸⁾ Open Public Consultation survey (N=96), data reflecting the percentage of respondents selecting "Fully meets the objectives" or "Partially meets the objectives" (56 out of 96 responses: 45% partial +

stakeholders closest to pilot line operations – expressed the strongest confidence, with 77% indicating partial or full effectiveness in bridging the lab-to-fab gap ⁽⁶⁹⁾. This positive assessment from those directly engaged with the infrastructures suggests that pilot lines are on track to deliver their intended bridging function.

The implementation of the pilot lines has increased businesses’ interest in R&D projects and, most importantly, encouraged **cross-segment collaboration between RTOs and industrial actors** ⁽⁷⁰⁾. Their effectiveness is visible globally, as Europe’s pilot line approach remains unique compared to R&D programs in the U.S., China, Taiwan, South Korea, and Japan. To maintain this competitive advantage, SEMI Europe recommends to reinforce the pilot line ‘ecosystem’ by improving synergies between RTOs and industry and ensuring faster approval procedures that support effective industrial uptake ⁽⁷¹⁾.

In a nutshell, **pilot lines appear to be well suited** as advanced technology infrastructures enabling technology development and verification. Definitive effectiveness assessment must await full operational deployment and sufficient time for measuring industrial technology transfer. Stronger emphasis on industrialisation and clearer State aid guidance would enhance the pilot lines’ capacity to achieve their bridging objective.

Design Platform

As the platform is still under development, it is **too early to judge its effectiveness**. However, the intervention is well aligned with the underlying problem, and early implementation steps indicate progress towards tackling the structural barriers that have kept Europe stagnant in the fabless market. The platform has delivered on its set-up and structuring, moving from concept to implementation with the selection, under the Chips JU, of a consortium of 12 leading European research players to act as the Platform Coordination Team, and of 9 DETs that will offer application engineering support services to startups.

The platform is explicitly positioned as the **entry point to advanced European design capabilities** and is complemented by a substantial acceleration and incubation programme for fabless IC, photonic, and quantum start-ups and SMEs, with around EUR 220 million of Chips JU funding, to be matched by participating states, and distributed to selected beneficiaries using the infrastructure.

However, as explained in Sections 2.1.3.1 and 3.1.1, the setting up of this platform is particularly complex and involves many different sequential steps. Therefore, user onboarding will only start in the second half of 2026. Consequently, effectiveness can only be assessed in terms of the above explained readiness and alignment (governance, scope, funding, timelines), while concrete impact on user uptake, number of designs

14% fully). Question: To what extent do the five selected pilot lines support the transition from “Lab to fab”?

⁽⁶⁹⁾ Open Public Consultation survey (N=17), data reflecting the percentage of research and technology organisation respondents selecting "Fully meets the objectives" or "Partially meets the objectives" (13 out of 17 responses: 53% partial + 24% fully). Question: To what extent do the five selected pilot lines support the transition from “Lab to fab”?

⁽⁷⁰⁾ Aeneas, EPoSS, Inside, document submitted under the Open Public Consultation, not public.

⁽⁷¹⁾ SEMI Europe, <https://www.semi.org/en/semi-press-release/semi-europe-publishes-30-recommendations-for-a-forward-looking-european-chips-act>

brought to tape-out, and strengthening of Europe's design ecosystem will need to be measured at a later stage.

Quantum chips

The Initiative's objective on quantum chips **contributes to establishing European capacity in an emerging technology domain** where early strategic positioning can shape future competitive advantage. Six consortia were selected for pilot lines covering distinct quantum technology platforms (see Section 3.1.1). This multi-pathway approach addresses technological uncertainty in what could be the future winning quantum technology platform by maintaining openness across development pathways rather than prematurely selecting a single or few quantum technology platform directions.

The programme is designed as a long-term foundational research investment. The programme represents effective integration of quantum objectives into the Chips Act framework. The established architecture provides mechanisms for coordinated European quantum chip development. However, the **pathway from research to industrial deployment** presents challenges characteristic of frontier technology development. Effectiveness in achieving industrial translation will depend substantially on factors beyond the programme's direct control, including the emergence of practical applications and evolution of quantum computing markets. The assessment of effectiveness should be calibrated to realistic timescales, recognising that quantum chips represent a strategic capability-building exercise rather than an intervention expected to deliver short-term competitiveness impact.

Competence centres

Competence centres **enable national/regional SMEs and other companies to access semiconductor expertise and equipment** they cannot independently afford, thereby extending benefits beyond traditional players (Workshop 3, 4). They have been launched in 2025 in all EU Member States and Norway to broaden access to semiconductor expertise, technology infrastructures, and training. Given their recent launch, competence centres need to work on their visibility to attract stakeholders, in particular, SMEs (Workshops 5, 12; Interviews 3, 8).

Some stakeholders across design, manufacturing, packaging, automotive and telecoms noted that expected **benefits from competence centre activities are real but may not scale to match rapidly growing needs** for applied engineering and packaging expertise (Workshops 5, 8, 10; Interviews 7, 11). Technological trends such as AI accelerators, chiplet architectures, and power semiconductors were increasingly shaping industrial priorities. To achieve intended objectives, competence centres must scale their activities, expand applied training, improve communication, and effectively connect SMEs to pilot lines and the European design platform in the coming years.

Overall, the competence centres represent an **essential framework for supporting SMEs, start-ups and research actors**, but their recent launch means that time to reach local industry and, in particular, SMEs and startups was short.

When it comes to **skills**, so far competence centres have not yet started developing education and training initiatives, since such activities require proper investigation and planning prior to actual implementation. Thus, from an effectiveness perspective, **the national competence centres did not yet contribute to enlarge and qualify the talent pool Europe needs** to strengthen its ecosystem and support the Chips Act's objectives.

Only preparatory work such as the Training and Skills Development focus group set up by the Support Action coordinating the competence centres has been undertaken. Conversely, once the network of the competence centres will become fully operational, it will benefit from, build on, and complement the wide range of different initiatives already launched by various DGs of the Commission, as listed in Section 3.1.1.

Chips Fund

The Chips Fund has proven to be **highly effective in supporting innovative semiconductor and quantum startups and scale-ups**, attracting private capital, and addressing key financing gaps along the innovation and growth chain (see Section 3.1.1). The EIC Accelerator thematic Challenge saw its entire EUR 300 million budget fully utilized in less than two years. This highlights strong market demand and the Fund's capability to identify and support high-potential companies in these sectors. However, it also highlights that **the budget allocated to the Chips Fund was insufficient considering the demand**. Additionally, semiconductor, photonics, and quantum companies could access the EIC Accelerator open calls, which ensured that also outstanding projects outside the above thematic areas could be funded, with an estimated EUR 500 million in additional grants and equity from 2020 to 2025. Again, strong demand shows that allocated budgets were insufficient.

Similarly, as explained in Section 3.1.1, the **STEP programme has effectively contributed to tackle the structural lack of later-stage risk capital** and supported companies entering capital-intensive expansion. Likewise, within the InvestEU framework, the EIF has through its financial partners extended support to 31 companies strengthening the transition from seed to growth and complementing EIC tools.

While it is premature to assess long-term effects such as market share, industrial capacity, or strategic autonomy, the complete utilization of budgets, robust project pipelines, and coverage of various company lifecycle stages indicate that the initiative is **on track to achieve its goals**. However, rapid budget depletion signifies **insufficient funding**, given the extensive demand in the semiconductor sector ⁽⁷²⁾, including photonics and the burgeoning quantum chip segment. Moving forward, to ensure the effectiveness of the Chips Fund, adequate and consistent funding for scaling fabless semiconductor companies centred on leading-edge chip designs will be crucial.

ECIC – European Chips Infrastructure Consortium

As explained in Section 3, potential consortia implementing actions under the Initiative were given the option to establish an ECIC, a legal instrument modelled closely on the EDICs (European Digital Infrastructure Consortia) created under the Digital Decade Policy Programme ⁽⁷³⁾. ECICs were included in the Chips Act proposal to enhance the effectiveness of cross-border cooperation by offering a streamlined, EU-recognised governance framework. However, the use of EDICs could not be guaranteed at the time because the DDPP had not been decided at the moment the Chips Act was proposed.

⁽⁷²⁾ Open Public Consultation survey (N=96), 28 respondents out of 96 (29%) indicated that despite not having previously applied to the Chips Fund, they will do so in the future.

⁽⁷³⁾ <https://eur-lex.europa.eu/eli/dec/2022/2481/oj/eng>

The accelerated implementation timeline (pilot line calls launched three months after the Act's entry into force) likely limited the feasibility of applying for ECIC status, as consortia focused on preparing technical proposals and relied on familiar legal structures. Although ECIC recognition could have been sought after selection, no applications were submitted, suggesting that expected benefits did not justify the administrative effort. Overall, the ECIC instrument broadens available options and could, in theory, support cross-border project implementation, but its non-use so far shows it has not enhanced the Initiative's effectiveness, though it may still be useful for future large-scale projects.

4.1.1.2. Pillar II

FOAK facilities

Pillar II has been highly effective in triggering a **sharp rise in announced manufacturing investments** from a previously weak baseline, though its impact on EU market share, strategic oversight, and crisis readiness remains in progress. National authorities' targeted survey responses strongly validate the need for EU-level coordination in this area, with 87.5% (21 of 24) agreeing or strongly agreeing that EU-level coordination is necessary for achieving semiconductor sovereignty in investment and manufacturing capacity ⁽⁷⁴⁾. Before the Chips Act's strategy, investment aid for semiconductor fabs was largely impossible outside assisted regions, and EU support focused mainly on R&D rather than large-scale production. As the cost of advanced fabs rose sharply over the past two decades, companies increasingly sought public support to de-risk major capital exposure (support that was readily provided elsewhere). Consequently, Europe's **investments lagged far behind** Asia and the U.S., leading to a prolonged erosion of competitiveness; EU semiconductor **capital expenditure** fell to **about 4%** of the global total and stagnated for over a decade. Only a small number of projects received EU-approved State aid. As indicated in the European Court of Auditors' report, just around EUR 2.1 billion in State aid was awarded from 2013 to early 2022 ⁽⁷⁵⁾. Key European players reported total capital investments of about EUR 8 billion between 2013 and 2018, mainly for brownfield capacity expansion.

The first **IPCEI on Microelectronics** was launched in December 2018; it was the very first use of the 2014 IPCEI Communication, justified by the needs to support this sector beyond early R&D, up to first industrial deployment. The IPCEI played a significant role as a policy instrument and has been an important tool in bridging the gap between advanced research and manufacturing, by allowing support until first industrial deployment, and establishing a broad network of collaborations among EU companies. Further, it contributes to **ecosystem growth**, fostering strong **cross-border collaborations** and closer interactions among businesses, academia, startups, and other R&D partners.

The 2018 IPCEI enabled at least **two new greenfield projects**, from Infineon in Villach (AT, EUR 1.6 billion) and Bosch in Dresden (DE, EUR 1 billion). Bosch declared this to be their biggest single investment in the history of the company, which it could make in

⁽⁷⁴⁾ Targeted survey of National authorities. run by PPMI, October-November 2025. Question: "Investment and manufacturing capacity: To what extent do you disagree or agree that EU-level coordination (rather than purely national action) is necessary for achieving EU's semiconductor sovereignty in each of the areas of the Chips pillars?" N=24.

⁽⁷⁵⁾ https://www.eca.europa.eu/ECAPublications/SR-2025-12/SR-2025-12_EN.pdf

Dresden thanks to the IPCEI ⁽⁷⁶⁾. Furthermore, STMicroelectronics built a new 300mm fab in Agrate (IT) and expanded Crolles (FR), while GlobalFoundries (GF) expanded its fab capacity in Dresden for the FDSOI 22nm node. This led to a total of about **EUR 15 billion** private investments in the period 2013-2021, with an average of EUR 2.1 billion per year.

With the Chips Act, the EU has created a dedicated framework for FOAK facilities with the IPF/OEF status and associated guidance, which resulted in a **large surge of investment**: the Commission has approved State aid for eleven FOAK projects to date, with more than **EUR 32 billion** in combined public and private investments, and additional projects are in the pipeline. These projects span advanced logic, power electronics, SiC, FD-SOI, photonics and advanced packaging, and are located across several Member States, signalling a broad strengthening of Europe's industrial base. This means that the level of investments in semiconductors, with an average of EUR 8.5 billion/year, has risen to a level **five times higher than it was before the Chips Act**. The **ESMC** project exemplifies this shift:

The **European Semiconductor Manufacturing Company (ESMC)** is a joint venture between Taiwan Semiconductor Manufacturing Company (TSMC), Robert **Bosch** GmbH, **Infineon** Technologies AG, and **NXP** Semiconductors N.V under the leadership of TSMC. ESMC will manufacture semiconductors on 300 mm wafers with 22–28 and 12–16 nm node sizes. Production will start in late 2027 and reach full capacity in 2029. The project is on track and will boost Europe's resilience by acting as a strategic buffer against semiconductor supply disruptions. In terms of effectiveness, ESMC will likely have a direct impact on EU resilience as it will produce chips in larger node sizes which are mainly demanded by automotive and other industrial users in the European chips market. In addition, ESMC has pledged to prioritize EU and German orders during potential supply crises and will also serve customers beyond its shareholder base, with a strategic focus on European small and medium-sized enterprises (SMEs) and start-ups.

Public investment triggered by the Chips Act was essential for ESMC, as such capital-intensive projects depend on substantial and predictable public support. ESMC demonstrates that major semiconductor investments are strategic decisions supported by strong regional innovation ecosystems. Saxony's dense network of research organisations, universities, specialised firms, suppliers and technical labour market reduced investor risk and was decisive in ESMC's location choice. The case underscores that sustained public funding, strong innovation ecosystems, and proactive labour-market measures are all critical for building competitive semiconductor manufacturing capacity in Europe.

Therefore, **overall, the intervention has been effective** in mobilising a higher level of investment. The Commission initially aimed to mobilise **EUR 43 billion** in policy-driven investments in support of the Chips Act up to 2030. Taking into account all components contributing to this target, i.e. public and mobilised funding under Pillar I, national support for Pillar II and the IPCEI on Microelectronics and Communication Technologies, **close to 80% of the envisaged volume** now appears to be committed in roughly **40% of the available time**. This acceleration has been facilitated also by the availability of **RRF resources**, with a number of IPCEIs, first-of-a-kind, and Chips JU projects incorporated into national recovery and resilience plans.

⁽⁷⁶⁾ <https://www.bosch-presse.de/pressportal/de/en/come-and-see-the-future-in-dresden-the-new-wafer-fab-is-giving-birth-to-technology-for-tomorrows-world-230016.html>

Given that semiconductor manufacturing facilities typically require 2–5 years from ground-breaking to ramping up production, **it is still too early to observe a measurable impact on Europe’s effective output capacity** and, consequently, on its global market share. Unfortunately, also decisions beyond the Union’s control may have a profound impact, as the Intel case illustrates:

Intel’s proposed semiconductor fab in Magdeburg, Germany, was one of the most ambitious European industrial initiatives in recent years, but ultimately never materialised. Announced in March 2022 in the context of the EU Chips Act, the project intended to manufacture chips at 1.5 nm node sizes and thereby establish Europe as the location of one of the world’s first sub-2 nm semiconductor fabs. Despite the offer of EUR 10 billion in German federal subsidies, the project was paused in September 2024 and eventually cancelled in July 2025. Between 2023 and 2025, Intel experienced financial pressure marked by operating losses and declining market shares and employee cuttings. These financial strains triggered a strategic reassessment of the project under new CEO Lip-Bu Tan, who was appointed in March 2025. Unlike other Intel fabs, Magdeburg was designed as a foundry-only site, and it was unclear if enough demand would exist for its products. The new CEO shifted from the plan of building up foundry capacity toward a more cautious, demand-driven capacity model. Thus, Magdeburg no longer fitted the revised strategy of Intel. The twin project of a back-end facility in Wrocław, Poland, mainly intended to serve the Magdeburg’s production, suffered the same fate. With Intel’s manufacturing costs estimated considerably higher than those of competitor TSMC (based on IDC estimates, 1 Euro of capex spent in Taiwan is equivalent to 1.45 Euro spent in the European Union), the company hesitated to establish a leading-edge site in Europe. Moreover, the lack of committed customers for advanced node chips reflects the misalignment between Intel’s planned production capacities and Europe’s actual semiconductor market and further highlights the need to stimulate industrial demand in advanced node sizes.

In parallel, a **global technology race in semiconductors** has clearly emerged, with the semiconductor industry now treated as a core strategic asset rather than a purely commercial activity. The United States, China, Japan, South Korea and Taiwan – joined by several emerging Asian economies – have all launched ambitious support packages combining large public subsidies, tax credits and regulatory facilitation, pushing worldwide semiconductor investment to unprecedented levels. Therefore, while Pillar II has clearly accelerated the pipeline of large manufacturing projects compared to the pre-Chips Act situation, independent assessments underline that **current investments may be insufficient to close the gap with the US and Asia** ⁽⁷⁷⁾.

Once approved projects become operational, IDC projects that **manufacturing capacity in the Union will increase by more than 38% in absolute terms by 2030**. However, as global capacity is expected to grow at a similar pace, **Europe’s share would remain broadly unchanged at around 8%**. Moreover, because this capacity is concentrated in relatively mature technology nodes, its output has lower added value and profit margins than leading-edge logic (such as AI chips). This implies that, even with the same share of capacity, **Europe’s share of global semiconductor revenues may actually decline**. Another important aspect is the total value in terms of revenues across the various stages of the semiconductor value chain: a 2024 study from IDC requested by the Commission

⁽⁷⁷⁾ Semi Europe – Chips Act report; https://www.semi.org/sites/semi.org/files/2025-11/SEMI_Chips_Act_Report_Full_Report.pdf

found that because of ongoing investments in other regions, **without the Chips Act Europe's share would have fallen from 8.5% to a mere 5.9% ⁽⁷⁸⁾**.

Another aspect to consider is the **strategic oversight on priority investments**: funding for FOAK manufacturing facilities under Pillar II comes solely from Member States, while the Commission provides only guiding principles for the assessment under State aid rules, not an EU budget for factory incentives. As a result, the Commission can assess State aid and grant IPF/OEF status but has **limited ability to steer a coherent EU investment strategy** (such as prioritising technologies, nodes, or locations) or to avoid resource dispersion and subsidy races. This risks a patchwork of nationally driven projects rather than a coordinated EU-wide manufacturing landscape, weakening long-term strategic coherence.

In addition, although semiconductor equipment is covered by the Chips Act, investment and support remain limited due to a perceived **narrow FOAK definition ⁽⁷⁹⁾**, restricting technologies under Pillar II. Facilities to produce semiconductor manufacturing equipment are within scope of the FOAK definition, but **unclear criteria reduce legal certainty** for potential multi-billion-euro projects, risking delays or cancellations. The same applies to key materials (specialty gases, photoresists, polysilicon). Stakeholders therefore call for stronger support to equipment, materials, and components to reinforce Europe's position in the value chain, sustain technological sovereignty, and reduce vulnerability to supply disruptions ⁽⁸⁰⁾. OPC position papers echo these calls, with stakeholders specifically highlighting the importance of strengthening Europe's PCB manufacturing and back-end processing capabilities to complement front-end investments ⁽⁸¹⁾.

Recognition of IPF/OEF status

The formal designation in October 2025 of **four major projects as IPF or OEF** (see Section 3.1.2) was a key milestone. These facilities will combine leading-edge process technologies and vertical integration with obligations to support the Union in crisis situations via priority-rated orders. **This directly serves the pillar's core objective of improving security of supply and resilience in the EU**. At the same time, the number of IPF/OEF designations remains modest relative to the size of the European market and the breadth of potential crisis-relevant facilities. In practice, the procedure has been de facto coupled with the granting of State aid; companies believe that they are expected to obtain (or at least apply for) State aid in order to be considered for IPF/OEF status (see example in the text box below), even if this is not the case.

⁽⁷⁸⁾ Contract: CNECT/2022/MVP/0084, "Semiconductors market data by feature size, sector and region", IDC, September 2025.

⁽⁷⁹⁾ Digital Europe, <https://www.digitaleurope.org/resources/chips-act-2-0-from-emergency-response-to-strategic-industry-development/>; ZVEI, <https://www.zvei.org/en/press-media/publications/towards-a-european-chips-act-20>; ESRA, Position Paper 2025, <https://www.esra-org.eu/#documents>

⁽⁸⁰⁾ SEMI Europe, <https://www.semi.org/en/semi-press-release/semi-europe-publishes-30-recommendations-for-a-forward-looking-european-chips-act>; Technology Industries of Finland, https://teknologiateollisuus.fi/wp-content/uploads/2025/10/TIF_Recommendations_EU_Chips_Act_2.0_271025.pdf. Various major industrial companies in documents submitted to the Call for Evidence, not public;

⁽⁸¹⁾ Position papers submitted to the consolidated public consultation of the review of the Chips Act, September–November 2025. Stakeholders emphasised value chain completeness. See also the Synopsis report.

In May 2024, a semiconductor manufacturing company submitted an application for the status of IPF under Article 15 of the Chips Act. In this case, the relevant Member State did not, in parallel, notify the intention to give State aid to this company in the context of FOAK. The company wanted to obtain the IPF status to signal to investors the company was a validated European company. At that time, the Commission services deemed that as IPFs should be considered FOAK facilities according to Article 13(2), the company was not able to receive the IPF status, including the rights and obligations associated with the label. This interpretation illustrates the unintended consequences of the intertwined FOAK definition and IPF or OEF, hindering the positive effects of receiving such status.

This coupling helps to align incentives but also explains the relatively small pool of labelled facilities and may limit the coverage of the crisis-response toolbox (priority-rated orders) in the event of a major disruption.

Stakeholder feedback on Pillar II implementation indicates positive early traction: OPC results show that 62% of respondents indicated that Pillar II partially or fully meets its objectives of strengthening security of supply and resilience⁽⁸²⁾. More specifically, 70% of respondents indicated that IPF and OEF facilities partially or fully contribute to security of supply, with supply chain actors showing particularly strong support at 74%⁽⁸³⁾.

Label of design centres of excellence

The “design centres of excellence” introduced in the Chips Act were never operationalised. The label emerged late in the legislative negotiations after co-legislators considered and rejected bringing design activities under the FOAK framework, as design facilities do not face comparable capital-intensive barriers. Instead, the label was added simply to reaffirm that design activities were already eligible under existing RDI State aid rules and to provide a symbolic designation mainly for SMEs or competence centres. Although reflecting the strategic importance of chip design, the label offered no new funding, regulatory advantages, or incentives. Unlike IPF/OEF facilities, which receive practical benefits such as fast permitting, the design-centre label was seen as offering **no meaningful added value**, and implementation work was halted.

As a result, **the label did not strengthen Europe’s design ecosystem**: it aligned with policy priorities but provided no usable mechanism, was not applied, and had no impact⁽⁸⁴⁾. This gap indicates that future revisions of the Chips Act should consider more effective, better-targeted tools to support advanced chip design capabilities.

⁽⁸²⁾ Open Public Consultation survey (N=97), data reflecting the percentage of respondents selecting "Fully meets the objectives" or "Partially meets the objectives" (60 out of 97 responses: 57% partial + 5% fully). Question: In your view, is the pillar 2 ‘Security of supply and resilience’ of the Chips Act successful in delivering on its objectives?

⁽⁸³⁾ Open Public Consultation survey (N=95), data reflecting the percentage of respondents selecting "Fully contribute" or "Partially contribute" (67 out of 95 responses: 46% partial + 24% fully). Question: To what extent are ‘integrated production facilities’ and ‘open EU foundries’ contributing to the security of supply of semiconductors and the resilience of the Union’s semiconductor ecosystem?

⁽⁸⁴⁾ Digital Europe, <https://www.digitaleurope.org/resources/chips-act-2-0-from-emergency-response-to-strategic-industry-development/>

4.1.1.3. Pillar III

Governance – ESB

The ESB's tasks, structure, and operations are of a mainly **technical and advisory role**. In its two years of operation, the ESB has addressed several topics in accordance with its statutory duties (Art. 28) ⁽⁸⁵⁾. It has advised the PAB of the Chips JU on the work programme, the IPF/OEF applications, and on international engagements. However, it has not yet examined other mandated areas (IP rights, confidential information, certification of green/trusted/secure products, or crisis tools). Several Member States have also not submitted complete lists of Key Market Actors due to company-level information challenges.

Because no crisis has been declared, the ESB's crisis-governance effectiveness cannot be fully assessed. Still, a Commission tabletop exercise on supply-chain disruptions showed ESB members responding proactively and cooperatively, demonstrating readiness (see Section 3.1.3) ⁽⁸⁶⁾. The ESB has been particularly effective in tasks outside Article 28, serving as a platform for Commission–Member State coordination on semiconductor policies beyond the Chips Act, including national strategies, cross-border impacts (see Nexperia case below), IPCEIs, and the EU Economic Security Strategy.

Overall, **the ESB functions effectively as a governance body**, with a scope already extending beyond its original mandate. A future Chips Act revision could simplify and broaden its mandate and strengthen horizontal cooperation and information flows among Member States and with the Commission ⁽⁸⁷⁾.

Monitoring and crisis response

The monitoring and crisis response pillar has largely been effective in progressing towards the objective of developing an in-depth understanding of global semiconductor supply chains. Pillar III activities aimed to solve the need for systematic monitoring and crisis response. **The outputs were in fact delivered:** the Commission developed an initial list of early warning indicators, established a strategic mapping framework, and coordinated monitoring and crisis response activities through the ESB. However, there are still steps to be taken towards the operational effectiveness of these outputs.

The consultation showed a **misunderstanding about the roles of the different actors in the monitoring and crisis response activities**. While coordination between the Commission and Member States took place via the ESB (including information on possible disruptions, see the Nexperia case below), most of the outputs were not shared with industrial stakeholders. The reason was both confidentiality matters as well as avoiding creating further fear and uncertainty in the supply chain, which might have a spiralling effect of actually worsening a supply disruption/crisis by triggering an artificial spike in demand.

⁽⁸⁵⁾ Agendas and minutes of all meetings are available at <https://ec.europa.eu/transparency/expert-groups-register/screen/expert-groups/consult?lang=en&groupID=3932>

⁽⁸⁶⁾ <https://digital-strategy.ec.europa.eu/en/news/commission-and-member-states-rehearse-coordinated-response-semiconductor-supply-chain-shortages>

⁽⁸⁷⁾ DigitalEurope, <https://www.digitaleurope.org/resources/chips-act-2-0-from-emergency-response-to-strategic-industry-development/>

Achieving systematic monitoring, risk preparedness, and crisis response under Pillar III requires further work. Implementation to date shows the **complexity of global semiconductor supply chains, limited data availability, and the need for action not only by the Commission but also by Member States and industry**. Crisis response also demands **case-specific tools** whose effectiveness is hard to assess without information that becomes accessible only once a crisis is declared. The Commission will therefore continue work through the service contract described in Section 3.1.3.

Monitoring

Monitoring activities delivered strategic-mapping analysis through reports, implemented the SCAN system, and established a semiconductor alert mechanism (see Section 3.1.3). Reports recommended adding specific indicators, as Pillar III monitoring still needs substantial development. "SCAN helps to underpin structural dependencies and to identify early signs of supply chain distress using official data. However, the alert system has been under-used.". Workshop participants noted that monitoring focuses mainly on manufacturers and should extend to distributors and major downstream users, who are critical supply-chain nodes (Workshop 7, 14). National authorities stressed that unclear purposes and use of data discouraged company participation (Workshop 14). Overall, stakeholders view the mechanism as solid but still embryonic.

Despite the EU alert infrastructure, **industry relies on commercial networks for early warnings**. Geopolitical risks and new trade barriers were cited as major operational obstacles, underscoring the importance of monitoring. Yet, only 34% of OPC respondents reported having implemented monitoring systems ⁽⁸⁸⁾. Participants recommended indicators beyond production capacity, covering design, talent, critical materials, and leadership in areas like photonics and quantum technologies (Workshops 7, 13, 14; Workshop 4, 11). This reveals a gap between monitoring's intended focus on disruptions and stakeholders' expectations related to strategic autonomy. Stakeholders also noted uncoordinated, duplicative data requests from Commission services and Member States (Interview 12). Member States described the monitoring framework as complex (Workshop 13).

Crisis response

No crisis stage was activated since the entry into force of the Chips Act. Thus, it is difficult to assess the effectiveness of the crisis response toolbox. The alerts and preventive action phase, leading to the activation of a crisis, was simulated in a tabletop exercise involving the ESB and the Council **Working Party on Competitiveness and Growth (Industry)** ⁽⁸⁹⁾. The exercise clearly showed the importance for the EU to **increase its preparedness and to invest to reduce its dependencies on third countries**. It also showed that **decision-makers need a mandate to collect precise and reliable data** to properly assess supply chain disruptions, even in order to prevent a crisis from materialising.

⁽⁸⁸⁾ Open Public Consultation survey (N=93), data reflecting the percentage of respondents selecting "Yes" to implementation of monitoring systems (32 out of 93 responses). Question: Have you developed or implemented a monitoring system for the semiconductor supply chain in your organization?

⁽⁸⁹⁾ <https://digital-strategy.ec.europa.eu/en/news/commission-and-member-states-rehearse-coordinated-response-semiconductor-supply-chain-shortages>

For the **crisis toolbox**, stakeholders in consultation workshops noted that the practical steps for using it were not clear enough. The main reason for this is that depending on the crisis, the actual implementation of the tools will largely vary. For example, for a specific crisis, using priority-rated orders (PROs) or common purchasing might not be effective. The Commission will follow up with the implementation with internal work and through the service contract explained in Section 3.1.3.

Nevertheless, it must be noted that **Pillar III's effectiveness is somewhat constrained by limited EU visibility into semiconductor supply chains**, weakening crisis preparedness. Despite improved coordination through the ESB and initial early-warning measures, monitoring remains insufficiently integrated across materials, equipment, design tools, and downstream users. Fragmented and sensitive data further restrict the ability to anticipate disruptions, leaving Pillar III with only partial system-level visibility – a limitation exemplified in the **Nexperia case** presented in the box below.

On 30 September 2025, the Dutch Minister of Economic Affairs issued an order under its national legislation (the Goods Availability Act) regarding the semiconductor manufacturer Nexperia. Separately, on 1 October 2025, the Amsterdam Enterprise Chamber of Appeal took interim measures related to the company. Shortly afterwards, the Chinese authorities imposed company-specific export control measures on all Nexperia locations in China. This prevented packaging operations performed by Nexperia in China to be re-imported in Europe (i.e., the wafers produced in Europe are shipped to China for low-cost operations of their assembly and packaging into final products – however, these final products could then not be reshipped to Europe, because of the Chinese export control measures taken). Economic operators in the EU and from close partners (including the U.S., Japan) sounded the alarm regarding the licensing process, shipments delays and halts, and the ramifications for downstream industries. The Chinese government eased export restrictions early November. In December 2025, shipments of available chips has continued but uncertainties remain.

4.1.2. *Efficiency*

The efficiency criterion examines whether the intervention achieved its objectives at reasonable cost and without unnecessary burdens. For the Chips Act, this involves assessing the relationship between resources used (administrative, financial, time) and results achieved (industry uptake, infrastructure deployment, private investment leverage), and identifying unintended cost drivers or duplicative obligations. The analysis considers whether the legislative framework and its implementation were proportionate and streamlined, using cost–benefit analysis, burden-reduction indicators, and comparisons with alternative or baseline scenarios to assess value for money. The overview of benefits and costs presented in Annex III is integrated into the pillar-level analysis below, with Annex III retaining the detailed assumptions and supporting calculations.

As implementation is still at an early stage for several instruments, cost and benefit evidence remains partial and, in some cases, based on indicative estimates (for example standard cost model assumptions for administrative burden). In Pillar II, operating cost data for new fabs are not yet available and some total investment figures are not disclosed, whilst in Pillar III the costs and burdens of crisis measures are inherently uncertain because no crisis stage has been declared. Accordingly, efficiency findings in this section should be read as an initial assessment grounded in available evidence, avoiding conclusions that cannot yet be robustly substantiated.

In the following subsections, efficiency will be examined pillar by pillar, focusing on whether resources were proportionate to results and whether implementation generated avoidable costs or administrative burdens.

4.1.2.1. Pillar I

Pillar I demonstrates **strong efficiency in resource mobilisation and financial leverage**, with instruments delivering substantial outputs relative to inputs. In financial terms, as of November 2025, total EU-level public expenditure committed under Pillar I is around EUR 1,960.5 million (EUR 1,831.2 million for pilot lines, EUR 92.3 million for competence centres, EUR 25 million for the Design Platform, and EUR 12 million for design-related activities), whilst national public expenditure stands at roughly EUR 1,957.3 million for pilot lines and competence centres, broadly matching EU contributions. The most striking efficiency achievement is the approximately 1:1 leverage ratio between EU contributions and national funding for pilot lines, competence centres, and quantum chip pilots. This is particularly remarkable for the case of the competence centres, which prompted an unprecedented EU-wide mobilisation, with all Member States, including those that had never engaged in JU activities, participating and providing funding. Additionally, the Chips JU achieved strong administrative cost-effectiveness in 2023, with total administrative costs representing just 1.09% of operational expenditure, comparing favourably to benchmarks for similar Joint Undertakings.

Beyond financial leverage, market uptake provides complementary evidence of **efficient resource targeting**. The Chips Fund demonstrated strong demand, with the EIC Accelerator thematic allocation fully deployed in less than two years. This strong uptake occurred within the context of a EUR 300 million EIC allocation and EUR 250 million InvestEU dedicated capacity for semiconductors, validating that the well-documented European venture capital gap for semiconductor startups persists and that demand substantially exceeds available resources. By relying on existing instruments and governance structures, notably the EIC Accelerator (both thematic and open calls), the STEP programme and the InvestEU/EIF framework, the Chips Fund has leveraged established procedures, expertise and synergies. In cost terms, the Chips Fund adds EUR 425 million in EU contribution: EUR 300 million via the EIC Accelerator (EUR 62 million in grants and EUR 238 million in recommended equity investment to 24 startups through the dedicated Semiconductor and Quantum Technologies challenges) and EUR 125 million via InvestEU (EUR 68 million signed or approved with four financial partners, resulting in EUR 116 million in equity investment to 31 companies)

The Chips Fund is designed to crowd in private investments with a leverage factor of 3 to 5. This strongly suggests that objectives have been pursued at a reasonable cost for the EU budget and with limited additional administrative burden for both the institutions and beneficiaries. Available burden estimates indicate that administrative effort is nonetheless material for applicants: a standard cost model suggests an average of around 70 person-days per Chips Fund beneficiary for applications, due diligence and reporting (about EUR 30,000 per funded project, excluding costs for unsuccessful applicants), whilst across Pillar I grants an estimated 10-20 person-days per application (midpoint 15 days) implies around EUR 3 million in administrative and compliance costs for 514 participants in 44 projects over four years (indicative).

At the same time, the **strong demand and rapid budget consumption of the Chips Fund** suggest a highly competitive environment, which can be seen as efficient in terms

of selection quality, but also implies that **many worthy projects remain unfunded**. This underlines that the main constraint is budgetary rather than operational inefficiency. Overall, taking into account leverage effects of private funding, use of existing structures, and the absence of obvious deadweight or underuse, the intervention appears to have delivered its early objectives at a reasonable cost and without evident resource wastage. At this stage, the efficiency assessment is also supported by early output evidence reported elsewhere in the evaluation (for example the operationalisation of pilot lines and competence centres), although full cost-effectiveness will depend on sustained utilisation rates and longer-term outcomes.

Deployment timelines varied across Pillar I components, but generally demonstrate satisfactory efficiency given the scale and institutional novelty of the instruments involved. Pilot lines – which are complex cross-border technology infrastructures with substantial equipment procurement requiring coordination across multiple Member States – progressed from call launch to grant agreement signing within just ten months. Competence centres achieved operational status across 28 countries within timeframes stakeholders described as reasonable (workshop 14). The Design Platform experienced notably longer implementation timelines due to structural complexity and a novel cloud-based virtual infrastructure, though these extended timescales remain proportionate to the scope and ambition of establishing fundamentally new European capacities in design. For quantum chip pilots, six Framework Partnership Agreements have been signed without financial commitment, with first commitments expected at the beginning of 2026, which limits the extent to which cost-effectiveness can be evidenced at this stage beyond readiness.

Whilst the fundamental structure of separate funding programmes under the current MFF cannot be easily altered, **improved guidance and harmonised timelines** could reduce administrative burden. The efficiency gains from such procedural improvements would benefit all stakeholder groups, with proportionally larger benefits for SMEs and academic actors facing higher relative coordination costs.

4.1.2.2. Pillar II

As explained in Section 3.1.2, Pillar II of the Chips Act has made significant strides in **mobilising substantial resources to enhance Europe's semiconductor capabilities**. The mobilisation of over EUR 80 billion in investments, including under an IPCEI and of Pillar II, demonstrates the Act's capacity to attract large-scale financing and support the objective of expanding Europe's semiconductor production base. OPC results show that 62% of respondents indicated that Pillar II of the Chips Act was (partially or fully) successful in delivering on its objectives (see Section 4.1.1.2), and that 71% of respondents agreed partially or fully that the Chips Act Pillar II has made the EU a more attractive location for semiconductor manufacturing) ⁽⁹⁰⁾.

The administrative burden of **prolonged approval processes** has emerged as a significant challenge in Pillar II's implementation ⁽⁹¹⁾. The extensive timelines for

⁽⁹⁰⁾ Open Public Consultation survey (N=96), data reflecting the percentage of respondents selecting "Fully" or "Partially" (69 out of 96 responses: 61% partial + 10% fully). Question: To what extent had the European Chips Act Pillar 2 on security of supply and resilience, made the EU a more attractive location for semiconductor manufacturing?

⁽⁹¹⁾ ZVEI, <https://www.zvei.org/en/press-media/publications/towards-a-european-chips-act-20>

permitting approvals have become a substantial cost factor, particularly in comparison to other more efficient systems. For example, Interview 5 with industry representatives states that **while State aid approval in the EU takes 10-12 months** ⁽⁹²⁾, **the same procedure takes 6 months in South Korea and Taiwan, and even less than one month in other regions**. Nevertheless, in the case of IPF/OEF the Commission increased the procedural efficiency of the intervention with the publication of guidelines ⁽⁹³⁾. Whilst direct EU-level financial costs are limited (public investments are made by Member States and the EU role is largely regulatory and supervisory), these time costs can materially affect overall efficiency by delaying delivery and increasing financing and opportunity costs for capital-intensive projects.

Efficiency achievements in Pillar II are mainly impacted by **fragmented coordination across the EU, national, and industrial stakeholders**. Certain stakeholders have pointed out some inefficiencies in the administrative processes, such as extended timelines for State aid approvals (Workshops 4 and 9). Potential changes in the administrative procedures could be envisaged. Some stakeholders present at Workshop 4 as well as ESIA, ZVEI and DigitalEurope ⁽⁹⁴⁾ propose the establishment of a centralised EU semiconductors budget (inspired by the Draghi report) that could unify decision-making and expedite strategic investments and give ‘top ups’ in IPCEIs and FOAK projects. Budget dedicated to semiconductors under the upcoming European Competitiveness Fund (ECF) would enable fast funding for highly strategic projects ⁽⁹⁵⁾. Indicative administrative-cost estimates for the State aid lifecycle suggest recurring compliance and processing effort for firms and administrations (for example, stylised estimates of around 50 person-days per beneficiary per year for firms and comparable order-of-magnitude effort for EU and national authorities), but the evidence base remains incomplete and does not capture operating costs of new facilities, which are not yet available.

Another element that affects the implementations efficiency is the **limited staffing and resources** dedicated to the implementation of the Chips Act (around 20 Commission staff, as compared to initially around 120 staff in the American CHIPS Act office). Nevertheless, the interaction between the Commission and notifying parties reflects efforts to enhance coordination and technical rigour. For both FOAK and IPCEI cases, DG COMP and DG CNECT work in close coordination; the former engaging in discussions with Member States during pre-notification and notification stages whilst the latter provides technical assessment and evaluation of spillover effects.

⁽⁹²⁾ Ibidem and Interview 5

⁽⁹³⁾ Communication (C/2024/4911) from the Commission on the Guidance on the application for an undertaking to obtain the status of integrated production facility and open EU foundry pursuant to Article 15 of the Chips Act Regulation (EU) 2023/1781

⁽⁹⁴⁾ ESIA, https://www.eusemiconductors.eu/sites/default/files/2025.09.12_ESIA-Position_EUChipsAct2.pdf; ZVEI, <https://www.zvei.org/en/press-media/publications/towards-a-european-chips-act-20>; DigitalEurope, <https://www.digitaleurope.org/resources/chips-act-2-0-from-emergency-response-to-strategic-industry-development/>

⁽⁹⁵⁾ Semi Europe, https://www.semi.org/sites/semi.org/files/2025-11/SEMI_Chips_Act_Report_Full_Report.pdf

4.1.2.3. Pillar III

Pillar III's efficiency is shaped by a paradox: its value lies in preparedness even when its tools are never used ⁽⁹⁶⁾. Because no crisis has been declared, **assessing the efficiency of this pillar can only be done with inherent limitations**. In cost terms, Pillar III currently entails modest running costs linked to monitoring and coordination: indicative estimates suggest annual business compliance costs of around EUR 0.6 million (around 50 firms each spending roughly 160 hours per year), EU-level monitoring costs of around EUR 1.5 million (including FTE and analytical support), and national administrative costs of around EUR 1.5 million in total across Member States (modelled).

The ESB's set-up and Commission-led coordination have been proportionate to the value created. It has provided a plenary forum for Member States to exchange views and has spawned expert groups such as the situational-analysis taskforce ⁽⁹⁷⁾ facilitating more agile workflows. The ESB was established on time and within its expected cost. However, given that several crisis-stage tools have not been activated, this proportionality finding should be treated as an initial assessment focused on preparedness outputs rather than a definitive judgement on cost-effectiveness.

A recurring recommendation is to **strengthen exchanges between the ESB and industry** (Workshop 7, ESIA), reflecting the incomplete implementation of an anticipated high-level industry body. This dialogue could improve once the Steering Committee foreseen in the Terms of Reference for the Industrial Alliance is established. A first step has been the formation of a high-level Industry Advisory Group as a subgroup of the Industrial Alliance which will produce in March 2026 a report on industry priorities for the Chips Act revision before transitioning into the foreseen Steering Committee of the Alliance. Even so, bringing together experts from all Member States and observers has helped build relationships, improve information flows, and support consultations. From an efficiency perspective, more structured industry exchange is also relevant to keeping monitoring requests proportionate and reducing duplication, thereby limiting compliance costs.

Furthermore, the Commission is **using the ESB to develop crisis coordination mechanisms** in close collaboration with the Member States to enable the Union to react to crises. To increase the coordination efficiency and clarify the roles of different actors, the Commission organised a tabletop exercise on coordinated response to a semiconductor supply chain crisis (see Section 3.1.3).

At the same time, the Commission-internal organisation of the obtained data to glean insights in times of crisis has not been tested yet. However, pre-crisis stage supply chain challenges (see Nexperia case in Section 4.1.1.3) have shown that not only the Member States but also the Commission are facing **challenges regarding their ability to obtain and work with data in a more timely and efficient manner**. Similarly, Workshop 7 participants reported that the lack of a shared platform to monitor semiconductor value

⁽⁹⁶⁾ Assessment in this subsection is based on Workshop 7, Workshop 3, ESIA, and the European Economic and Social Committee.

⁽⁹⁷⁾ The Task Force on Situational Analysis is a subgroup of the European Semiconductor Board composed of a small number of experts volunteered by 6 Member States. It assists the Commission in the collection and analysis of evidence regarding rapidly developing situations or imminent risks to economic security in the field of semiconductors, when coordinating 27 Members would be too slow.

chains across Europe creates challenges for EU crisis preparedness. At the same time, companies report that they **remain cautious about sharing supply chain information** due to competition concerns, complicating data aggregation and sharing whilst protecting sensitive information. Increasing the administrative abilities of the Commission to request and handle data in a preventive stage would save time and resources should a crisis occur since the necessary time and caution in establishing the tools would pre-empt failures in an ad hoc set-up during a crisis. This also has a direct efficiency implication: improving data-handling processes and confidentiality safeguards in the preventive stage can reduce the risk of costly, duplicative or low-quality data collection during a crisis.

Finally, industry representatives express concern that the **crisis-toolbox measures could impose heavy administrative burdens**. However, these tools are intended for use only in critical situations, where such burdens would be justified and applied solely when necessary and proportionate to keep essential sectors functioning. Since these measures have not been used, their administrative and opportunity costs remain prospective and should not be treated as observed efficiency outcomes at this stage of implementation.

4.1.3. Coherence

This section assesses the coherence of the Chips Act internally, across its three pillars, and externally, in relation to other EU initiatives, Member State actions, and wider EU policy priorities.

4.1.3.1. Internal coherence across the three pillars

The Chips Act is structured around three interlinked pillars that were designed to operate as a single policy pipeline, connecting upstream research and development (Pillar I), industrial deployment (Pillar II), and crisis preparedness (Pillar III). Governance arrangements through the ESB were designed to ensure coherence across the three pillars, including through common oversight and coordinated crisis response.

From a conceptual perspective, **the pillars are coherent and mutually reinforcing**. Pillar I is intended to generate the research and development outputs that could become the bases for manufacturing investments under Pillar II, while Pillar III protects both through monitoring and emergency measures. This architecture was explicitly conceived to address the structural gap between publicly funded research and industrial deployment.

4.1.3.2. External coherence with EU, national, and regional initiatives

Coherence with EU initiatives

The Chips Act is broadly coherent with EU initiatives pursuing similar objectives, notably the Digital Europe Programme (DEP), Horizon Europe (HE), the Critical Raw Materials Act (CRMA), but also European Regional Development Fund (ERDF), European Social Fund Plus (ESF+), Connecting Europe Facility (CEF), InvestEU, Erasmus+ and the Recovery and Resilience Facility (RRF). This is confirmed by policy-document analysis and stakeholder consultation. From the abovementioned initiatives, the Chips Act is particularly coherent with DEP and HE, which serve as the two funding backbones of Pillar I. **DEP** provides horizontal digital infrastructures, while **HE** supports upstream research, piloting and demonstration. Moreover, the Act is also complementary

to the **CRMA** ⁽⁹⁸⁾, as both pursue strategic autonomy by addressing different segments of the value chain: the Chips Act focuses on semiconductor design and manufacturing, while CRMA targets critical raw materials.

InvestEU provides part of the financing backbone of the Chips Fund, bridging the gap between grants and commercial investment. Stakeholders noted navigation difficulties between the Chips Fund and EIC support mechanisms (Workshop 14), indicating practical coherence issues in funding access. Coherence with **IPCEIs**, namely IPCEI ME/CT, is high. IPCEIs continue to support high-risk cross-border R&D and first industrial deployment, while the Chips Act complements this through permanent capacity building and resilience mechanisms. Stakeholders confirmed alignment and synergies between the two instruments (Interviews 1, 6 and 9). When it comes to the EU programmes listed in Annex III of the Chips Act, there is a broad coherence with ERDF, ESF+, CEF, Erasmus+ and the Recovery and Resilience Facility (RRF). These instruments support complementary parts of the value chain, from regional financing to skills.

Coordination will be needed between the Chips Act and the proposed **European Competitiveness Fund** (ECF) or the upcoming **Quantum Act**. Coherence with the latter will provide an opportunity to establish a comprehensive European quantum policy frameworks that leverages synergies across multiple instruments.

The Chips Act is coherent with the EU's **strategic autonomy, economic security, and competitiveness agendas**. It aligns with the European Economic Security Strategy, Dual-Use export controls, the Foreign Subsidies Regulation, and the Strategic Technologies for Europe Platform (STEP). Together, these instruments reduce strategic dependencies and reinforce industrial capacity. The Act is coherent with EU competition and industrial strategy, as reflected in industrial strategies and the Draghi Report, and it complements digital and green frameworks.

Coherence with national initiatives

At national level, coherence is generally high. Policy reviews confirm that national strategies in Germany, France, the Netherlands, Portugal, Ireland, Finland and Czechia explicitly refer to the Chips Act and align governance structures and co-financing instruments. The importance stakeholders place on coordination is reflected in OPC results: 86% of respondents indicated that the Chips Act has contributed adequately, well, or very well to increasing governance and coordination between national and regional authorities and agencies ⁽⁹⁹⁾.

Furthermore, stakeholder feedback indicates broad recognition that **strengthened coordination is necessary**. OPC results show that 88% of respondents agreed that dispersed national strategies require EU-level coordination to ensure Member States

⁽⁹⁸⁾ <https://eur-lex.europa.eu/eli/reg/2024/1252/oj/eng>

⁽⁹⁹⁾ Open Public Consultation survey (N=67), data reflecting percentage of respondents rating coordination as "Adequately", "Well", or "Very well" (58 out of 67 responses: 61% adequately + 16% well + 9% very well). Question: To what extent has the Chips Act contributed to increase the governance and coordination between different national and regional authorities and agencies?

contribute efficiently and coherently to strengthening the semiconductor value chain ⁽¹⁰⁰⁾. This strong consensus validates the Act's coordinated governance approach.

Coherence with regional initiatives

At regional level, regional stakeholders reported limited inclusion in governance processes and limited involvement in implementation. However, it is important to note that the reasons for fragmentation go beyond the scope of the Chips Act. Workshop 4 with the European Semiconductor Regions Alliance (ESRA) ⁽¹⁰¹⁾ showed that the Chips Act has in many cases strengthened and empowered the regional industrial policies of regions with a background in semiconductors, and that it offered unique opportunities by complementing existing national and EU instruments. In fact, ESRA credits its own creation, and its work on exchanging good practices and representing regional instances, to the political impulse given by the Chips Act. OPC position papers from regional stakeholders further emphasise opportunities to strengthen multi-level coordination, noting that success depends on close collaboration between research, companies, pilot lines, centres of excellence, and public policy at all governance levels ⁽¹⁰²⁾.

4.2. How did the EU intervention make a difference and to whom?

4.2.1. EU added value

This criterion assesses the EU added value of the Chips Act. Because semiconductor value chains are cross-border and no Member State is self-sufficient, **EU action aims to avoid duplication, achieve scale, and coordinate investments**. The assessment examines how effectively the Act has pooled resources, aligned priorities, strengthened cooperation, reduced fragmentation, and improved the EU's collective capacity to face global competition and supply-chain risks, delivering benefits beyond national initiatives.

4.2.1.1. Pillar I

Pillar I has created **transnational infrastructures beyond the reach of individual Member States**, offering pan-European access to five pilot lines and six quantum chip pilots across 13 countries. This avoids redundancy, ensures broad technological coverage, and enables efficient prototype production. Without the EU framework, Member States would face costly, duplicative investments with low utilisation, while smaller countries would lack access to advanced facilities. The design platform and competence centres further support cross-border expertise sharing.

OPC results strongly confirm this EU added value: 70% of respondents agreed Pillar I increased EU competitiveness through enhanced design, systems integration, and

⁽¹⁰⁰⁾ Open Public Consultation survey (N=94), data reflecting percentage of respondents selecting "Strongly agree" or "Agree" (83 out of 94 responses: 38% strongly agree + 50% agree). Question: Do you agree with the following statement: "Dispersed national strategies require EU-level coordination strategies to ensure that Member States contribute efficiently to the strengthening of the EU's semiconductor value chain in a coherent and complementary fashion."

⁽¹⁰¹⁾ <https://www.esra-org.eu/>

⁽¹⁰²⁾ Position papers submitted to the consolidated public consultation of the review of the Chips Act, September–November 2025. Regional stakeholders highlighted coordination opportunities. See also the Synopsis report.

production capabilities, and 78% agreed it enabled the development and deployment of cutting-edge semiconductor and quantum technologies (¹⁰³).

4.2.1.2. Pillar II

The EU added value of Pillar II lays in **de-risking large-scale investments in compliance with State aid rules** and allowing for **faster national permitting procedures**. The Chips Act Communication explains the principles for the case-by-case assessment of State aid measures supporting new semiconductor manufacturing facilities directly under Article 107(3)(c) TFEU. In particular, the Commission may take into account the fact that projects are FOAK in the EU and will verify that the aid does not exceed the project's funding gap (taking into account the counterfactual scenario in the absence of aid when relevant). Such case-by-case assessment of manufacturing aid directly under the Treaty is exceptional as manufacturing aid is typically only allowed in assisted regions. These measures under Pillar II complement support measures for R&D&I activities and IPCEI projects up to first industrial deployment, where projects have to demonstrate their uniqueness at global level. Coordination sought to prevent a subsidy race among Member States while creating spillovers and conditions attractive enough to compete globally for semiconductor manufacturing capacity. Moreover, the EU added value of IPF/OEF facilities mainly lies in their commitment to accept and prioritise crisis-relevant orders in times of crisis.

However, Pillar II gives the Commission **limited tools at the EU level for steering manufacturing investments**, since public support mainly comes from Member States. As a result, investments have naturally developed in a decentralized manner, with firms often choosing locations based on national funding conditions rather than broader EU strategies, possibly impacting efforts to address value chain gaps at the Union level.

4.2.1.3. Pillar III

Under Pillar III, the ESB was created to coordinate monitoring, risk preparedness, and crisis response at the EU level, a feat not possible at the national level due to fragmented priorities. The ESB lowers transaction costs and enhances communication across Member States, providing distinct EU-level value. It strengthens economic security for all, including smaller Member States less involved in the semiconductor industry, by providing resilience and insights into the value chain. The ESB offers agility for quick, coordinated action during disruptions and serves as a point of contact for industry stakeholders. Through crisis response tools, the ESB enhances collective Member State action, providing EU-added value. These efforts streamline responses to crises, minimizing fragmentation risks and securing Europe's economic stability. Coordinated EU-level action was strongly supported by the OPC results: 88% of respondents agreed or strongly agreed that dispersed national strategies require stronger EU-level coordination to ensure Member States contribute coherently to the semiconductor value chain, and only 2% disagreed (see footnote 100). The targeted survey results also show

(¹⁰³) Open public consultation survey (N=96), data reflecting the percentage of respondents selecting "Fully meets the objectives" or "Partially meets the objectives" to Question Q6. To what extent does pillar 1 'Chips for Europe Initiative' of the Chips Act deliver on its objectives? Options: "To reinforce advanced design, systems integration and chip production capabilities in the Union, thereby increasing the competitiveness of the Union" and "To enable development and deployment of cutting-edge semiconductor technologies, next-generation semiconductor technologies and cutting-edge quantum technologies and the innovation of established technologies".

high level of agreement on the need for EU-level coordination in order to achieve sovereignty for the EU in semiconductors (ranging 75-86 % depending on stakeholder group). OPC position papers similarly call for strengthened international partnerships with key semiconductor-producing nations, proposing more formalised cooperation mechanisms and risk-based frameworks to enhance Europe's global semiconductor collaboration ⁽¹⁰⁴⁾.

4.3. Is the intervention still relevant?

4.3.1. *Relevance*

The relevance criterion assesses whether the Chips Act's objectives and intervention logic **remain suited** to current needs, technological developments, market conditions, and geopolitical realities. It examines whether the Act still addresses its original problems, how these have evolved, and whether new challenges have emerged. It also evaluates whether the Act's instruments align with stakeholder needs across the value chain and whether any gaps or new priorities exist.

4.3.1.1. *Pillar I*

Pillar I addresses fundamental capability gaps in the EU semiconductor ecosystem that have become even more urgent since the Chips Act's adoption. The strategic relevance must be **assessed against the counterfactual situation**: without the Chips Act, the EU would possess only the KDT Joint Undertaking supporting bottom-up research projects without political steering or strategic coordination. The entire architecture that Pillar I has established would simply not exist.

The response of Member States in developing **national semiconductor strategies** shaped by the Chips Act provides tangible evidence that the intervention corresponds to genuine needs at both national and European levels. In several cases, parts of the Chips Act structure are often directly mirrored in national strategies, demonstrating alignment between European intervention and Member State priorities. For many Member States, competence centres represent the first engagement with semiconductor policy, catalysing strategic thinking and capacity development that would not have occurred without EU-level framework and co-funding.

Pilot lines translate EU research excellence into industrial deployment. The lab-to-fab gap persists as a major drawback for the EU semiconductor sector despite our excellence in R&D, with fragmentation across the EU reducing the speed and impact of technology transfer. The EU's strengths in research and technology organisations allow for industrial-scale prototyping infrastructure to enable technology transfer, a need that has not diminished since the Chips Act's adoption. Pilot line relevance is evidenced by the strong demand received, in the form of industry access requests, even before their official launch. However, survey evidence suggests that structural barriers to technology transfer persist: nearly half of RTO respondents (47%, 8 of 17) reported significant barriers to transferring research results into industrial application. R&I alone cannot secure

⁽¹⁰⁴⁾ Position papers submitted to the consolidated public consultation of the review of the Chips Act, September–November 2025. Stakeholders provided recommendations for international cooperation frameworks. See also the Synopsis report.

European competitiveness without complementary manufacturing capacity, identifying gaps in packaging, substrates, PCB production and system-integration activities (Workshops 7, 8 and 11, Interviews 8, 11; position paper – Global Electronics Association ⁽¹⁰⁵⁾).

The Design Platform addresses the EU's weakness in chip design capabilities, where the continent lags behind global competitors despite strong electronics and systems integration sectors. Technological trends such as AI accelerators, chiplet architectures, and power semiconductors increasingly shape industrial priorities, intensifying demand for design expertise. Since 2023, market growth has been increasingly driven by AI-related applications, particularly processors and memory for data centres, reinforcing the strategic relevance of strengthening leading-edge design and integration capabilities in the Union. Despite ongoing efforts, the Europe's design deficit persists, and EU-level intervention remains necessary to close capability gaps that national programmes have not resolved (workshop 14).

Competence centres continue to be relevant thanks to their semiconductor-focused activities across all Member States. This unprecedented geographical reach addresses national/regional capability building and SME access that national programmes alone could not achieve given the concentration of semiconductor expertise in some Member States. Just like shared pilot lines expanded access to advanced prototyping capability, competence centres have strengthened collaboration and training (Workshops 3, 5 and Interview 7). A *Coordination and Support Action* ensures knowledge sharing among competence centres rather than isolated national efforts. Given that most competence centres only began operations in 2025, their longer-term impacts on technological capability and competitiveness cannot yet be evidenced, but early outputs indicate strong alignment with identified needs.

Skills emerged as a cross-cutting constraint ⁽¹⁰⁶⁾: stakeholders across design, R&I, manufacturing, packaging, automotive, telecoms and materials reported persistent shortages in applied semiconductor engineering, packaging and system-integration skills. The OPC results confirm this: the majority of respondents (94%) fully agreed or agreed that the European semiconductor industry faces serious talent shortages, posing a major bottleneck for growth and innovation, which requires investment in attraction, skilling, reskilling, and training policies ⁽¹⁰⁷⁾.

Workshop 14 with the Chips JU Public Authorities Board emphasised that long-term vision and continuity should take priority over launching new initiatives. National authorities stressed that sustained commitment to existing instruments creates essential consistency for extended development processes that are characteristic for semiconductor technology. Pillar I remains highly relevant to address the persistent capability gaps that require European-level action. These are design weaknesses, lab-to-fab gaps, fragmented competence centres and insufficient venture capital. Addressing our capability gaps is

⁽¹⁰⁵⁾ Global Electronics Association, <https://emails.ipc.org/links/GlobalElectronicsAssocChipsActPlusPosition.pdf>

⁽¹⁰⁶⁾ European Semiconductor Regions Alliance, Position Paper 2025, <https://www.esra-org.eu/#documents>

⁽¹⁰⁷⁾ Open public consultation survey (N=94), data reflecting the percentage of respondents selecting “Strongly agree” or “Agree” (89 out of 94 responses). Question: Do you agree with the statement that the European semiconductor industry faces serious talent shortages requiring investment in attraction, skilling, reskilling and training policies?

even more urgent given intensifying global competition and geopolitical technology dynamics.

4.3.1.2. *Pillar II*

This section assesses whether Pillar II remains aligned with Europe's evolving industrial needs. Stakeholders have confirmed the relevance of the Chips Act's core objectives of reinforcing domestic manufacturing capacity and reducing strategic dependencies. Data from the OPC supports that IPFs/OEFs partially or fully contribute to the security of supply of semiconductors and the resilience of the Union's semiconductor ecosystem (see footnote 83). However, many considered the original design to be increasingly misaligned with current vulnerabilities, as it was perceived as focusing primarily on front-end fabrication while overlooking dependencies in substrates, specialty chemicals, advanced packaging, RF and power modules, PCBs and EMS (Workshops 2, 7, 9, 11; Interviews 8, 9, 10).

Several stakeholders argued that maintaining minimum viable capacity and skills had become more relevant than achieving a global 20% market share (Workshops 10, 11, 15), pointing to a growing mismatch between Pillar II indicators and industrial realities ⁽¹⁰⁸⁾. OPC position papers validate this perspective, with industry stakeholders emphasising that production capabilities must be accompanied by framework conditions that support end-market development for semiconductors made in the EU ⁽¹⁰⁹⁾.

Finally, stakeholders identified weak domestic demand as a growing constraint that is specific to advanced-node production ⁽¹¹⁰⁾. While global demand for semiconductors remains strong, market leaders nowadays tend to locate cutting-edge fabrication where sustained local demand exists, as production follows demand. In case of a severe crisis, for instance an earthquake destroying advanced production facilities on Taiwan, it is very likely that countries will limit domestic production for domestic consumption via export controls and other measures. Considering potential exposure during crises, and to reduce their dependencies on other parts of the world, countries such as the United States and Japan have invited the world leader in advanced nodes manufacturing, TSMC, to set up advanced node facilities on their soil. Thanks to sufficient local demand, TSMC agreed to do so.

The Union remains dependent on third countries for advanced-node manufacturing capacity. In the event of a severe supply-chain disruption or geopolitical crisis, export controls or prioritisation of domestic markets could limit EU access to such production. In case of a crisis, the Union may be faced with a situation where its industries do not have the possibility to access advanced nodes production. Demand side measures, such as demand aggregation, may therefore be needed to put in place sufficient local demand to convince market leaders to establish advanced production facilities in the Union and/or to justify public-private investments in small-scale advanced nodes production in Europe.

⁽¹⁰⁸⁾ This is echoed by DigitalEurope, who states that "Europe's next targets must reflect strategic relevance, not production quotas", <https://www.digitaleurope.org/resources/chips-act-2-0-from-emergency-response-to-strategic-industry-development/>

⁽¹⁰⁹⁾ Position papers submitted to the consolidated public consultation of the review of the Chips Act, September–November 2025, including contributions from ASML and other industry stakeholders. See also the Synopsis report.

⁽¹¹⁰⁾ ZVEI, <https://www.zvei.org/en/press-media/publications/towards-a-european-chips-act-20>

In this context, such demand-side measures were considered relevant to anchor advanced production capacity in the Union and reduce strategic dependency (Workshops 4, 10, 12; Interviews 2, 3, 11). A public-sector investor further warned that without credible demand projections and production baselines, monitoring and crisis-response mechanisms under Pillar III risk being weakened, as they depend on realistic assumptions about available capacity (Interview 2).

These considerations suggest that Pillar II remains relevant to Europe's industrial objectives, but that its original focus and performance indicators may not fully reflect evolving technological and geopolitical realities.

4.3.1.3. *Pillar III*

Pillar III's focus on systematic monitoring, risk preparedness and crisis response remains relevant, as supply chain dependencies persist. Geopolitical tensions, trade restrictions, export-control regimes and subsidy competition have further increased the strategic importance of systematic monitoring and preparedness mechanisms. Supply chains have become instruments of economic security policy, heightening the relevance of coordinated EU-level action. As discussed in Section 3.2, global value chains have changed dramatically. Therefore, European companies dependent on semiconductors have reported early improvements in coordination that may support risk mitigation through the Chips Act, but they are now exposed to new challenges caused by drastic changes in global markets.

Economic security and digital sovereignty have gained relevance in the Commission's overall policy goals, pointing to the increased importance of resilient semiconductor ecosystems. Moreover, **the necessity of ex-ante risk preparedness as opposed to ex-post crisis response has increased in light of unforeseen supply chain disruptions** (see Nexperia case in Section 4.1.1.3). Pillar III mechanisms improved information exchange and crisis coordination (Workshops 6, 14, 15); however, given the short implementation period, impacts on actual resilience or crisis mitigation capacity cannot yet be evidenced. The Commission was largely successful in addressing the needs for improved visibility of supply-chain risks of public authorities and large industrial actors (Workshops 6, 14, 15; Interviews 1, 4). Nevertheless, crisis preparedness can only be achieved through **cross-pillar interventions and multi-stakeholder actions** between the Member States, the Commission and the private sector. In light of intensified geopolitical tensions and supply-chain weaponisation, the Chips Act may contribute to mitigating certain risks, but cannot fully address all emerging vulnerabilities.

Scope is key in assessing the relevance of Pillar III, both within the semiconductor value chain and the European Union. Crisis response mechanisms protect all Member States, not just those with production capacity. Many EU industries rely on the same semiconductors and product flows within the Single Market. This makes the Pillar III mechanisms being embedded in the ESB, with full Member States representation, relevant. As OPC results demonstrate, most stakeholders are either uninvolved with and do not know the extent to which Pillar III delivers on its objectives (40%) or believe it did not meet its objectives (30%) ⁽¹¹¹⁾.

⁽¹¹¹⁾ Open public consultation survey (N=96), data reflecting the percentage of respondents selecting "Don't know / Not involved" or "Does not meet the objectives" (67 out of 96) for the question: Q18.

Consultations suggest that, to capture system-wide risks, the scope of crisis response mechanisms needs to be extended to cover base materials, substrates, materials, packaging, assembly, downstream electronics, and end-user industries. Not including these elements allows vulnerabilities in the value chain to go unnoticed, limiting the relevance of crisis response for downstream and end-user sectors, and eventually customers (Workshops 7,9,11; Interviews 8, 10). The PCB assembly and EMS industries seek inclusion and argue that a wider approach to risk mitigation can help identify risk patterns more effectively (Workshops 6, 7, 9, 11, 14, 15; Interview 1, 4, 8, 10).

To what extent does Pillar 3 (Monitoring and crisis response) of the Chips Act deliver on its objectives?

5. WHAT ARE THE CONCLUSIONS AND LESSONS LEARNED?

5.1. Conclusions

This evaluation concludes that **the Chips Act has been key in establishing a European semiconductor regulatory and policy framework** that did not previously exist and did so in a short period of time. It mobilised substantial public and private investment, introduced state-of-the-art EU-level infrastructures, and put in place governance mechanisms for coordination and crisis preparedness. Stakeholder confidence in the overall strategic direction remains high, and the Act is widely perceived as a necessary response to geopolitical, technological, and economic pressures.

At the same time, **the transition from output delivery to system-wide results and impacts is still ongoing**. The main constraints are structural and economic rather than operational and relate to the Union's ability to industrialise innovation, finance scale-ups, reinforce supply chain resilience, and generate system-level intelligence.

The Act has been **instrumental in building technology infrastructures and early-stage manufacturing capacity**. The creation of EU-level pilot lines, competence centres and shared infrastructures has ensured coordinated effort. Such initiatives are already improving access to advanced tools and support a strong cross-border collaboration. The impact of other components (namely, quantum chip pilots and the design platform) will only become apparent at a later stage. In any case, stakeholders widely recognise the Act's contribution to strengthening Europe's R&I base and improving coordination across Member States.

By contrast, **progress in manufacturing deployment and subsequent increased strategic autonomy is still at an early stage**, partly due to long lead times between investment decisions and actual production in fabs. Europe remains structurally dependent on non-EU suppliers in critical segments, particularly at advanced technology nodes, and the loss or delay of major investment projects demonstrates that sovereignty has not yet materially improved.

Across the evaluation criteria, **the lab-to-fab gap emerges as an important challenge**. The Act has already managed to move technologies to higher readiness levels and – considering the short time since its entry into force – stable pathways to volume manufacturing are expected to materialise in the coming years. Many outputs operate effectively at a technical level and will generate the industrial capacities required to secure European supply later in time. The challenge confronting the EU is no longer primarily innovation generation, but **industrialisation and scale**.

The evaluation also finds that **limited private capital continues to limit the scaling of European semiconductor firms**. While the Act mobilised unprecedented levels of public funding, private investment (particularly, late-stage and institutional) remains insufficient compared to competing regions. Support for scale-ups is constrained by structural features of the European financial system, including the lack of a real Capital Market Union, existing rules for pension funds, and conservative investment practices. This weakens European value capture and incentivises scale-ups to relocate or get acquired by non-EU firms. The Act has improved early-stage innovation capacity, but the allocated budget to the (EIC Accelerator part of the) Chips Fund, consumed in its first two years, has proven insufficient. Thematic instruments with patient capital are necessary to help semiconductor startups in scaling up and broader measures must be conceived to create the conditions required for industrial 'champions' to emerge.

In addition, the evaluation finds that **current EU-level instruments to address security of supply and economic security vulnerabilities are useful tools, but should be further strengthened**. On the one hand, manufacturing deployment is shaped primarily by industry investment decisions supported through national funding frameworks. Demand-side weaknesses further undermine resilience. On the other hand, fragmented markets, low volumes in key sectors, and limited procurement coordination reduce the commercial viability of European production. Without demand aggregation and reliable market signals, new capacity risks underutilisation.

Finally, the evaluation concludes that **the EU has limited insight into EU and global semiconductor supply chains to support strong crisis preparedness**. Although the ESB substantially improved coordination and early-warning mechanisms were initiated, monitoring should consider a more integrated approach across materials, equipment, design tools, and downstream users. Data collection remains fragmented and sensitive, limiting the ability to anticipate disruptions. Pillar III therefore provides only partial system-level visibility.

Overall, the Chips Act has delivered quickly and credibly on its initial ambition to build European capacity. However, effectiveness in terms of autonomy and resilience depends on whether Europe can now convert infrastructures into industrial output, innovation into scale, and coordination into actionable intelligence.

5.2. Lessons learned

Several lessons emerge from the evaluation regarding the design and implementation of the Chips Act. First, **turning innovation into industrial capacity** requires policy mechanisms that explicitly bridge pilot line infrastructures and manufacturing investments. While the Chips Act successfully created world-class research and validation facilities, experience shows that market-scale production does not emerge automatically from technological capability alone. Future initiatives would benefit from embedding transition mechanisms that facilitate movement from pilot lines into industrial deployment more systematically.

Second, **demand orientation** should be built into industrial policy instruments. The evaluation highlights that supply-side investment alone does not necessarily generate scale or competitiveness in the absence of reliable market uptake. Instruments that support deployment should therefore be accompanied by measures that increase demand, such as procurement coordination or consumption incentives.

Third, **access to finance** must remain central to industrial policy. The evaluation shows that the FOAK framework improved legal certainty for major investments, but certain stakeholders claim that they still face long notifications and State aid procedures, and project-level uncertainty. Late-stage venture capital and institutional investment constraints similarly limit scale-up funding. These factors weaken Europe's competitiveness and slow the growth of globally competitive firms.

Finally, **crisis preparedness depends on high-quality system intelligence**. The evaluation shows that effective monitoring requires up-to-date visibility across the entire value chain, covering not only fabrication, but also materials, packaging, design tools and downstream users. Future frameworks could prioritise improved data collection, shared data infrastructures, and integrated reporting in order to enable timely risk detection and coordinated responses.

ANNEX I – EVALUATION MATRIX

Effectiveness

EVALUATION QUESTION	SUB-QUESTION	JUDGEMENT CRITERIA	INDICATORS	DATA SOURCES
How successful has the EU's intervention been in achieving (or progressing towards) the objectives of the Chips Act? To what extent did the expected changes result from EU action delivered?	What are the outcomes and results of the Chips act on the areas indicated in the objectives? To what extent are these results and impacts resulting from the Chips Act?	Extent to which the intervention's outcomes align with the specific objectives outlined in the Chips Act's intervention logic (e.g., strengthening research leadership, addressing skills shortages, increasing production capacity) The positive or negative effects of the intervention can be linked directly to the interventions of the Chips Act.	Progress against indicators set out in Annex II of the Chips Act Regulation Rate of commitment of Pillar I budget via the Chips JU (JU) Work Programme Number of 'First-of-a-Kind' (FoaK) facilities established and operational Amount of public and private investment mobilised under the Chips Act Number of SMEs and start-ups supported through the Chips Fund Share of stakeholders who report progress towards the objectives (in %) (by MS, type of stakeholder) Contextual information on potential other trends and developments that could explain the observed results	Desk research and document review Targeted online survey, expert interviews, workshops and the OPC Case studies Analysis of results Impact evaluation

EVALUATION QUESTION	SUB-QUESTION	JUDGEMENT CRITERIA	INDICATORS	DATA SOURCES
What has been the quantitative effect of the Chips Act in terms of investment in the European semiconductor industry?	How did the investments levels look like before and after the interventions of the Chips Act? To what extent are the changes in investment levels resulting from the Chips Act?	The volume and type of new of public and private investment mobilised directly attributable to the framework and incentives established by the Chips Act. The positive or negative investments changes can be linked directly to the interventions of the Chips Act.	Total value (€ billion) of public and private investment announced and committed since the introduction of the Chips Act Disaggregation of investment by pillars of the Chips Act, type of facility, value-chain segment, technology nodes and MS Value (€ billion) of State aid approved for FoaK and IPCEI projects R&D expenditures in the EU chips sector since the introduction of the Chips Act, and comparison with non-EU countries Semiconductor patents in the EU since the introduction of the Chips act, compared with non-EU countries FDI inflows into the EU semiconductor sector, attributed to the Chips Act, if possible Comparison of investment trends against the pre-Chips Act baseline Levels of new public and private investments reported by (industry) stakeholders (in EUR) (by Member State, type of investments, policy and pillar focus) Contextual information on potential other trends and developments that could explain investment developments Share of national authorities agreeing that investments occurred due to the Chips Act (in %) (by Member State and policy area) Assessment of the causal link between the EU intervention and the observed changes in investments controlling for potential other factors	Desk research and review of statistics Assessment of costs and benefits, modelling of investment flows attributable to the Act Targeted online survey, expert interviews, workshops and the OPC
Has the Chips Act reduced supply chain dependencies for European industry in practice?	In which areas have supply chain dependencies been reduced and in which areas not? How have the different pillars contributing to reducing supply chain dependencies?	Evidence demonstrates a measurable decrease in reliance on single non-EU sources for critical semiconductor components, materials, or equipment, and an increase in the resilience of EU-based supply chains.	Change in EU's global market share in specific value chain segments (e.g. advanced packaging, SiC/GaN wafers) Analysis of trade data imports/exports of key semiconductor products, linking to relevant pillar efforts Number of new EU-based suppliers for critical materials and equipment, across pillars I and II Perceptions of downstream industrial users (automotive, healthcare, telecoms) on security of supply and how different pillars have impacted this perception Analysis of supply chain mapping exercises conducted under Pillar III	Desk research and review of statistics Targeted online survey, expert interviews, workshops and the OPC Desk research on international/ academic evidence Impact evaluation Analysis of results

EVALUATION QUESTION	SUB-QUESTION	JUDGEMENT CRITERIA	INDICATORS	DATA SOURCES
To what extent are the activities and implementation methods suited to protect the EU's security interests and help reinforce the EU's strategic autonomy?	How fitting are the activities and methods of the Chips Act to achieving strategic autonomy and security interests? To what extent has the Chips Act fostered 'managed interdependence' by strengthening partnerships and diversifying supply chain collaborations with non-EU partners?	The governance mechanisms (Pillar III) and investment frameworks (Pillar II) are effectively designed and implemented to anticipate, monitor, and mitigate supply chain disruptions and support production in strategic technology areas. The EU has successfully leveraged the Chips Act to build more resilient supply chains through strategic international cooperation, reducing critical dependencies on single sources while reinforcing its position within a network of reliable global partners.	Contextual information about semiconductor policies and initiatives to increase strategic autonomy and security on other countries, and their evaluation results Number of early warnings issued by the ESB Timeliness of crisis response mechanism activation (simulations or real events) Assessment of the effectiveness of ESB monitoring, warning and crises response Assessment of the functionality and readiness of the Pillar III crisis response toolbox (e.g., priority-rated orders, common purchasing) Analysis of the criteria for Foak status to assess alignment with strategic technologies Share of stakeholders who state that the ESB is effective (in %) (by Member State, type of stakeholder) Comparative evaluation of the suitability of each pillar's activities and methods in reinforcing strategic autonomy, considering their distinct roles (e.g. R&D, industrial scaling, crisis management) and evidence from other countries Number and value of joint R&D projects or investments with key international partners Analysis of trade data showing diversification of imports for critical semiconductor materials and equipment away from single-country dominance Assessment of the effectiveness of cooperation mechanisms established under international agreements (e.g., EU-US TTC, EU-Japan Digital Partnership) Stakeholder perceptions from EU industry and international partners on the quality and strategic value of the collaboration Evidence of the EU leveraging partnerships to gain access to technologies or markets where it has identified gaps	Desk research and review of statistics Targeted online survey, expert interviews, workshops and the OPC Desk research on international/ academic evidence Impact evaluation Analysis of results
In case targets or objectives have not been met or the expected progress has been delayed, what were the causes? Will it be possible to achieve the objectives on time? Were there any mitigating measures taken? What could be alternative targets that may be considered?	Will it be possible to achieve the objectives on time? Were there any mitigating measures taken? What could be alternative targets that may be considered?	Identification of a clear causal link between specific hindering factors (internal or external) and any identified implementation gaps or delays and mitigation measures.	Assessment of progress on each Pillar and activities Variance analysis of actual vs. planned progress against key milestones (e.g. pilot line operational dates) for each pillar Assessment of the causes behind delays and challenges to achieve objectives Analysis of unsuccessful projects and causes of failure Analysis of mitigating actions taken by the Commission/Chips JU Expert and stakeholder opinions on the realism of current targets and potential alternatives, considering the performance and challenges of each pillar Identification of alternative scenarios and targets	Targeted online survey, expert interviews, and workshops State-of-play analysis of global context

EVALUATION QUESTION	SUB-QUESTION	JUDGEMENT CRITERIA	INDICATORS	DATA SOURCES
What external factors have hindered progress towards achieving the objectives of the Chips Act?	What were the challenges or problems the Chips Act faced with its implementation and achieving results? Which of these challenges and problems were due to external factors?	Identification and the impact assessment of specific geopolitical, economic, and technological factors outside the direct control of the EU intervention.	Analysis of competing global subsidy programmes (e.g., US CHIPS Act, China's Big Fund) and their impact on investment decisions Assessment of the impact of global economic conditions (e.g., inflation, energy costs) Analysis of geopolitical events (e.g., trade tensions, export controls) affecting supply chains and their differential impact on each pillar's objectives Identification of unforeseen technological shifts Forecast modelling of EU market share trajectory vs. the 20% Digital Decade target, considering the current pace of each pillar's implementation Identification of causal factors (e.g., administrative delays, funding gaps, market dynamics, geopolitical events) through root cause analysis and process tracing, specifically analysing their impact on each pillar's progress	Targeted online survey, expert interviews, workshops, and the OPC State-of-play analysis of global context Impact evaluation Case studies Policy recommendations analysis
What are the spill-over effects of the Chips Act, if any? How does the Chips Act contribute to horizontal priorities, in particular to Europe's competitiveness and security?	How does the Chips Act contribute to horizontal priorities (e.g., twin transitions and preparedness)? How does the Chips Act contribute to Europe's competitiveness and security?	Evidence of positive or negative unintended effects in adjacent policy areas. Clear contribution to broader EU goals such as the Green Deal, digital sovereignty, and economic security.	Analysis of how Chips Act investments support digitalisation, research and innovation Analysis of how Chips Act investments support the development of energy-efficient semiconductors (Green Deal alignment) Spill-over effects noted by stakeholders (most popular categories of spill-over effects in online survey) Assessment of the Act's role in strengthening the EU's horizontal priorities in green and digital transition Number of patents filed generated from Chips Act-funded research Job creation figures in related sectors (e.g. equipment manufacturing, software development) Case study evidence of technology transfer to other sectors Spill-over effects noted by stakeholders (most popular categories of spill-over effects in online survey) Assessment of the Act's role in strengthening the EU's position in global technology standard-setting bodies	Desk research and review of statistics Targeted online survey, expert interviews, workshops and the OPC Analysis of results Case studies

EVALUATION QUESTION	SUB-QUESTION	JUDGEMENT CRITERIA	INDICATORS	DATA SOURCES
Have any concrete benefits for Europe's semiconductor industry and its users materialised?	What are the observed changes in the beneficiary stakeholders' businesses? Are the changes in line with expectations?	Evidence of tangible improvements in competitiveness, innovation, and market access for EU firms and users	Growth in revenue and market share of European semiconductor companies Increased market share of semiconductors produced in the EU in applicable segments Reduction in production downtime for user industries due to chip shortages and the role of Pillars III and II mechanisms specifically Testimonials from companies (beneficiaries and users) on specific benefits gained (e.g. access to pilot lines, improved supply stability, new business opportunities), linking benefits to specific pillars Case study evidence of successful product development or market entry facilitated by the Act, identifying the contributing pillar(s) Comparative analysis of the types and scale of benefits realised across the different pillars	Desk research and review of statistics Targeted online survey, expert interviews, workshops and the OPC Case studies Analysis of results and assessment of costs and benefits
To what extent were the technologies selected under the Chips Act relevant, and how well do they lend themselves to industrial technology transfer?	To what extent were the technologies selected relevant to meet changing needs? How well do the technologies lend themselves to industrial technology transfer?	The technology focus of Pillar I aligns with future market demand and strategic industrial needs, and clear pathways exist for their adoption by European industry.	Number of industrial partners and research institutions participating in pilot lines Number of licenses and patents resulting from the pilot lines. Expert assessment of the long-term strategic relevance of selected technologies and stages of the semiconductor value chain Analysis of pilot line governance and access models to assess their industry-friendliness Stakeholder feedback on the effectiveness of bridging the "lab-to-fab" gap Assessment of the role of Competence Centres in driving technology transfer Evaluation of the alignment between Pillar I's technological focus and Pillar II's manufacturing investments	Desk research and review of statistics Targeted online survey, expert interviews, workshops and the OPC Analysis of results Case studies
How effective have the communication of the Chips Act and Chips Act related activities been?	Did the communication on the Chips Act reach the relevant stakeholders, and across the value chain? What activities were more and less successfully communicated?	Key stakeholder groups are well-informed about the opportunities offered by the Chips Act, and the EU's strategic intent is clearly communicated both internally and globally.	Media monitoring metrics (volume of coverage, engagement metrics, sentiment analysis), for each pillar's specific initiatives where relevant Website and social media analytics for Chips Act-related portals Participation rates at info days and brokerage events Stakeholder awareness levels assessed through surveys, differentiating awareness of each pillar's opportunities Analysis of the clarity and accessibility of communication materials (e.g., call documents, guidance), per each pillar Coverage of Chips Act, assessing the framing and visibility for pillars, if possible	Desk research and document review Targeted online survey, expert interviews, workshops and the OPC Media analysis

EVALUATION QUESTION	SUB-QUESTION	JUDGEMENT CRITERIA	INDICATORS	DATA SOURCES
What is the direct and indirect impact of the Chips Act on the labour market?	What has been the effect on job creation and wages? What has been the effect on skills development and talent attraction?	The intervention has a demonstrable effect on job creation, skills development, and talent attraction within the EU semiconductor ecosystem.	Number of individuals trained through Chips Act-supported initiatives (e.g. Competence Centres, Chips Academies) Number of direct jobs created in new/expanded facilities Wages, employment and skills shortages and vacancies data in the sector (trend data) Data on talent mobility (attraction of researchers/engineers to the EU) Share of stakeholders who report availability of qualified skilled labour (in %) (by MS, type of stakeholder)	Desk research and review of statistics Targeted online survey, expert interviews, workshops and the OPC Analysis of results and assessment of costs and benefits Impact assessment
Are the indicators and targets set adequate to measure the success of the Chips Act?	Are the indicators selected suitable for measuring success with semiconductor policy? Are the indicators useful and feasible to monitor and track?	The existing indicators and the overarching Digital Decade target are specific, measurable, achievable, relevant, and time-bound (SMART) for assessing the Act's performance.	Expert review of the relevance and robustness of indicators, including those specific to each pillar Analysis of the methodology and baseline for the 20% Digital Decade target, assessing its suitability as an overarching goal Stakeholder perceptions on the usefulness and adequacy of current monitoring data and framework Comparison with monitoring frameworks of similar initiatives internationally Identification of potential gaps in the current monitoring framework	Targeted online survey, expert interviews, workshops and the OPC Desk research and document review Analysis of results and policy recommendations
How accessible were the activities stemming from the Chips Act and related policies to start-ups and SMEs?	Were SMEs able to apply for and get funding? Were SMEs able to join pilot lines?	Application processes and support structures are designed and implemented in a way that facilitates, rather than hinders, the participation of smaller actors.	Funding from the Chips Act, in particular the Chips Fund, awarded to SMEs and start-ups Number of SMEs and start-ups accessing pilot lines and the design platform Success rates of SME applicants in Chips JU calls compared to large enterprises SME and start-up feedback on the complexity of application procedures and the usefulness of support services (e.g. from Competence Centres) Stakeholder perceptions on the accessibility of activities across the different pillars Case studies of SME or start-up participation Analysis of the design of the Chips Fund to assess its suitability for early-stage companies	Desk research and review of statistics Targeted online survey, expert interviews, workshops and the OPC Case studies Analysis of results

Relevance

EVALUATION QUESTION	SUB-QUESTION	JUDGEMENT CRITERIA	INDICATOR	DATA SOURCES
How well do the original objectives of the Chips Act correspond to current and emerging needs?	What are the current or emerging needs in the European semiconductor ecosystem? What are the original and current objectives of the Chips Act?	The extent to which problems identified in the 2022 Staff Working Document remain pertinent, and the Act's objectives are aligned with new challenges and opportunities that have emerged since its adoption.	Contextual information on recent technological trends (e.g., demand for AI chips) and geopolitical shifts Share of stakeholders who agree that the current strategic focus of the Act is relevant (in %) (by Member State, type of stakeholder) Overlap or mismatch of the original problem definition with the current state-of-play of the semiconductor industry Overlap or mismatch of the objectives of the Act with the strategies of other major semiconductor players (e.g., US, China)	Desk research on market developments and documentary review Targeted online survey, expert interviews, workshops and the OPC Analysis of results
To what extent does the Chips Act address the needs of its main stakeholders?	What are the current or emerging needs and challenges in the European semiconductor ecosystem? How has the Chips Act balanced support between cutting-edge (<5nm) and mature/mainstream semiconductor technologies? Does this balance align with the current and emerging needs of stakeholders?	Key technological, market, and geopolitical developments are identified to determine the current and emerging needs justifying EU intervention. This includes any evolving problems (e.g. new supply bottlenecks, surging demand for AI chips, skills gaps) that have arisen or intensified post-2022. Degree to which the different pillars and instruments of the Chips Act are tailored to the specific needs of key stakeholder groups. The Act's portfolio of support is strategically balanced, addressing both the long-term objective of technological leadership in advanced nodes and the immediate resilience needs of key downstream sectors for mature chips.	Contextual information on needs and challenges: recent industry trends, shock events and data market changes, combined with stakeholder testimonies on needs Share of stakeholders who agree that the Chips Act and the different pillars address their needs/challenges (in %) (by Member State, type of stakeholder) Share of uptake of the different instruments by stakeholder groups (in %) (by Member State, type of stakeholder) Distribution of funding (€ and %) from Pillars I and II allocated to projects targeting cutting-edge vs. mature nodes Number of FoaK facilities approved for advanced vs. mainstream technologies Analysis of demand forecasts from key user industries (e.g., automotive, healthcare) versus the technology focus of supported projects Stakeholder perceptions (industry associations) on the alignment of the Act's focus with their sector's needs Analysis of the criteria for pilot lines and FoaK facilities to assess the weighting given to different technology nodes. Case study evidence on how supported projects address specific supply chain gaps identified by downstream users Difference between reported needs and specific support offered by the Act	Desk research on market developments and documentary review Targeted online survey, expert interviews, workshops and the OPC Analysis of results
To what extent is the Chips Act sufficiently flexible to adapt to emerging needs and changing circumstances?	To what extent has the implementation of the Chips Act responded to relevant political and economic developments?	The Act's implementation mechanisms (e.g., Chips JU work programmes, ESB deliberations) have demonstrated an ability to adjust priorities and actions in response to unforeseen events or	Evidence of the Act's implementation being referenced or adjusted in response to major political statements or economic shock Case studies that demonstrate adaptation (or lack thereof) Share of stakeholders who agree that the strategy is able to adapt and provide testimonies on successful	Desk research and document review Case studies Targeted online survey, expert interviews, workshops and the OPC

EVALUATION QUESTION	SUB-QUESTION	JUDGEMENT CRITERIA	INDICATOR	DATA SOURCES
		new opportunities.	adaptation (in %) (by Member State, type of stakeholder)	
Which parts of the semiconductor value-chain benefit the most from the Chips Act? Which parts of the value-chain are benefiting the least?	Which stakeholders benefit and not from the Act and its pillars? What type of benefits are there and how are they distributed among stakeholders (financial, learning, collaboration, etc)?	The support provided by the Chips Act is distributed across the value chain in a manner that is strategically justified, addressing the most critical gaps without neglecting other important segments.	Breakdown of funding and investment by value chain segment Share of stakeholders that prefer specific parts of the Act (in %) (by Member State, type of stakeholder, part/pillar of the Act) Share of stakeholders that claim that they benefit from specific parts of the Act (in %) (by Member State, type of stakeholder, part/pillar of the Act) Analysis of whether the distribution of benefits and support of the Act aligns with the strategic gaps identified in the problem definition	Targeted survey and mapping and analysis of the state of the value chain Expert interviews, workshops and the OPC Analysis of results
To what extent do the needs/problems addressed by the Chips Act continue to require action at EU level as opposed to intervention at national/regional level?	What are the needs and problems the Chips Act aims to address? What are the needs and problems that national/regional level governance tries to address?	The scale of investment required, the cross-border nature of value chains, and the need for a unified stance in global competition confirm that the rationale for EU-level action remains strong (subsidiarity principle).	Contextual information on the scale of challenges and economies of scale (e.g. global subsidy race) versus the capacity of individual MS to respond Overlap or mismatch between the Act budgets and scope with national semiconductor strategies or other international initiatives Share of stakeholders that claim that an EU-level framework is needed versus purely national initiatives (in %) (by Member State, type of stakeholder)	Desk research and documentary review of semiconductor policies in Europe Analysis of policy options considering international dimensions Targeted online survey, expert interviews, workshops and the OPC

Efficiency

EVALUATION QUESTION	SUB-QUESTION	JUDGEMENT CRITERIA	INDICATOR	DATA SOURCES
How operationally efficient is the Chips for Europe Initiative?	How efficient was the implementation of the Chips for Europe Initiative? How efficient is the application process for initiatives sourcing funds from different streams?	The resources (financial, human, administrative) utilised by the Chips for Europe Initiative are proportionate to the outputs and results achieved. Application and funding processes are streamlined and minimise administrative burden.	Administrative costs as a percentage of the total budget Average time-to-grant and time-to-pay for Chips JU projects Cost-benefit analysis of key actions (e.g., pilot lines) Beneficiary and applicant feedback on the complexity and burden of application procedures and multi-stream funding applications Analysis of processes for projects combining funds (e.g., from HE and Digital Europe) to identify bottlenecks	Cost-benefit analysis Desk research: Chips JU financial reports and internal control documents, European Court of Auditors' reports Stakeholder consultations: survey of applicants and beneficiaries, interviews with Chips JU staff and with beneficiaries who applied for (multi-stream) funding
Is the governance structure of the Chips JU sufficiently agile to implement the objectives of the Chips Act and adapt to technology and market developments?	Do the decision-making processes, roles, and interactions within the Chips JU's governing bodies enable it to respond swiftly to new market and technology developments?	The implementing bodies possess the necessary human resources, technical expertise, and administrative capacity to effectively manage their respective tasks under the Chips Act.	Assessment of decision-making processes of the Chips JU's governing bodies Assessment of the roles and interaction between the Public Authorities Board, the Industrial and Research Board, and the Executive Director Analysis of the time taken to launch new calls or adapt work programmes in response to identified needs, market or technology shifts Stakeholder perceptions of the JU's agility and responsiveness Comparison with governance models of similar international initiatives	Desk research: Chips JU founding regulation and rules of procedure; minutes of Governing Board and Public Authorities Board meetings Targeted interviews: with Chips JU management, board members, and parent DGs (CNECT, RTD), interviews with industry representatives Formulation and analysis of policy recommendations
How well-equipped are the relevant implementing bodies such as the Chips JU, the European Commission, the EIB, the EIF, and the EIC to implement the Chips Act?	Do the Chips JU, Commission, EIB, EIF, and EIC possess the necessary resources to effectively coordinate?	The implementing bodies possess the necessary human resources, technical expertise, and administrative capacity to effectively manage their respective tasks under the Chips Act.	Staffing levels and expertise profiles within each body relative to their mandated tasks Analysis of budget execution rates for administrative expenditure Self-assessment by the bodies of their capacity and identification of any resource gaps Analysis of coordination mechanisms between the different implementing bodies Stakeholder feedback on the professionalism and expertise of the bodies	Desk research: annual reports and management plans of the Chips JU, EIB, EIF, EIC, other reports as applicable Targeted interviews and surveys: with management and operational staff from all named implementing bodies
How efficient is the State aid approval process for First of a Kind (Foak) facilities and IPCEI projects?	Are the duration, complexity, and administrative burden of the State aid notification and approval process for Foak and IPCEI	The duration and complexity of the State aid notification and approval process are proportionate and do not create undue delays that jeopardise	Average time from pre-notification to final Commission decision for Foak and IPCEI projects in the semiconductor sector Comparison with State aid approval times in other sectors Feedback from MS and companies on the clarity of	Desk research: analysis of public State aid decisions and timelines Targeted interviews: with officials from DG COMP, DG CNECT, relevant Member State ministries, and companies that have undergone the

EVALUATION QUESTION	SUB-QUESTION	JUDGEMENT CRITERIA	INDICATOR	DATA SOURCES
	projects appropriate and timely?	strategic investments	guidance and the administrative burden of the process Analysis of the interaction between the Commission (DG COMP, DG CNECT) and notifying parties Comparison with processes in other sectors	process
How complementary has the IPCEI on Microelectronics and Communication Technologies (9) been to the Chips for Europe Initiative to achieve the objectives of the Chips Act?	Do the two instruments operate in a complementary manner, avoiding overlaps and featuring sufficient coordination to form a coherent support landscape?	Extent to which the IPCEI and the Chips for Europe Initiative operate in a synergistic manner, targeting different but complementary aspects of the R&D&I chain, avoiding overlaps and reinforcing mutual objectives	Mapping of projects funded under both instruments to identify areas of focus and potential overlap or synergy Analysis of coordination mechanisms between the Commission services managing the IPCEI and the Chips JU Stakeholder views on how the two instruments interact and whether they form a coherent support landscape	Desk research: IPCEI project documentation; Chips JU work programmes and funded project lists Targeted interviews: with Commission officials (DG COMP, DG CNECT), Chips JU staff, and beneficiaries of both instruments State-of-play analysis: to map the broader policy landscape.
What is the extent of the administrative and financial burden on beneficiaries of the Chips Act?	What are the quantifiable administrative and financial costs for beneficiaries, and are the reporting and auditing requirements perceived as clear and streamlined?	The reporting, auditing, and administrative requirements for beneficiaries are streamlined, clear, and proportionate to the funding received	Estimation of person-hours and financial costs incurred by beneficiaries for administrative compliance (reporting, audits) e.g. using the Standard Cost Model Number of reporting requirements and frequency. Beneficiary survey responses on the perceived level of administrative burden Stakeholder perceptions on specific burdens and pain points of beneficiaries Identification of specific sources of burden (e.g., complex financial reporting, duplicative information requests) and their relative weight	Desk research: analysis of reporting and auditing requirements and comparison with the administrative burden of other EU programmes Cost-benefit analysis: specific component on administrative burden Stakeholder consultations: survey of beneficiaries with dedicated questions on administrative burden; workshop and interviews to discuss specific pain points
Have any inefficiencies in the implementation of the Chips Act been identified? Could the implementation of any of its components be done in a more efficient way? What potential simplification and cost-reduction measures should be considered?	What specific bottlenecks, redundancies, or overly complex procedures exist, and what concrete, feasible simplification measures can be proposed to address them? Where can the implementation of the Chips Act be simplified and made more efficient?	The evaluation identifies specific bottlenecks, redundancies, or overly complex procedures in the Act's implementation and proposes concrete, feasible measures for simplification.	Mapping and analysis of implementation processes and a catalogue of potential simplification measures (e.g. streamlining application forms, harmonising reporting across programmes, greater use of lump sums). Stakeholder validation of proposed measures Cost-benefit assessment of proposed simplification measures	Synthesis of findings from all other evaluation questions Stakeholder consultations: dedicated questions in surveys and interviews on simplification ideas, workshop discussion Cost-benefit analysis: analysis of unjustified cost elements Policy recommendations analysis: formulation and analysis of simplification options
How efficient is the overall governance of the Chips Act?	Are the roles and responsibilities between the Commission, ESB, and Chips JU clearly defined and are the information flows and decision-making processes between them efficient?	The governance structure, including the roles of the Commission, the ESB, and the Chips JU, ensures coherent, timely, and cost-effective implementation of the Act as a whole.	Analysis of the clarity of roles and responsibilities between the different governance bodies Assessment of the efficiency of information flows and decision-making processes between the ESB, Commission, and Chips JU Identification of any governance gaps or overlaps Stakeholder perceptions of the overall governance efficiency	Desk research: analysis of the Chips Act Regulation and internal working arrangements between the bodies Targeted interviews: with members of all key governance bodies (Commission, ESB, Chips JU)

EVALUATION QUESTION	SUB-QUESTION	JUDGEMENT CRITERIA	INDICATOR	DATA SOURCES
Have the skills and talent initiatives under the Chips Act been efficient in addressing sector needs?	Do the resources invested in talent development, attraction, and retention yield a measurable increase in qualified professionals who meet the industry's skills needs?	The resources invested in skills initiatives have yielded a measurable increase in the availability of qualified talent, addressing critical skills gaps identified by the industry.	Ratio of programme graduates who secure employment in the EU semiconductor sector within a set timeframe Metrics on the international recruitment of top-tier talent into EU-based companies and research institutions Analysis of the administrative efficiency of establishing and running skills academies and competence centres Employer or association feedback on the quality and relevance of skills provided by the new training programmes Testimonials on the attractiveness of the EU as a destination for a career in semiconductors	Desk research: analysis of programme budgets and enrolment data from Chips Academies and competence centres; reports from the European Chips Skills Academy (ECSA) Stakeholder consultations: surveys and interviews with the semiconductor industry, heads of training institutions Cost-Benefit Analysis: to assess the cost-effectiveness of skills initiatives.

Coherence

EVALUATION QUESTION	SUB-QUESTION	JUDGEMENT CRITERIA	INDICATOR	DATA SOURCES
To what extent is the Chips Act coherent with other EU, national and regional interventions that have similar objectives? To what extent have synergies been achieved? What could be done to improve the coherence with other related EU, national or regional initiatives?	To what extent have synergies been achieved with other related initiatives? What could be done to improve coherence with other EU, national, or regional initiatives?	Extent to which the Chips Act complements and reinforces other relevant policies without creating contradictions or duplications. Existence of mechanisms in place to foster synergies.	Evidence of joint planning, coordination mechanisms, or mutual reinforcement between the Chips Act and other initiatives Identification of any instances of policy conflict, redundancy or of synergies and cooperation between the Chips Act and other EU policies, including the framework programmes, the Single Market, competition policy. Stakeholder perceptions on the coherence of the overall policy landscape.	Desk research: analysis of HE, RRF plans, and IPCEI documentation or other relevant documentation at national and regional level Interviews: with MS officials, regional authorities, and managers of national programme
To what extent the various components of the Chips Act generated synergies and/or compensated possible trade-offs among them?	How do the three pillars of the Chips Act interact to create a mutually supportive framework? How are potential trade-offs identified and managed?	Extent to which the three pillars of the Chips Act are implemented in a mutually supportive way in terms of internal coherence.	Analysis of the functional links between the three pillars Evidence of information sharing and joint decision-making between the bodies responsible for each pillar Identification of any trade-offs (e.g., focus on cutting-edge in Pillar I vs. need for mature nodes in user industries) and how they are managed	Desk research: analysis of the Chips Act Regulation, the overall intervention logic and implementation documents Targeted interviews, surveys and workshop: with officials from the Commission, Chips JU, and ESB, focusing on inter-pillar coordination
To what extent is the Chips Act coherent with actions funded under EU Programmes listed in Annex III of the Chips Act Regulation, the Recovery and the Resilience Facility, the Digital Decade Policy Programme objectives and targets (10) and other EU programmes with similar objectives? Have synergies materialised with EU Programmes listed in Annex III of the Chips Act Regulation? In which areas should synergies be fostered?	Have synergies materialised with the EU Programmes listed in Annex III of the Chips Act Regulation? In which areas should synergies be fostered?	The extent to which the Chips Act is implemented in alignment with the objectives and funding streams of related EU programmes, leveraging them for mutual benefit and avoiding fragmentation of effort.	Detailed mapping of the links and potential synergies between the Chips Act and other funding programmes (HE, Digital Europe, RRF, etc.) Analysis of the alignment of Chips Act objectives with the Digital Decade targets Review of Member State RRF plans and its use for coherence with Chips Act goals Evidence of concrete synergies that have materialised Stakeholder suggestions on areas for future synergies	Desk research: analysis of selected EU programmes Targeted interviews and workshops with officials from relevant Commission DGs (e.g., EMPL, REGIO, ECFIN)
To what extent is the Chips Act coherent with current wider EU policies and priorities?	How does the Chips Act contribute to the European Green Deal and the digital transition?	Extent to which the Chips Act supports and is supported by major EU strategic priorities, such as the European Green Deal, the digital transition, open strategic autonomy, and economic security.	Analysis of how Chips Act contributes to key EU policy objectives Assessment of the Act's role in the broader digital, green and competitiveness agenda Review of Commission policy documents and communications to assess the integration of the Chips	Desk research: Analysis of key Commission Communications and Strategies on the Green Deal, Digital Decade, and Economic Security etc. as well as other documents and communications, analysis of

EVALUATION QUESTION	SUB-QUESTION	JUDGEMENT CRITERIA	INDICATOR	DATA SOURCES
	How does the Act support the EU's goals for open strategic autonomy and economic security?		Act into the broader policy framework Review of selected commentaries and policy papers published on the Chips Act	European Council conclusions and European Parliament resolutions Policy recommendations analysis: this task will explicitly consider coherence with wider EU priorities
How coherent is the governance architecture of semiconductor policy in Europe? In particular, how do the different layers of governance and coordination interact with each other? How do they ensure a coherent approach towards industrial and institutional stakeholders?	How do the different layers of governance and coordination (e.g., Commission, ESB, Chips JU) interact with each other? How do they ensure a coherent approach towards industrial and institutional stakeholders?	Extent to which the different governance bodies interact effectively, with clear communication channels and a shared strategic direction, presenting a unified front to stakeholders.	Mapping of the governance architecture and the formal/informal links between its components Perceptions of representatives from various levels of governance Expert feedback on the clarity and coherence of their interactions with the governance system Identification of any coordination failures or jurisdictional ambiguities	Desk research: analysis of governance documents for all relevant bodies Targeted interviews, workshops: with experts and representatives from all layers of the governance architecture and with stakeholders who interact with them (e.g., industry associations).

EU added value

EVALUATION QUESTION	SUB-QUESTION	JUDGEMENT CRITERIA	INDICATOR	DATA SOURCES
Which benefits were achieved so far that go beyond what Member States could achieve while acting alone? Which concrete benefits does the Chips Act offer that go beyond other existing national or regional initiatives with similar objectives?	Which concrete benefits does the Chips act offer that go beyond the benefits of other existing national or regional initiatives with similar objectives?	Extent to which the Chips Act has generated outcomes of a scale, scope, or nature that would not have been feasible through uncoordinated national or regional actions.	Evidence of large-scale, cross-border collaboration (e.g., pan-EU pilot lines) that would be difficult to organise nationally Stakeholders agree that their MS could not implement changes without TSI support (in %) (by Member State) Identification of benefits related to critical mass, coordination, and a unified EU approach Analysis of the EU's increased leverage in international partnerships and trade negotiations due to a unified strategy Assessment of the creation of a more coherent and attractive single market for semiconductor investment, reducing fragmentation	Desk research: comparison of the achievements of the Chips Act with the scale and scope of purely national semiconductor initiatives Case studies: cases evidencing the EU added value of cross-border projects. Targeted interviews: with MS and industry on the benefits of EU-level coordination. Impact evaluation: to quantify the 'EU effect' against a baseline of uncoordinated national actions.
To what extent does the Chips Act promote cooperation among Member States to achieve its objectives?	How has the European Semiconductor Board (ESB) functioned as a forum for Member State cooperation? Has the Chips Act framework led to joint strategic planning or coordinated national investments?	Extent to which the Act has demonstrably incentivised and facilitated collaboration, information sharing, and joint investment among MS in the semiconductor field.	Number of MS participating in Chips JU projects Volume of cross-border investment within the EU semiconductor sector Analysis of the functioning of the ESB as a forum for MS cooperation and information exchange Evidence of joint strategic planning or coordinated national investments fostered by the Chips Act framework Stakeholder perceptions of the level and quality of inter-state cooperation	Desk research: analysis of the composition of project consortia in Chips JU calls; ESB meeting minutes and other relevant documents Targeted interviews and workshops: With Member State representatives on the ESB and participants in cross-border projects.

Recommendations and follow-up questions

EVALUATION QUESTION	SUB-QUESTION	JUDGEMENT CRITERIA	INDICATOR	DATA SOURCES
What are the key shortcomings or constraints of the Chips Act in fulfilling its stated aims?	What are the main weaknesses in the design of the Chips Act (e.g., funding levels, scope, governance structure, monitoring framework)? What are the most significant bottlenecks and challenges in the implementation of the Act (e.g., administrative burden, state aid)?	Identification of the main weaknesses and challenges in the design and implementation of the Chips Act.	Synthesis of the findings from the evaluation of the five main criteria (effectiveness, efficiency, relevance, coherence, EU added value) to identify key shortcomings Stakeholder identification of the main constraints they face. Stakeholder identification of the main constraints they face.	All data sources used for the evaluation Specific questions in stakeholder consultations on shortcomings and constraints
What key lessons and actionable recommendations can be drawn for the future of EU semiconductor policy?	Which mechanisms and instruments of the Chips Act have proven most successful and should be reinforced in future policies? What specific, evidence-based recommendations can be made to improve the design, governance, and implementation of EU semiconductor policy? How can future policy be designed to be more flexible and adaptive to the highly dynamic technological and geopolitical landscape?	Formulation of evidence-based and actionable recommendations for improving EU semiconductor policy	Synthesis of the findings from the evaluation of the five main criteria (effectiveness, efficiency, relevance, coherence, EU added value) to identify key shortcomings Stakeholder identification of the main constraints they face. Stakeholder identification of the main constraints they face.	All data sources used for the evaluation Specific questions in stakeholder consultations on shortcomings and constraints

ANNEX II – MAIN POINTS OF COMPARISON

The main points of comparison are:

- The situation before the intervention (2021);
- The situation during the evaluation of the Chips Act (using monitoring data, evaluation and impact assessment findings, 2025).

It must be noted that some initiatives mentioned below were expected to be rolled out later compared to others, which explains why some elements have progressed less two years after entry into force of the Chips Act.

Table 2. Main points of comparison

Point of comparison	Value before the Chips act	Value at the time of the evaluation
EU global market share ⁽¹¹²⁾	2021: 8.9%	2025: 10.5%
Investment mobilised (Foak State aid cases)	2021: n.a.	2025: EUR 32 billion
The number of beneficiaries involved in the actions supported by the Initiative	2021: n.a.	2025: 514
The number of unique legal entities involved in the actions supported by the Initiative	2021: n.a.	2025: 313
The number of design tools developed or integrated under the Initiative	2021: n.a.	2025: 0
The total amount co-invested by the private sector in design capacities and pilot lines under the Initiative	2021: n.a.	2025: 0
The number of users of semiconductors or user communities seeking, and the number of users of semiconductors or user communities obtaining, access to design capacities and pilot lines under the Initiative	2021: 0	2025: Up to 60 SMEs/start-ups using pilot lines
The number of businesses, which have used the services of national competence centres supported by the Initiative	2021: 0	2025: 20
The number of persons who have successfully concluded training programmes supported by the Initiative to acquire advanced skills and training on semiconductor technologies and quantum technologies	2021: 0	2025: 100 (via competence centres)
The number of active competence centres in the Union in the context of the Initiative	2021: 0	2025: 30
The number of start-ups, scale-ups and SMEs that have received venture capital from the Chips Fund activities and the total amount of capital investments made.	2021: 0	2025: 55 companies (EUR 354 million equity investment and EUR 62 million in grants)
The amount of investment by companies operating in the Union,	2021: 0	2025: tbd

⁽¹¹²⁾ Source: Contract CNECT/2022/MVP/0084, *Semiconductors market data by feature size, sector and region*, IDC, September 2025

Point of comparison	Value before the Chips act	Value at the time of the evaluation
including by segment of the value chain in which they operate.		
Number of working pilot lines	2021: 0	2025: 5
Number of training programmes launched	2021: 0	4 (through competence centres)
Number of SMEs/start-ups receiving funding	2021: 0	Chips Fund: 55 startups/SMEs
Number of FoaK State aid projects supported	2021: 0	2025: 11
Number of semiconductors IPCEI projects	2021: 0	2025: 68
ESB operational	2021: No	2025: Yes
Emergency toolbox operational	2021: No	2025: Partly
SCAN system operational	2021: No	2025: Yes

ANNEX III – OVERVIEW OF BENEFITS AND COSTS

Costs of the European Chips Act

The European Chips Act represents a significant financial commitment by the EU institutions and EU Member States to strengthen the semiconductor ecosystem. It generates direct financial and administrative costs as well as indirect costs across its three pillars.

Direct Financial Costs

Direct financial costs cover public expenditure and capital investments required to implement the Act, borne mainly by EU and national administrations, with complementary private investment.

Pillar I

Pillar I entails large public financial commitment, channelled through grants, Joint Undertaking contributions, and equity-type instruments. Citizens and consumers do not face direct financial costs, as funding comes from EU and national budgets. At EU level, as of November 2025, total public expenditure under Pillar I is around EUR 1,960.5 million: EUR 1,831.2 million for pilot lines, EUR 92.3 million for competence centres, EUR 25 million for the Design Platform, and EUR 12 million for design-related activities. The amount for pilot lines includes capital investment and operational expenditure, combining Horizon Europe and Digital Europe resources. The EU has foreseen about EUR 120 million over four years to competence centres, which – with EUR 92.3 million – is expected to be slightly lower in commitments due to Iceland not opting for a competence centre and several countries not going for the maximum amount of EUR 4 million over 4 years. To establish and operate the Quantum Chip pilots and the Design Platform, amounts of around EUR 200 million and EUR 400 million respectively are foreseen. Six Framework Partnership Agreements have been signed for quantum chip pilots. These come without financial commitment. First commitments for quantum chip pilots are expected for beginning of 2026. EUR 37 million has been committed on the Design Platform and design-related activities. The Chips Fund adds EUR 425 million: EUR 300 million via the EIC Accelerator, which has awarded EUR 62 million in grants and EUR 238 million in recommended equity investment to 24 startups through the dedicated Semiconductor and Quantum Technologies challenge and EUR 125 million via InvestEU, where EUR 68 million has been signed or approved with four financial partners, resulting in EUR 116 million in equity investment to 31 companies.

At national level, public expenditure stands at roughly EUR 1,957.3 million, including EUR 1,862.1 million for pilot lines and EUR 95.3 million for competence centres, with national support broadly matching EU contributions. No national financial costs were incurred for the Design Platform so far. Businesses do not yet face formal direct financial charges under the grant schemes so far. However, access to pilot lines, design platform, and quantum chip pilots, as well as support from competence centres come with a cost.

Pillar II

Pillar II focuses on security of supply and resilience through large-scale manufacturing facilities, potentially supported by State aid. Citizens and consumers do not bear direct financial costs, which fall instead on national administrations granting State aid and on private investors financing new fabrication plants. Eleven State aid decisions for FOAK facilities

represent a total public–private investment of EUR 32.2 billion. Total investments for some State aid supported projects are not disclosed. In parallel, the IPCEI on microelectronics and communication technologies covering research and innovation projects mobilises EUR 21.8 billion, of which EUR 13.7 billion is private investment and EUR 8.1 billion is State aid. For firms, the main direct financial costs are the capital expenditure for constructing and equipping fabs and the recurring operating costs (labour, utilities, maintenance), although detailed operating cost data are not yet available. No additional direct EU-level financial cost is recorded, as public investments are made by Member States, and the EU role is largely regulatory and supervisory.

Pillar III

Pillar III establishes monitoring and crisis response mechanisms, with modest direct financial implications. Citizens and consumers do not incur direct costs. For businesses, potential financial impacts arise only if crisis-stage measures are activated. Priority-rated orders could force manufacturers to prioritise certain customers, generating opportunity costs in the form of foregone revenues, disruptions, and strained commercial relationships. Export restrictions and information obligations would add compliance costs for semiconductor producers and downstream exporters. However, no crisis stage has been declared, and no such costs have materialised. For administrations, crisis coordination and enforcement costs remain minimal at this stage, although EU and national authorities would face higher resource demands if the crisis toolbox were used.

Direct Administrative Costs

Direct administrative costs comprise the human resources and operational effort required to manage, administer, and monitor the Act's instruments, for both participating firms and public authorities.

Pillar I

Administrative costs in Pillar I stem from managing multiple funding instruments and the associated application, due diligence, contracting, and monitoring processes. Citizens and consumers incur no administrative costs. For businesses, the administrative burden is perhaps most visible for SMEs and start-ups applying to the Chips Fund. A standard cost model suggests an average of 70 person-days (560 hours) per beneficiary for applications, due diligence, and reporting, at EUR 50-60 per hour, yielding about EUR 1.7 million in total for the 55 projects, or roughly EUR 30,000 per project. This number only considers selected proposals. Proposals that are not selected also make considerable investments to apply.

Across all Pillar I grants, an estimated 10-20 person-days per application (midpoint 15 days or 120 hours) at EUR 50 per hour for 514 participants in 44 projects results in around EUR 3 million in administrative and compliance costs, equivalent to about EUR 0.75 million per year over four years.

At EU level, managing the Chips Fund costs around EUR 5.6 million, assuming 160 person-days per funded project at EUR 80 per hour, or roughly EUR 100,000 per project. Administrative costs for other Pillar I instruments can be deducted from annual budgets of the Chips JU. Salary costs increased from EUR 3.9 million in 2023, before the Chips Act entered into force, to EUR 7.0 million in 2025. National administrations incur about EUR 0.7 million

(EUR 0.2 million per year) in administrative costs, based on roughly 25 person-days per project across relevant ministries and agencies.

Pillar II

Pillar II administrative costs relate to the State aid lifecycle. Citizens and consumers do not bear these costs. For businesses, subsidised firms are estimated to spend about 50 person-days per year (400 hours) on State aid applications, audit files, and reporting, at around EUR 80 per hour. This corresponds to approximately EUR 32,000 per beneficiary per year, or about EUR 1.0 million annually for a stylised set of 30 subsidised projects. At EU level, about 40 person-days per project per year (320 hours) at EUR 90 per hour imply around EUR 28,800 per project, or EUR 0.9 million per year across 30 projects. Nationally, preparing and notifying aid, liaising with the Commission, issuing decisions, and checking compliance is estimated at 60 person-days per project per year (480 hours) at EUR 80 per hour, i.e. EUR 38,400 per project per year or about EUR 1.2 million annually for 30 projects.

Pillar III

The administrative costs of Pillar III arise from the supply chain monitoring mechanism and crisis coordination structures. Citizens and consumers do not incur these costs. For businesses, regular monitoring surveys impose a recurring burden: if around 50 key semiconductor firms each spend roughly 160 hours (20 person-days) per year compiling and reporting data at EUR 70 per hour, the total annual compliance cost is about EUR 0.6 million, or EUR 11,000-12,000 per firm. Additional costs from consultations and crisis protocols would emerge only if these tools were used; to date, they remain minimally deployed.

At EU and national level, monitoring requires around eight full-time equivalents across DG CNECT and the ESB at roughly EUR 120,000 per FTE, plus around EUR 0.5 million in analytical support contracts, bringing annual EU monitoring costs to about EUR 1.5 million. For national administrations, assuming in each of the 27 Member States about 0.5 FTE ($\approx$ 800 hours a year) in relevant ministries and agencies is devoted to data provision at EUR 70/hour, the annual national administrative cost of feeding the EU monitoring mechanism is roughly EUR 1.5 million in total, or about EUR 55 000 per Member State.

For national administrations, crisis coordination and legal enforcement costs involving competition, customs, and trade authorities would increase if measures were activated, but they remain negligible in the absence of a declared crisis.

Indirect Costs

Indirect costs reflect potential distortions, opportunity costs, and unintended effects that are harder to quantify but relevant for overall efficiency.

Pillar I

Under Pillar I, citizens and consumers do not directly bear indirect costs. For businesses, there is a risk of market distortion and crowding out: non-beneficiary firms may face competitive disadvantages, and private investors may be displaced as public funding shapes investment patterns. Resource misallocation is possible if sizable public support diverts efforts from more productive alternatives. Universities and research and technology organisations may also face overlapping mandates and redundancy with other projects. At EU level, multiple funding

streams (Horizon Europe, Digital Europe, joint procurement) risk inefficient budget allocation if coordination is insufficient. National governments face similar risks of duplication if responsibilities between national and EU initiatives are not clearly aligned.

Pillar II

Given the scale of manufacturing support, Pillar II indirect costs are potentially more significant. For citizens and local communities, major fabs entail high water, energy, and land consumption, which can stress local infrastructure and the environment. For firms, opportunity costs arise because large-scale State aid for fabs may limit resources available for SMEs and early-stage R&D, potentially crowding out innovation-focused support. Facility operators face substantial environmental compliance costs, while local and regional authorities may need to upgrade infrastructure and, in some cases, subsidise utilities. For national administrations, devoting sizeable budgets to semiconductor manufacturing implies trade-offs with other priorities such as SMEs, research, or social policy. If crisis-related export restrictions and information obligations were activated, they could provoke retaliatory action by trading partners and disrupt exports from downstream industries, causing further indirect losses.

Pillar III

Indirect costs under Pillar III are largely contingent. Citizens and consumers could be affected if export controls triggered retaliatory measures that influence prices or availability of goods. For businesses, crisis measures such as export controls and priority-rated orders could restrict market access and disrupt commercial relationships, creating opportunity costs beyond direct compliance. To date, no crisis stage has been declared, so these costs remain hypothetical; they would materialise only if the crisis response toolbox were deployed.

Benefits of the European Chips Act

The Act is designed to generate substantial benefits along the semiconductor value chain, from R&I infrastructure to manufacturing capacity and more resilient supply chains. These benefits can be grouped into direct (immediate outputs and outcomes) and indirect (longer-term systemic effects).

Direct Benefits

Direct benefits include infrastructure established, investment leveraged, jobs created, and enhanced monitoring and coordination capabilities.

Pillar I

Pillar I directly builds technology infrastructures and supports SMEs and start-ups. Quantitatively, five advanced pilot lines are operational in 2025, providing cutting-edge fabrication and packaging capabilities to European firms. Around 60 SMEs and start-ups are already using these facilities, with individual lines expecting dozens of SMEs per year, multiple prototypes, and multi-project wafer runs. A network of 30 competence centres across Member States and Norway supports skills development and technology diffusion; early evidence shows centres training engineers and supporting SMEs, indicating practical uptake.

The Design Platform, currently being established, will provide shared design infrastructure through dedicated coordination, design enablement teams, and cloud-based tools.

The Chips Fund has backed 55 projects with EUR 62 million in grants and EUR 354 million in equity, offering risk capital to innovative firms. A leverage ratio of about 5 suggests each euro of funding mobilises roughly EUR 5 from national and participant investment. The Chips Fund's EUR 425 million EU contribution is expected to crowd in more than EUR 2 billion in additional private and EIF resources. For EU and national administrations, the establishment of a coordinated European semiconductor research ecosystem and strong leverage of national and private funds are key direct benefits.

Pillar II

Pillar II directly increases European manufacturing capacity, mobilises substantial private investment and generates high-quality employment. Semiconductor manufacturers and downstream industries gain new EU-based capacity from eleven FOAK facilities with total investment of EUR 32.2 billion, improving access to local production and reducing exposure to external bottlenecks. Companies benefit from an estimated 16 000 direct high-skill fab jobs and roughly 30 000 indirect jobs in suppliers and services once the FOAK pipeline is fully built out, with a direct wage bill in the order of EUR 0.9 billion per year that supports regional incomes, tax bases and local supply chains. Given total FOAK investment of EUR 32.2 billion and typical aid intensities in the 30-50% range, firms are likely contributing roughly EUR 16-22 billion of private co-investment, corresponding to about 1-1.5 EUR of private funding for every Euro of public support. Overall semiconductor investment commitments in Europe now exceed EUR 80 billion ⁽¹¹³⁾, and demonstrate a strong multiplier effect of State aid. Technological upgrading through smaller technology nodes, advanced packaging technologies and wide-bandgap power electronics strengthens the capabilities of EU semiconductor firms, gives downstream industries access to advanced chips produced in Europe, and supports long-term competitiveness and sovereignty in critical semiconductor value chains, thereby reinforcing the industrial base of the EU and its Member States.

Pillar III

Pillar III directly improves supply chain visibility and coordination. While citizens and consumers are not explicit primary beneficiaries, better intelligence on supply-demand conditions can help avoid or mitigate disruptions, supporting market stability. For businesses, the monitoring mechanism improves predictability and reduces uncertainty by providing information on demand trends and supply bottlenecks across the value chain, leading to better planning and investment decisions. For EU and national administrations, the monitoring system and European Semiconductor Board provide a stronger evidence base for policymaking, enable earlier identification of risks, and support more timely, targeted use of crisis instruments if needed.

⁽¹¹³⁾ This figure represents both announced and planned investments in the context of Pillar II FOAK projects and past microelectronics IPCEIs.

Indirect Benefits

Indirect benefits are the broader, longer-term effects on innovation, resilience, skills, and competitiveness that build on the Act's direct outputs.

Pillar I

Pillar I indirectly reinforces the innovation ecosystem, human capital, and downstream sector performance. Citizens and consumers benefit from a more innovative economy and stronger EU industrial competitiveness in sectors such as automotive, artificial intelligence, and defence, which depend on advanced semiconductors. Students, engineers, and technicians gain from expanded training opportunities and better employment prospects. For businesses, innovation and knowledge spillovers emerge as more firms access pilot lines and competence centres: about 60 SMEs and start-ups already use pilot lines, with around 41% of supported entities being newcomers, showing that the initiative opens up the ecosystem. At least 100 trainees across several programmes demonstrate early progress in skills development. SMEs and start-ups benefit from technology diffusion and collaboration, while larger firms gain from supply chain synergies and access to innovations coming out of publicly supported infrastructure. Upcoming talent development calls of EUR 45 million in 2026 are set to deepen these effects. Downstream sectors gain through more dependable chip supply and productivity improvements. For EU and national administrations, enhanced resilience and reduced dependency on external fabrication capacity, combined with a more skilled workforce, constitute important strategic benefits, with each Member State hosting at least one competence centre and early evidence of local spillovers.

Pillar II

Pillar II indirectly improves supply chain resilience, fosters regional development, and raises global competitiveness. For citizens and consumers, the existence of critical semiconductor capacity within Europe reduces vulnerability to external shocks, while communities near manufacturing clusters benefit from increased economic activity and a more dynamic innovation environment. Regional clustering in locations such as Dresden and Crolles generates multiplier effects as suppliers, services, and skilled workers concentrate around anchor fabs. For businesses, more resilient EU supply chains translate into reduced exposure to global disruptions, while knowledge transfer and spillovers strengthen the wider innovation system through collaborations between fabs, equipment providers, and research institutes. Increased global competitiveness allows EU semiconductor firms to remain at or near the technological frontier rather than relying on foreign competitors, offering strategic advantages. For public authorities, stronger supply chain security and reduced strategic vulnerability demonstrate the value of coordinated industrial policy and provide a template for future initiatives in other critical sectors.

Pillar III

Pillar III indirectly supports better market functioning, more responsive policy, and long-term optimisation of semiconductor supply chains. Citizens and consumers benefit from more stable markets and improved supply continuity, supported by the existence of crisis-response structures even if they are not yet activated. For businesses, systematic data collection and analysis can dampen extreme inventory cycles and help align capacity with demand, reducing costly mismatches. For EU and national administrations, the information and analytical

capabilities developed under Pillar III enable more evidence-based decisions, both in crisis situations and in routine adjustments to the policy framework governing the semiconductor sector.

CBA tables by pillar

Table 3. Pillar I CBA table

	Overview of costs and benefits identified in the evaluation: Pillar I							
		Type	Citizens / Consumers		Businesses		Administrations (EU and national)	
			Quantitative	Comment	Quantitative	Comment	Quantitative	Comment
Direct financial costs	Public expenditure/grants funding	Recurring (annual)	No financial costs incurred.		No financial costs incurred		EU: total of EUR 1960.5 million (92.3 million for Competence Centres, 25 million for Design Platform, 1831.2 million for Pilot lines, and 12 million for design-related activities). National: total of EUR 1957.3 million (95.3 million for Competence Centres, and 1862.1 million for Pilot lines).	
	Capital investment and operational expenditure to Pilot lines	One-off + Recurring (annual)	No financial costs incurred.		Industry consortia and RTOs cost-sharing, in-kind contributions, cost-sharing for pilot line operations cannot be reliably isolated.		EU: total of EUR 1831.2 million (898.5 million for HE grants, 45.1 million for DEP grants, and 887.7 million for DEP JPA). National: total of EUR 1862.1 million (554.3 million for HE grants, 45.1 million for DEP grants, and 1262.8 million for DEP JPA).	
	Capital investment and operational expenditure to competence centres	One-off + Recurring (annual)	No financial costs incurred.		No financial costs incurred. Full network-wide numbers regarding operational expenditure are not available yet. Illustrative data show that competence centre RO-SMARTYS trained 50 engineers and supported 20 SMEs, while LMCC hired 28 staff.		EU: total of EUR 92.3 million for 4 years (1 million per year per competence centre, 27 MS + Norway, and a support action). National: total of EUR 95.3 million for 4 years (1 million per year per competence centre, 27 MS + Norway).	
	Capital investment and operational expenditure to Design Platform	One-off + Recurring	No financial costs incurred.		No financial costs incurred.		EU: total of EUR 265 million (the 2024 Call for Expression of Interest and a EUR 25 million Coordination and Support Action in order to select a central consortium, referred to as the PCT, and three 2025 calls: EUR 5 million call for Coordination and Support Actions to set up and integrate Design	

Overview of costs and benefits identified in the evaluation: Pillar I								
		Type	Citizens / Consumers		Businesses		Administrations (EU and national)	
			Quantitative	Comment	Quantitative	Comment	Quantitative	Comment
							Enablement Teams, EUR 15 million call for tenders for the central cloud infrastructure that will support the operation of the Design Platform, and EUR 220 million Grant to identified beneficiary)	
							National: no financial costs incurred.	
	Chips Fund support	Recurring	No financial costs incurred.		EUR 2150 million in planned private leverage. Financial costs to SMEs and start-ups (compliance and application burden). Not possible to quantify.		EU: total of EUR 425 million (300 million for EIC Accelerator, all disbursed to 24 startups, and 125 million for InvestEU, resulting in 116 million in equity investment to 31 companies).	
Direct administrative costs	Administrative cost related to the Chips fund	Recurring	No administrative costs incurred.		Estimated administrative cost for SMEs and start-ups applying to and reporting under the Chips Fund, based on an average of 70 person-days (560 hours) per beneficiary for application, due diligence and reporting, valued at EUR 50-60/hour. For 55 supported projects this yields a total cost of approx. EUR 1.7 million (≈ EUR 30 000 per project).		EU: approx. EUR 5.6 million. Standard cost model combining EIC/EIF staff time and intermediaries' overheads for managing the Chips Fund. Assumes approx. 160 person-days (1 280 hours) per funded project across programme design, calls, due diligence, contracting and monitoring, at EUR 80/hour. For 55 projects this gives an estimated approx. EUR 5.6 million total (≈EUR 100 000 per project, range EUR 80 000-120 000), calculated as average hours × labour cost × number of projects.	
	Administrative and Compliance burden - All Pillar I instruments	Recurring (annual)	No administrative costs incurred.		Semi-quantitative SCM estimate for application and reporting burden across all Pillar I grants (Pilot lines, competence centres, Design Platform, Quantum FPAs). Assumes on average 10-20 person-days per application: midpoint 15 days (120 hours) per participating organisation, at EUR 50/hour. Across 514 participants in 44 projects this yields approx. EUR 3 million in administrative and compliance costs, or approx. EUR 0.75 million per year		EU: approx. EUR 3.1 million per year for Pillar I under the Chips JU. National: approx. EUR 0.7 million total (≈EUR 0.2 million per year), assuming 25 person-days per project across national ministries and agencies.	

Overview of costs and benefits identified in the evaluation: Pillar I								
		Type	Citizens / Consumers		Businesses		Administrations (EU and national)	
			Quantitative	Comment	Quantitative	Comment	Quantitative	Comment
					over a 4-year period.			
Indirect costs	Market distortion / Crowding-out risks	Indirect cost	No indirect costs incurred.		Non-beneficiary firms may face competitive disadvantage; competing private investors may experience displacement of funding.		Potential resource misallocation in broader innovation ecosystem.	
	Duplication / Fragmentation risks	Indirect cost	No indirect costs incurred.		Risk of overlapping mandates for universities/RTOs and redundant investments.		National governments risk redundant investments; EU institutions risk inefficient budget allocation.	
Direct benefits	Pilot lines established, Competence centres operational, Design platform established, SMEs/start-ups supported by Chips Fund	Output (infrastructure)	No direct benefits identified.		Semi-quantitative: by 2025 there are 5 advanced pilot lines and around 60 SMEs/start-ups using them, plus up to 31 competence centres and 55 Chips Fund projects supported (≈EUR 62 million in grants and EUR 354 million in equity).		EU: semi-quantitative; EU funding under Pillar I has enabled 5 pilot lines and 30 competence centres, with initial monitoring showing around 60 SMEs/start-ups accessing pilot lines, roughly 100 trainees and 4 training programmes delivered through competence centres, plus 55 Chips Fund projects supported. National: semi-quantitative; participating states co-finance pilot lines with about EUR 1.86 billion in national contributions against roughly EUR 1.83 billion EU funding, and match EU support of about EUR 1 million per competence centre per year for four years in 30 centres across MS and Norway.	
	Investment leveraged (public-private)	Financial leverage	No direct benefits identified.		Semi-quantitative: the leverage ratio for the Chips Fund stands at about 5, meaning each euro of funding mobilises approximately EUR 5 from national funding and project participant investment. The Chips Fund combines EUR 300 million (EIC) and EUR 125 million (InvestEU) with expected private and EIF resources above EUR 2 billion.		EU: semi-quantitative; with a Chips JU budget of about EUR 4.175 billion and up to EUR 2.875 billion dedicated to the Initiative, a leverage ratio of 2.6 suggests that several additional billions of national and participant investment are mobilised on top of EU contributions to pilot lines, competence centres, design platform and Chips Fund. National: semi-quantitative; Member States jointly contribute around EUR 1.86 billion in co-funding to the five pilot lines and match EU support of about EUR 1 million per competence centre per year for	

	Overview of costs and benefits identified in the evaluation: Pillar I							
		Type	Citizens / Consumers		Businesses		Administrations (EU and national)	
			Quantitative	Comment	Quantitative	Comment	Quantitative	Comment
							four years, while also expected to match sizeable design-platform and skills-related calls (such as the EUR 220 million grant to the design platform PCT and EUR 20 million open-source EDA call).	
Indirect benefits	Innovation and knowledge spillovers, Skills development and training, Enhanced resilience and sovereignty, Downstream sector benefits	Innovation ecosystem, Human capital, Strategic/industrial policy, Competitiveness	Citizens benefit from broader innovation and economic growth.		Semi-quantitative: up to 60 SMEs/start-ups already use pilot lines, with certain lines expecting 40–50 SMEs per year, 20–30 prototypes and about 20 MPW runs annually; at least 100 people have completed training across 4 programmes in the competence-centre network, and newcomers account for about 41% of funded entities.		EU: semi-quantitative; by 2025, the EU supports 5 pilot lines, 31 competence centres and at least 4 training programmes with around 100 trainees, alongside upcoming talent-development calls worth EUR 45 million that will complement competence-centre activities. National: semi-quantitative; each Member State hosts at least one competence centre (30 centres in the EU plus Norway), with early evidence from centres such as RO_SMARTYS showing around 20 SMEs supported and 50 engineers trained, indicating potential orders of magnitude for national spillovers as centres mature.	
			Students, engineers, technicians benefit from training opportunities. Employment prospects improved.		SMEs/start-ups benefit from technology diffusion; large firms from supply chain synergies.			
			EU citizens benefit from reduced dependency and supply chain security.		Industry gains skilled workforce.			
			Citizens benefit from improved competitiveness of EU industries (automotive, AI, defence).		Industry benefits from reduced dependency on external fabs and improved supply chain security.			
			Downstream industries (automotive, AI, defence, IoT) benefit from improved chip supply and innovation. Productivity gains, reduced supply chain disruptions.					

Table 4. Pillar II CBA table

Overview of costs and benefits identified in the evaluation: Pillar II								
		Type	Citizens / Consumers		Businesses		Administrations (EU and national)	
			Quantitative	Comment	Quantitative	Comment	Quantitative	Comment
Direct financial costs	Public subsidies for manufacturing facilities	One-off + Recurring	No financial costs incurred.		Private investments as required to get access to State aid.		Eleven State aid decisions for FOAK facilities: EUR 31.6 billion total public + private investment. No EU-level financial costs incurred..	
	Investments by industry in IPCEI	One-off	No financial costs incurred.		Private investment of EUR 13.7 billion in IPCEI.		IPCEI: EUR 21.8 billion (13.7bn private + 8.1bn State aid). No EU-level financial costs incurred.	
	Operational costs of new facilities	Recurring (annual)	No financial costs incurred.		Chip manufacturers and facility operators face annual OPEX (labour, utilities, maintenance). Full operating cost data are not available yet as labour costs and energy consumption will drive costs.		No financial costs incurred	
	Administrative and compliance costs for State aid instrument	Recurring (annual)	No administrative costs incurred.		Assuming subsidised firms spend around 50 person-days per year (400 hours) on preparing and updating State aid applications, audit files and reporting, at roughly EUR 80/hour fully loaded. This gives an annual administrative and compliance cost of about EUR 32 000 per beneficiary firm , which for a stylised group of 30 subsidised projects corresponds to roughly EUR 1.0 million per year borne by businesses.		EU: assuming about 40 person-days per project per year (320 hours) for assessing notifications, approving schemes or individual support and monitoring compliance, at an average EUR 90/hour. This implies around EUR 28 800 per project per year , which for 30 projects gives an estimated EUR 0.9 million in annual administrative cost at EU level. National: assuming roughly 60 person-days per project per year (480 hours) for preparing and notifying aid, liaising with the Commission, issuing decisions and checking compliance, at an average EUR 80/hour. This yields about EUR 38 400 per project per year , or approximately EUR 1.2 million per year across 30 subsidised projects , as a recurring administrative cost for Member States.	
Indirect costs	Economic costs for	Indirect economic	No indirect costs incurred.		Competing firms not granted FOAK recognition		EU: recognising FOAK facilities can create	

	Overview of costs and benefits identified in the evaluation: Pillar II							
		Type	Citizens / Consumers		Businesses		Administrations (EU and national)	
			Quantitative	Comment	Quantitative	Comment	Quantitative	Comment
	recognition of FOAK facilities – market distortion risks	cost			face relative disadvantage. Non-recipient semiconductor firms (especially SMEs, fabless companies) and competing global players face risks from subsidy race.		indirect economic costs if support confers exclusive advantages on a small number of labelled players, distorts competition and contributes to global subsidy races, even though safeguards such as funding-gap tests and clawback mechanisms are intended to limit overcompensation and crowding out. National: FOAK recognition and large, facility-specific subsidies risk skewing investment patterns towards a few host countries, placing non-host Member States and non-recipient firms at a relative disadvantage and creating budgetary trade-offs, while fragmented national support and limited EU-level coordination can amplify subsidy-competition dynamics within the Union.	
	Opportunity costs for State aid instrument	Indirect cost		Citizens face opportunity cost of funds allocated to fabs instead of alternative social investments.		Smaller firms and RTOs may receive less support for innovation vs. large-scale manufacturing.		National governments face budgetary trade-offs (fabs vs. SMEs, R&D, or alternative sectors).
	Environmental and infrastructure costs	Indirect cost		Local communities face environmental impact from high water, energy, and land use by new fabs.		Facility operators face high environmental compliance costs under EU standards.		National/local authorities face infrastructure upgrade costs and utility subsidy requirements.
Direct benefits	New manufacturing capacity created, Jobs created, Private investment mobilised, Technological upgrading	Output (infrastructure), Employment and income, Financial leverage, Technology leadership		Local workforce benefits from high-skill jobs (construction + permanent fab employment). Citizens benefit from access to advanced technology products.		Semiconductor manufacturers and downstream industries gain new EU-based capacity from eleven FOAK facilities with total investment of EUR 32.2 billion, improving access to local production and reducing exposure to external bottlenecks. Companies benefit from an estimated 16 000 direct high-skill fab jobs and roughly 30 000		EU and MS gain strengthened industrial base. Authorities benefit from employment growth and expanded tax base. For EU and MS the eight FOAK facilities imply around 16 000 permanent high-skill jobs plus tens of thousands of construction and indirect jobs, with a direct wage bill in the order of EUR 0.9 billion per year that supports regional incomes and tax bases.

Overview of costs and benefits identified in the evaluation: Pillar II								
		Type	Citizens / Consumers		Businesses		Administrations (EU and national)	
			Quantitative	Comment	Quantitative	Comment	Quantitative	Comment
					indirect jobs in suppliers and services once the FOAK pipeline is fully built out, supporting stable staffing, in-house capabilities and local supply chains. Industry gains investment opportunities. Given total FOAK investment of EUR 32.2 billion and typical aid intensities in the 30-50% range, firms are likely contributing roughly EUR 16-22 billion of private co-investment, corresponding to about 1-1.5 EUR of private funding for every Euro of public support. EU semiconductor firms gain upgraded capabilities (smaller technology nodes, advanced packaging technologies).		EU and MS demonstrate policy effectiveness through leverage ratio. Overall semiconductor investment commitments in Europe now exceeds EUR 80 billion, demonstrating a strong multiplier effect of State aid. For EU and MS the concentration of investment in advanced nodes, wide-bandgap power electronics, packaging and photonics strengthens Europe's technological capabilities beyond mature processes and supports long-term competitiveness and sovereignty in critical semiconductor value chains.	
Indirect benefits	Resilience of EU supply chains, Increased global competitiveness, Regional development and clustering, Knowledge transfer and spillovers	Strategic/industrial policy Industrial policy outcome Regional cohesion Innovation ecosystem	EU citizens benefit from supply chain security and reduced vulnerability to global shocks. Citizens benefit from stronger EU industrial position globally. Local communities benefit from spillover economic growth in semiconductor clusters (e.g., Dresden, Crolles). Citizens benefit from broader innovation ecosystem strengthening.		Industry faces lower risk from global shocks; downstream sectors gain stable chip access. EU semiconductor firms gain improved market position vs. US/Asia competitors. Investors/shareholders benefit from returns. Benchmark of EU vs global fabs in cost, yield, capacity, process node. SMEs in supply chain benefit from supplier contracts and partnerships. SMEs/start-ups gain access to advanced technology through collaborations. Number of joint projects with RTOs/universities, patents/publications co-authored, SME collaborations.		EU and MS gain supply chain security.	

Table 5. Pillar III CBA table

Overview of costs and benefits identified in the evaluation: Pillar III								
		Type	Citizens / Consumers		Businesses		(EU and national)	
			Quantitative	Comment	Quantitative	Comment	Quantitative	Comment
Direct financial costs	Priority-rated orders	Contingent (if crisis activated)	No financial costs incurred		Semiconductor manufacturers must comply with priority orders, facing loss of revenue from deprioritised customers, production disruptions, foregone contracts, strained business relations. These are opportunity costs. Downstream customers not prioritised may face delays or shortages if crisis stage declared.		No actual costs incurred yet.	
Direct administrative costs	Monitoring mechanism costs	Recurring (annual)	No administrative costs incurred.		Assuming around 50 key semiconductor firms are regularly surveyed, each spending roughly 160 hours per year (about 20 person-days) collecting and reporting supply-chain data at EUR 70/hour, the annual compliance cost of the monitoring mechanism for industry is about EUR 0.6 million in total (≈EUR 11 000-12 000 per firm).		EU: If around 8 dedicated FTEs across DG CNECT and the ESB work on monitoring at an average fully loaded cost of EUR 120 000 per year, complemented by roughly EUR 0.5 million in analytical support contracts, the annual EU-level monitoring cost is around EUR 1.5 million . National: Assuming in each of the 27 MS about 0.5 FTE (≈800 hours a year) in relevant ministries and agencies is devoted to data provision at EUR 70/hour, the annual national administrative cost of feeding the EU monitoring mechanism is roughly EUR 1.5 million in total, or about EUR 55 000 per MS .	
	Crisis coordination costs	Recurring (annual)	No administrative costs incurred.		Industry faces costs of engagement in consultations and compliance with crisis protocols (when activated).		EU and MS face coordination costs, administrative participation, reallocation of staff. Costs have been minimal to date as no crisis stage declared.	

Overview of costs and benefits identified in the evaluation: Pillar III								
		Type	Citizens / Consumers		Businesses		(EU and national)	
			Quantitative	Comment	Quantitative	Comment	Quantitative	Comment
	Export restrictions and information obligations	Contingent (if crisis activated)	EU trading partners may impose retaliatory measures if export controls activated.		Semiconductor manufacturers face restricted market access and compliance costs. Exporters in downstream industries face delays and trade disruptions. Lost export revenues, potential retaliation from trade partners.		No actual costs incurred yet. These are contingent costs that would only materialise if crisis stage declared and export restrictions implemented.	
	Legal and enforcement costs	Contingent (if crisis activated)	No administrative costs incurred.		No administrative costs incurred.		EU (DG COMP involvement) and national authorities (customs, regulators, trade ministries) face legal enforcement costs if crisis measures implemented. Costs minimal to date.	
Indirect costs	Indirect costs	n/a	No indirect costs incurred.		No indirect costs incurred.		No indirect costs incurred.	
Direct benefits	Supply chain monitoring mechanism established, Crisis coordination framework in place, Early warning of disruptions	Output (systemic visibility) Output (institutional preparedness) Risk mitigation	No direct benefits identified.		Industry benefits from predictability and reduced uncertainty through supply/demand trend visibility. Industry benefits from predictable crisis management protocols and clearer roles. Industry gains ability to adjust production planning. Downstream sectors benefit from early risk awareness through monitoring and reporting obligations.		EU and MS gain better evidence base for policymaking decisions. EU institutions gain coordination capacity; national authorities have clearer roles in crisis response.	
Indirect benefits	Faster crisis response capacity, Improved resilience of EU supply chains, Strengthened EU global position	Contingent (if crisis activated) Strategic/industrial policy Geopolitical influence	EU citizens would benefit from continuity of supply for essential products if crisis stage activated and measures effective. Society at large benefits from reliable supply of critical products through structural risk management. Citizens benefit indirectly from		Critical downstream industries (from the critical sectors, including , defence, health) would benefit from reduced disruption severity/duration through priority-rated orders and export restrictions if triggered. Industry benefits from reduced vulnerability to supply shocks through structural risk management mechanisms.		These benefits remain contingent on formal declaration of semiconductor crisis stage. As no such crisis has occurred to date, these benefits have not yet materialised. EU institutions and MS gain enhanced resilience capacity. EU institutions gain strategic autonomy in crisis governance of semiconductors. Global partners benefit from predictability of EU response.	

	Overview of costs and benefits identified in the evaluation: Pillar III							
		Type	Citizens / Consumers		Businesses		(EU and national)	
			Quantitative	Comment	Quantitative	Comment	Quantitative	Comment
			enhanced EU strategic autonomy.					

