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Subject:	PART 2/3 COMMISSION STAFF WORKING DOCUMENT IMPACT ASSESSMENT REPORT Accompanying the document Proposal for a Regulation of the European Parliament and of the Council on a framework of measures for strengthening Europe's semiconductor ecosystem repealing Regulation (EU) 2023/1782 (Chips Act 2.0)

Delegations will find attached document SWD(2026) 504 annex.

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PART 2/3

COMMISSION STAFF WORKING DOCUMENT

IMPACT ASSESSMENT REPORT

Accompanying the document

Proposal for a Regulation of the European Parliament and of the Council

on a framework of measures for strengthening Europe's semiconductor ecosystem repealing Regulation (EU) 2023/1782 (Chips Act 2.0)

{COM(2026) 504 final} - {SEC(2026) 504 final} - {SWD(2026) 505 final}

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ANNEX 1: PROCEDURAL INFORMATION

1. LEAD DG, DECIDE PLANNING/CWP REFERENCES

This Staff Working Paper was prepared by the Directorate-General for Communications Networks, Content and Technology.

The Decide reference of this initiative is PLAN/2025/2008.

This includes the Impact Assessment report as well as, annexed to the report, the Evaluation of the Chips Act.

2. ORGANISATION AND TIMING

The Impact Assessment was prepared by DG CONNECT as the lead Directorate-General.

The Inter-Service Steering Group established for the work streams on online platforms was associated and consulted in the process, under the coordination of the Secretariat-General, including the following services: DG BUDG (DG Budget), DG CLIMA (DG Climate Action), DG COMP (DG Competition), DG DEFIS (DG Defence Industry and Space), DG ECFIN (DG Economic and Financial Affairs), DG EMPL (DG Employment, Social Affairs and Inclusion), DG ENV (DG Environment), DG FISMA (DG for Financial Stability, Financial Services and the Capital Markets Union), DG GROW (DG Internal Market, Industry, Entrepreneurship and SME), DG HERA (DG Health Emergency Preparedness and Response Authority), DG INTPA (DG International Partnerships), JRC (Joint Research Centre), DG MOVE (DG Mobility and Transport), DG RTD (DG Research and Innovation), DG Regio (DG Regional and Urban Policy), DG TAXUD (DG Taxation and Customs Union), EEAS (European External Action Service).

The Secretariat-General and DG CNECT of the European Commission relaunched the Interservice Group for the revision of the Chips Act on the 15th of July 2025. The Group was iteratively consulted on the Impact Assessment of the draft proposal, the Evaluation of the Chips Act and on the key policy measures in the proposed regulation.

3. CONSULTATION OF THE RSB

The Regulatory Scrutiny Board (RSB) hearing took place on 28 January 2026. Following a first negative opinion, the RSB Board gave a positive opinion with reservations on the 30th of March. To address the feedback given by the Regulatory Scrutiny Board, the following changes were made in the Impact Assessment report and its annexes:

Findings of the Board	**Main modifications made in the report to address them**
(1) The measure to incentivise trusted chips is not sufficiently described to allow for the assessment of impacts.	The measure to incentivise chips in public procurement (policy measure 10) was revised into "*Recommend a security of supply*

	declaration for semiconductors in public procurement". Concretely, the revised PM10 would allow public procurement authorities in critical sectors to request from tenderers a supply chain declaration analysing the provenance of semiconductors in the tendered products, outlining their supply chain resilience strategy, in particular with regards to dual sourcing. The declaration would also need to assess the quota of semiconductors supplied from domestic undertakings or equivalent[1]. The public procurement authorities may use the supply chain resilience strategy as outlined in the declaration, and the quota of domestic or equivalent semiconductor suppliers, as award criteria along with price. (See further Section 5.2.3.3 and Section 6.2.1.3 of the main document)
(2) The report does not adequately analyse coherence with the existing and forthcoming policy initiatives and instruments. It is not sufficiently clear how interplay will be ensured to achieve synergies between the supply- and demand-side measures.	The interplay between the various measures, in particular the supply side and demand side measures, covering the whole value chain is explained in Sections 5.2, 6.2 and 8.2. Additional elements on coherence with other existing or upcoming policy measures (incl. to the CSA 2 proposal) and instruments were integrated in the report (Section 1.2).
(3) The analysis of the risk of inefficient allocation of resources is not sufficient.	The revised report assesses the costs of individual measures without prejudice to ongoing MFF negotiations. (Section 6 and Section 8; Annex 3 and Annex 4).

[1] See Article 2 of Chips Act 2.0.

ANNEX 2: STAKEHOLDER CONSULTATION (SYNOPSIS REPORT)

1. INTRODUCTION

This annex presents an overview of the five consultation activities: the open public consultation (OPC), call for evidence, surveys, expert interviews, and workshops. In line with the Terms of Reference and the Commission's Better Regulation Guidelines, it summarises findings across the evaluation criteria (effectiveness, efficiency, coherence, EU added value, and relevance), as well as prospective outcomes. This annex presents the stakeholder consultation findings and clarifies how they have been incorporated into the evaluation and policy-making process.

2. OUTLINE OF THE CONSULTATION STRATEGY AND METHODOLOGY

Stakeholder consultation is the structured process through which the Commission and its contractors gather information and perspectives from stakeholders regarding the Chips Act. The consultation strategy defines the scope, identifies the stakeholder groups to be reached, and clarifies the purpose of each activity.

The approach followed the Commission's Better Regulation Guidelines and comprised three main steps:

- Designing the consultation strategy;
- Conducting the consultation activities;
- Informing policymaking through the preparation of our reports.

The consultations aimed to gather stakeholder views and collect data to address the evaluation questions. Findings are presented by consultation method and stakeholder group, and were triangulated with evidence from other data collection and analysis activities.

The consultation tools were designed to be complementary. Surveys and the call for evidence provided broad input, particularly on effectiveness and efficiency, while interviews and workshops with stakeholders (including industry, research organisations, and external experts) supported more in-depth assessment of relevance, coherence, and EU added value. The OPC covered all evaluation criteria and enabled stakeholders and the wider public to share views on the Chips Act's implementation.

Although the study provides an overall evaluation of the Chips Act, the consultation findings are presented with a forward-looking focus, reflecting stakeholder suggestions for improvement. These insights are integrated in the final evaluation report alongside evidence from other methods.

Table 1. Main information on stakeholder consultation activities

Consultation activity	Target groups		Dates
• Open public consultation	• Organisations ▪ Individual respondents		5 September 2025 - 28 November 2025
• Call for evidence	• Organisations • Industry stakeholders • Research institutions	• Public authorities • NGOs	5 September 2025 - 28 November 2025
• Survey	• National and regional authorities • Industry users	• Supply chain actors • Research and design (R&D) organisations	24 October 2025 - 24 November 2025
• Interviews	• EU industries • Policymakers • Industry representatives	• Key investors • Interest groups/alliances • Worker unions	4 November 2025 - 19 November 2025
• Workshops	• Industry representatives • Regional and institutional actors • Research and academic organisations	• Supporting ecosystem • European Commission representatives	12 September 2025 - 17 December 2025

3. METHODOLOGICAL ADAPTATIONS AND LIMITATIONS

The consultation strategy was adapted during implementation. Initial stakeholder participation in the OPC and survey was relatively low, so additional targeted consultations were integrated into the consultation plan. Focus groups were replaced by several thematic workshops to allow broader participation. These included workshops with different stakeholder groups. With increased participation in the OPC and survey, the final consultation results reflect **a well-balanced mix of quantitative and qualitative inputs**. Besides, findings were triangulated across multiple sources, with each conclusion based on at least two independent data sources. Section 4 provides a comparison table showing consistency across consultation activities. Finally, the analysis focuses on outputs and early outcomes, reflecting the Act's recent entry into force (September 2023). Self-selection bias was mitigated through diverse methods and outreach to underrepresented groups. Limited financial data for Pillar II facilities (due to ongoing construction and confidentiality) were addressed through cost modelling and qualitative validation.

4. SUMMARISED RESULTS OF THE OPEN PUBLIC CONSULTATION (OPC)

The OPC was conducted over a **12-week period, from 5 September 2025 to 28 November 2025**. The questionnaire consisted of five sections covering respondent identification, views on the functioning of the current Chips Act, perspectives on possible future steps under a potential "Chips Act 2.0", stakeholder-specific questions, and an option to upload supporting documents. The open public consultation was available in all 24 EU official languages. It included both closed-ended and open-ended questions, allowing respondents to elaborate on their views. In total, **105 survey responses and 39 position papers** were received. One response was identified as a duplicate and another as a test submission; both were excluded, resulting in 103 responses included in the analysis.

The **statistical analysis of closed consultation questions** combined high-level aggregation with disaggregated insights by stakeholder group, enabling the identification of emerging trends within specific groups and helping to contextualise broader patterns across responses. To facilitate the analysis, more granular stakeholder categories were clustered into higher-level groups.

The **qualitative analysis of open-ended responses and position papers** used a hybrid approach, combining Large Language Model (LLM)-driven topic modelling with expert human validation to ensure a structured, consistent, and robust synthesis of stakeholder input across all evaluation criteria.

Two **organised campaigns** with 21 contributions were identified, primarily representing stakeholders from the European semiconductor and electronics ecosystem, including the EuroPractice consortium. Although campaign respondents did not submit identical answers to the closed questions, they repeated key messages across multiple open-ended questions; their inputs are therefore included in the closed-question analysis. The campaigns emphasised that revising the EU Chips Act must sharpen Europe's strategic focus on semiconductor innovation, industrial deployment, and competitiveness by improving funding tools, reducing bureaucracy, and strengthening collaboration across the value chain.

The OPC was answered predominantly by **organisations** (84%, 87/103), with **individual respondents** comprising 16% (16/103). Most responding organisations were international in scope (74%, 64/87) and primarily large enterprises with ≥250 employees (51%, 44/87), although medium (22%, 19/87) and small enterprises (21%, 18/87) were also represented.

Geographically, responses came **mainly from EU Member States** (91%, 94/103), with Germany contributing the most (26), followed by France (16) and Italy (10). Non-EU participation was limited to 9 responses, primarily from the United States (3) and Switzerland (2). Among individual respondents, a clear majority held EU nationality (88%, 14/16).

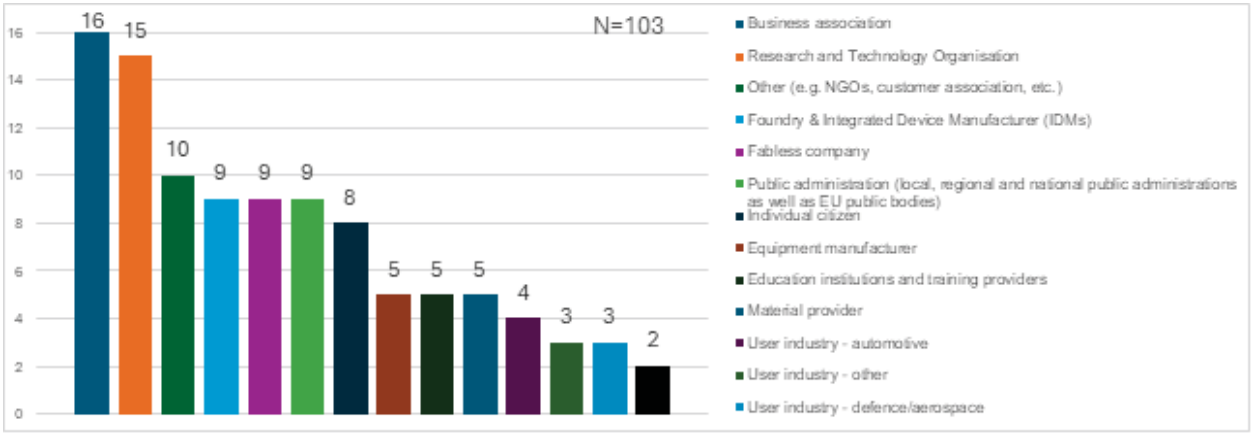


Figure 1. Stakeholder types

Source: Consolidated public consultation of the review of the Chips Act, September-November 2025, Question 2.

4.1. Effectiveness

The consultation results indicate strong positive assessments of Pillar I (Chips for Europe Initiative) across all stakeholder groups. Supporting research and innovation activities was the highest-rated objective, while progress on security-by-design principles for cybersecurity protection ranked somewhat lower in comparison. Position papers broadly align with these trends, with stakeholders consistently identifying Pillar I activities, such as pilot lines, competence centres, and start-up support, as having strengthened Europe's innovation infrastructure and supported technological capacity building. Concrete examples cited include support for start-ups and local benefits such as job creation.

Regarding **pilot lines** specifically, more than half of respondents (59%, 56/96) considered that they meet their objectives of supporting the transition from 'lab to fab', with RTOs/designers (76%, 13/17) and authorities (78%, 7/9 respectively) expressing the strongest positive views, while civil society and supply-chain respondents were more cautious. Answers to open-ended questions suggest that further industrialisation of pilot lines could be supported through state-aid framework reform (GBER revision) and sustained funding support, while end users highlighted the importance of market-driven orientation from the outset. Across sources, stakeholders note that closing the gap between innovation and industrial-scale production remains crucial to achieve high-volume production capabilities.

Competence Centres are broadly viewed as too early to assess fully, though some respondents representing RTOs/designers raised questions about inclusiveness for regional actors and noted operational considerations including budget constraints (civil society and economic stakeholders) and non-unified service costs (public authorities). When asked about other activities that could be covered, most stakeholders suggested waiting until centres become fully operational before expanding their remit.

At the same time, stakeholders express doubt that the 20% market share target is realistic under current conditions. Overall, position papers **characterise the Chips Act as a timely crisis response that created important momentum**, while emphasising that Europe now requires substantially scaled and more comprehensive intervention to achieve meaningful strategic outcomes.

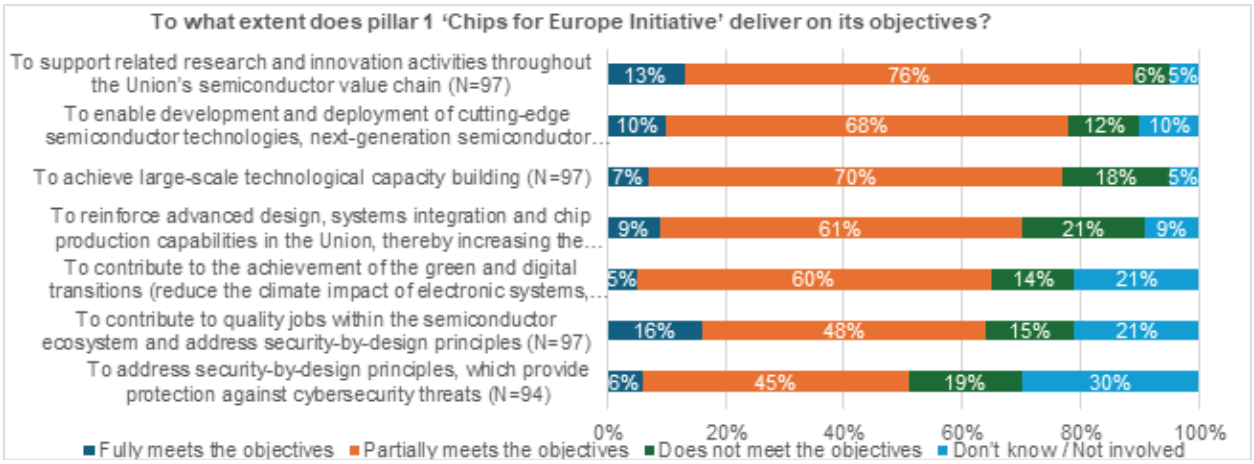


Figure 2. Achievement of Pillar I objectives

Source: Consolidated public consultation of the review of the Chips Act, September-November 2025, Question 6.

Pillar II (Security of supply and resilience) also received broadly positive assessments. Three quarters of respondents (75%, 60/97) considered that this Pillar fully or partially meets its objectives, with supply-chain respondents (70%, 19/27) and end users (67%, 8/12) expressing the strongest positive views, while authorities were more cautious 44% (4/9). A similarly large majority (71%, 69/96) indicated that Pillar II has made the EU a more attractive location for semiconductor manufacturing. Position papers note that while the Chips Act has mobilised substantial investment, questions remain about whether current funding levels are sufficient to keep pace with global competitive dynamics. Stakeholders also identify gaps in the value chain, including Europe's PCB manufacturing capacity and back-end manufacturing, which are perceived as undermining front-end investments and contributing to dependencies on non-European suppliers.

Pillar III (Monitoring and crisis response) received comparatively lower assessments. Almost a third of respondents (30%, 29/96) considered that Pillar III fully or partially meets its objectives, with an equal share indicating that objectives are not met. End users and civil society/economic stakeholders expressed the strongest positive views (each 33%, 4/12 and 11/33), while authorities reported the lowest (22%, 2/9). Current uptake of monitoring mechanisms remains limited: two-thirds of respondents (66%, 61/93) reported they had not developed or implemented monitoring systems within their organisations, and a similar proportion (66%, 57/86) indicated they have never reported or received alerts about potential supply chain disruptions. When asked in open-ended questions about suggested additions and changes to Pillar III, there was broad agreement across stakeholders that the Pillar requires further development beyond its current focus on shortage management, with supply-chain stakeholders highlighting practical concerns around information-sharing and export control frameworks.

Regarding chip supply shortages over the past 12-24 months, respondents most commonly reported experiencing shortages in final chips (39%, 22/57) and raw materials (26%, 15/57).

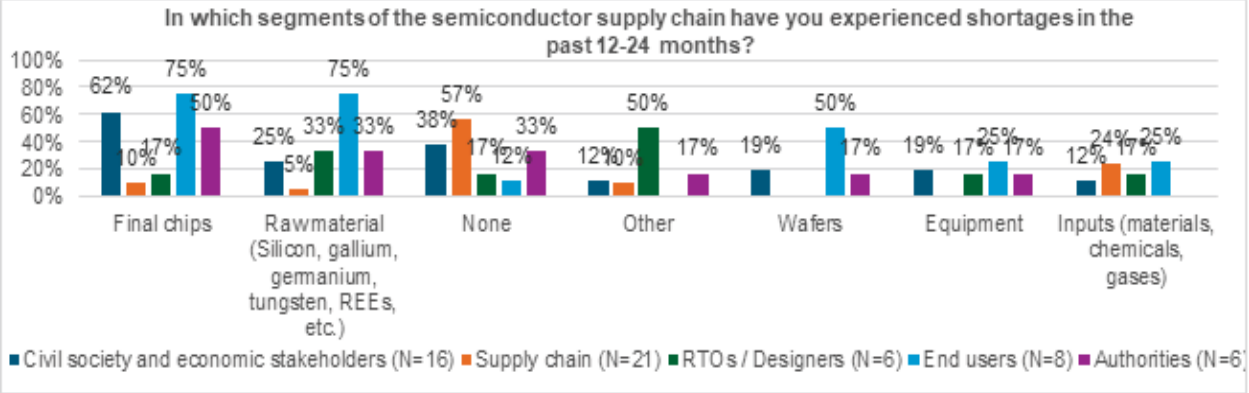


Figure 3. Supply shortages

Source: Consolidated public consultation of the review of the Chips Act, September-November 2025, Question 26.

Looking ahead at the next 2-3 years, a large majority (83%, 68/82) **of respondents anticipate further disruptions**. Geopolitical risks (82%, 64/78) and new trade barriers (81%, 63/78) emerged as the most frequently cited **threats** across stakeholder groups, followed by logistic bottlenecks (35%, 27/78) and natural hazards (26%, 20/78). Position papers echo these concerns, with stakeholders observing that Europe's relevance as a semiconductor market has declined relative to other regions, and that capacity gaps in advanced manufacturing nodes leave the EU reliant on a narrow base of non-European suppliers.

Respondents most widely supported diversifying trade partners (83%, 71/86) as a **mitigation measure** across all stakeholder groups, followed by investing in innovation for recycling, advanced materials or substitutes (73%, 63/86). Nearly two-thirds (65%, 51/79) considered it useful to introduce protective measures for the Union's semiconductor sector in the event of a crisis.

Communication effectiveness was assessed positively overall. A large majority (86%, 77/89) indicated that the implementation of the Chips Act has been communicated at least adequately within their relevant Member States, with broadly consistent views across stakeholder groups.

4.2. Efficiency

Experiences with implementation mechanisms varied considerably across stakeholder groups. Among fabless companies who engaged with EU-level initiatives, perceptions were mixed, with equal shares finding them not effective or somewhat effective (each 33%, 3/9). Among RTOs, 67% (6/9) reported having been part of one of the five pilot line projects under Pillar I. Most foundry and integrated device manufacturers rated their experience with the first-of-a-kind framework under Pillar II as neutral or satisfactory (each 44%, 4/9), though two-thirds (67%, 6/9) had not applied for integrated production facility or Open EU foundry status.

Position papers and answers to open-ended questions provide further insight into the challenges underlying these mixed experiences. A consistent finding across stakeholder groups is **concern about procedural complexity and slow timelines**. Stakeholders identify state aid approval delays, IPCEI and FOAK process complexity, administrative burden, and inconsistent pilot line access conditions as key efficiency barriers. The length of state aid approval processes is the most prominent concern, with stakeholders noting that timelines of up to two years from submission to grant notification create uncertainty and represent a competitive disadvantage relative to other semiconductor-producing regions. IPCEI is recognised as a valuable instrument, though its efficiency is seen as constrained by approval timelines, administrative complexity, and funding rates that are perceived as less competitive compared to global counterparts. Respondents also noted that Member States retain primary authority over planning and licensing processes, which can affect permit timelines.

Public authority involvement in supporting semiconductor development varies across functions. Among authority respondents, 67% (6/9) indicated they provide specific incentives to the semiconductor value chain, while 44% (4/9) have been involved in facilitating first-of-a-kind facility investments. Two-thirds (67%, 6/9) reported that their authority has developed a semiconductor strategy at national, regional, or local level. All authorities expressed interest in supporting strategic projects in line with the Commission's proposal for a European Competitiveness Fund.

Regarding **coordination and financing**, three quarters of respondents (75%, 64/85) indicated that strategic project selection and set-up should be coordinated at EU level, with strong cross-stakeholder consensus. A large majority of all respondents (87%, 74/85) favoured financing through a combination of funding sources. In their open-text responses, several respondents representing RTOs/designers highlighted the need to align support with market demand, noting that EU awards alone may not guarantee commercial viability. In terms of beneficial incentives for companies, end-user industry respondents particularly favoured financial support for R&D (89%, 8/9), subsidies for building manufacturing facilities (89%, 8/9), and tax incentives for chip production and usage (78%, 7/9).

4.3. Coherence

A large majority of respondents (86%, 58/67) reported that the **Chips Act has contributed to improving governance and coordination between national and regional authorities**, with 9% (6/67) indicating it contributed very well, 16% (11/67) well, and 61% (41/67) adequately. The strongest positive views came from authorities and RTOs/designers, while end users showed more mixed views. Position papers and open-ended responses indicate scope for further strengthening governance arrangements, including through more structured industry involvement in decision-making processes.

The most prominent **internal coherence** concern identified in position papers is the relationship between research and innovation activities under Pillar I and manufacturing capacity under Pillar II. Stakeholders argue that innovation delivers greater value when supported by clear pathways to industrial-scale production. As DIGITALEUROPE noted, "Pillar 1 and Pillar 2 […] must be more closely integrated. Innovation generated in Pillar 1 only delivers real value when it transitions into industrial-scale manufacturing under Pillar 2", a view echoed by other business associations such as Eurochambres and ESIA. Beyond internal coherence, respondents call for stronger alignment between the Chips Act and adjacent EU policy instruments, including the Quantum Act, Advanced Materials Act, EuroHPC, and EDIP, to ensure complementarity across policy domains. Stakeholders also identify a need for enhanced coordination across EU, national, and regional governance levels, with regional stakeholders emphasising that success depends on research, companies, pilot lines, centres of excellence, and public policy working closely together.

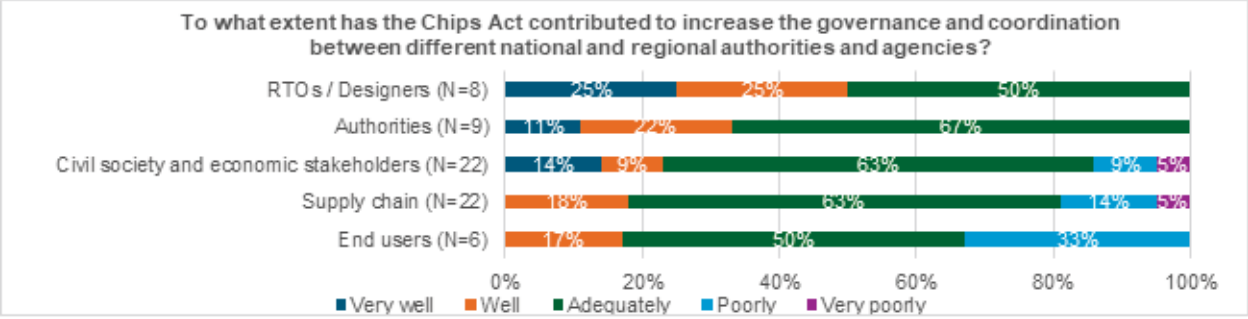


Figure 4. Impact on governance and coordination

Source: Consolidated public consultation of the review of the Chips Act, September-November 2025, Question 31.

Regarding **sustainability**, the majority of respondents (71%, 47/66) reported that their organisation has sustainable practices or policies in place for the semiconductor sector. Supply-chain actors showed the strongest uptake (85%, 17/20), while civil society/economic stakeholders (60%, 12/20) and RTOs/designers (56%, 5/9) showed more varied adoption. Among civil society and economic stakeholders, raw materials extraction was the most widely shared environmental concern (75%, 6/8), followed by high energy consumption, lifecycle assessment capabilities, and water usage. When prioritising concerns related to chips and electronic components, high energy consumption emerged as the top issue (86%, 6/7). In position papers and open-ended questions, some respondents noted potential tensions between environmental regulations and manufacturing requirements, while others observed that sustainability considerations are sometimes deprioritised relative to performance improvements and that incentives may need to target both new and existing equipment. Among business associations, the most frequently cited actions to promote sustainable practices were incentives for green manufacturing and R&D funding for eco-friendly technologies (both 85%, 11/13).

4.4. EU added value

Position papers show strong consensus that EU-level action provides irreplaceable value through coordination mechanisms that should be further strengthened. Stakeholders support a centralised EU-level strategic framework and significant EU budgetary contributions that complement Member State funding. Respondents frame EU coordination as essential for European semiconductor competitiveness, emphasising that it helps minimise fragmentation and enables scale effects that no individual Member State could achieve alone. In response to open-ended questions, authority representatives recommended the European Semiconductor Board as the primary coordination platform, with investments planned according to European priorities and demand to ensure resilient supply chains.

Views on extending information mandates showed no unanimous position across stakeholder groups. Almost half of respondents (47%, 40/85) supported giving the European Commission or National Competent Authorities a mandate to request information from companies along the semiconductor supply chain to prevent future disruptions, with a similar share (47%, 40/86) supporting mandates to address potential vulnerabilities such as overcapacities or dependencies.

International cooperation received strong support across all stakeholder groups. Collaborative R&D and innovation was the most widely supported action area, consistently ranking at or near the top for every group, while supply chain diversification and security of supply was another cross-cutting priority. Position papers similarly call for strengthened international partnerships with key semiconductor-producing nations, proposing more formalised cooperation mechanisms and risk-based frameworks.

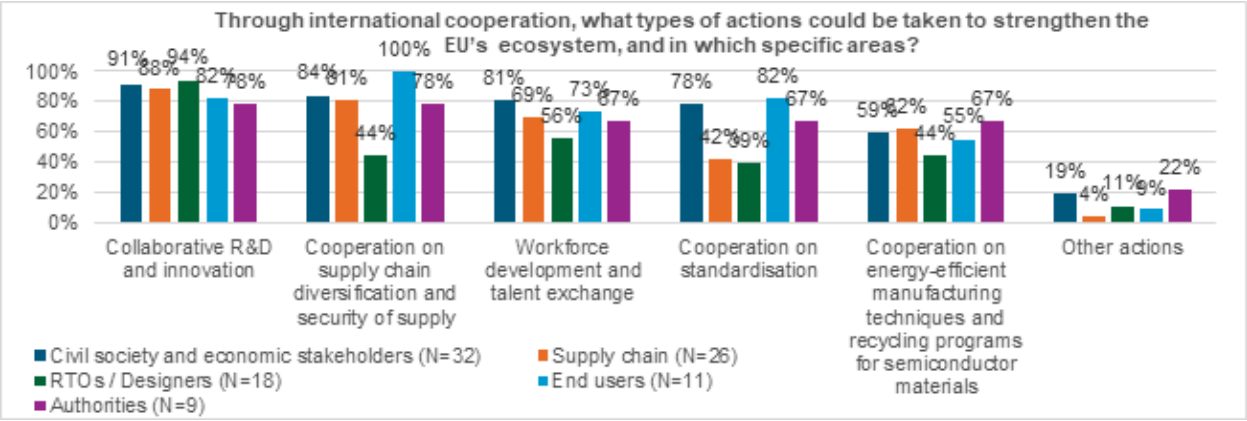


Figure 5. International cooperation actions

Source: Consolidated public consultation of the review of the Chips Act, September-November 2025, Question 63.

All end-user industry representatives (8/8) indicated that the **EU should focus on facilitating technology exchange** in its global semiconductor partnerships, with 88% (7/8) highlighting the importance of building strategic alliances with global leaders, while 75% (6/8) saw value in leading research initiatives. All public authorities (9/9) indicated that they engage in bilateral or multilateral cooperation with third countries in the field of semiconductors, covering areas such as R&D, industrial development, and investment. Among education institutions, half (2/4) indicated that the Chips Act incentivised companies to collaborate with European education institutions and align curricula with labour market needs.

4.5. Relevance

Views on framework adequacy were mixed. One quarter of respondents (25%, 23/94) agreed that the current Chips Act framework provides a sufficiently robust approach to address Europe's supply-side vulnerabilities, while almost half (44%, 41/94) disagreed and one-third (32%, 30/94) expressed a neutral view. RTOs/designers showed the strongest support (62%, 10/16), whereas supply-chain respondents were more cautious, with 56% (14/25) disagreeing. Among authorities, none agreed with the statement, with responses split between neutrality (67%, 6/9) and disagreement (33%, 3/9).

Position papers provide further insight into these reservations. A frequently cited concern is that **the Act's scope places too much emphasis on production capacity targets over alignment with European industrial needs**. As ASML emphasises, "A successful approach to the Chips Act review must not only help develop production capabilities but, more fundamentally, it must

create the framework conditions for industry to create […] an end market for more semiconductors 'made in the EU'." Respondents also note that the Act focuses predominantly on front-end chip manufacturing while giving insufficient attention to adjacent value chain segments, particularly printed circuit boards, packaging, and back-end processes. Design capabilities emerge as a prominent theme, with stakeholders arguing that the production-centric approach does not sufficiently recognise the role of chip design in European value creation. Position papers also highlight a disconnect between Chips Act priorities and the needs of key European user industries, particularly automotive, aerospace, defence, and industrial sectors, as well as emerging technology domains such as quantum, photonics, and AI chips.

Among supply-chain respondents, **key factors when selecting a location for semiconductor-related facilities relate to funding access, administrative ease, and skill availability**. Speed and ease of access to public funding was rated very important by 88% (15/17), while clarity of administrative processes and predictability of funding were similarly emphasised. The most frequently identified **barriers to developing an EU AI chip value chain** were lack of manufacturing capability (59%, 55/93), lack of investment instruments (57%, 53/93), skilled workforce shortages (55%, 51/93), and low domestic demand from hyperscalers or AI companies (55%, 51/93). Views varied across stakeholder groups.

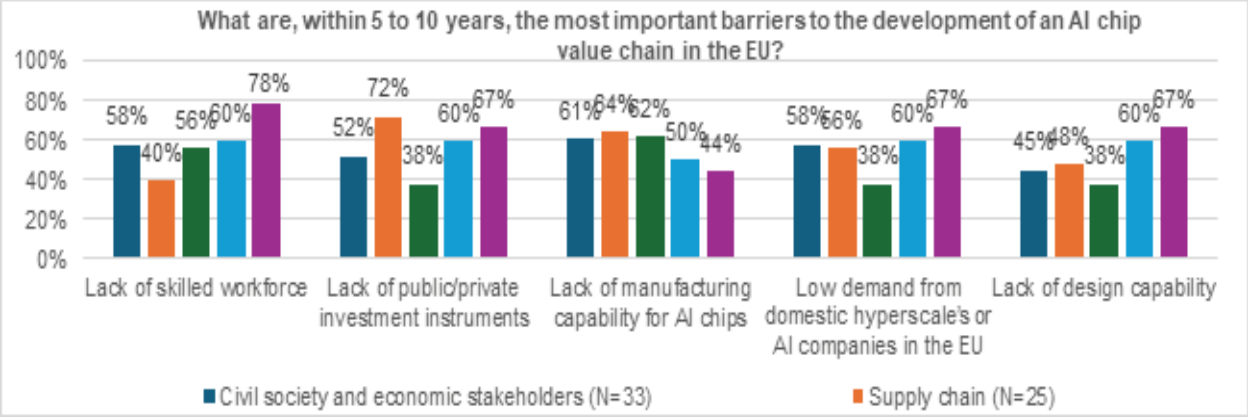


Figure 6. Barriers to AI chip value chain development

Source: Consolidated public consultation of the review of the Chips Act, September-November 2025, Question 42.

Specific obstacles varied by stakeholder type. Fabless companies identified limited access to venture capital and risk finance as the most critical obstacle (78%, 7/9), followed by high cost or limited availability of EDA tools and IP blocks (67%, 6/9). Supply-chain respondents highlighted complex or lengthy permitting procedures and energy costs (each 88%, 15/16). Public authorities unanimously identified access to financing or aid as a key challenge (9/9) to attracting large-scale semiconductor production projects to their region or country, with 78% (7/9) also highlighting skilled labour availability. When asked in open-ended questions what **measures** could mitigate these obstacles, end users emphasised the importance of continuous, proactive Commission dialogue, real-time trade restriction monitoring, early crisis engagement, and complete value chain resilience, extending beyond chip manufacturing. RTOs/designers highlighted EU-level supply observatories with real-time component data and shared strategic reserves for research components. Supply chain stakeholders called for coordinated EU-wide early-warning systems, harmonised export rules and chips diplomacy with like-minded countries.

Regarding **leadership potential**, respondents most frequently identified semiconductor manufacturing equipment as the segment where the EU has strongest potential to gain or reinforce leadership (79%, 70/89), followed by manufacturing of mainstream chips above 28 nm (62%,

55/89) and packaging, testing, and assembly (61%, 54/89). Fewer respondents (29%, 26/89) saw potential for leadership in advanced chip manufacturing below 10 nm. In terms of **end-user industry prioritisation**, defence/aerospace received strongest support (93%, 83/90), followed by automotive (82%, 75/92), energy (82%, 73/89), and data-centre infrastructure (79%, 73/92).

4.6. Prospective

Respondents expressed strong and consistent support for further Union action across all four action areas. Addressing talent shortages received the highest level of agreement, with 94% of respondents (88 out of 94) agreeing or strongly agreeing that the European semiconductor industry faces serious talent shortages requiring investment in attraction, skilling, reskilling, and training policies; notably, 65% (61 out of 94) strongly agreed, the highest intensity across all statements. The need for EU-level coordination of dispersed national strategies followed closely at 88% (83 out of 94), while lowering barriers for fabless companies and innovative semiconductor firms received 87% agreement. Making Europe a more attractive destination for next-generation chip manufacturing received 84% support (80 out of 95). Across stakeholder groups, there was broad convergence on these priorities, though with variations in intensity (see **Figure 7**).

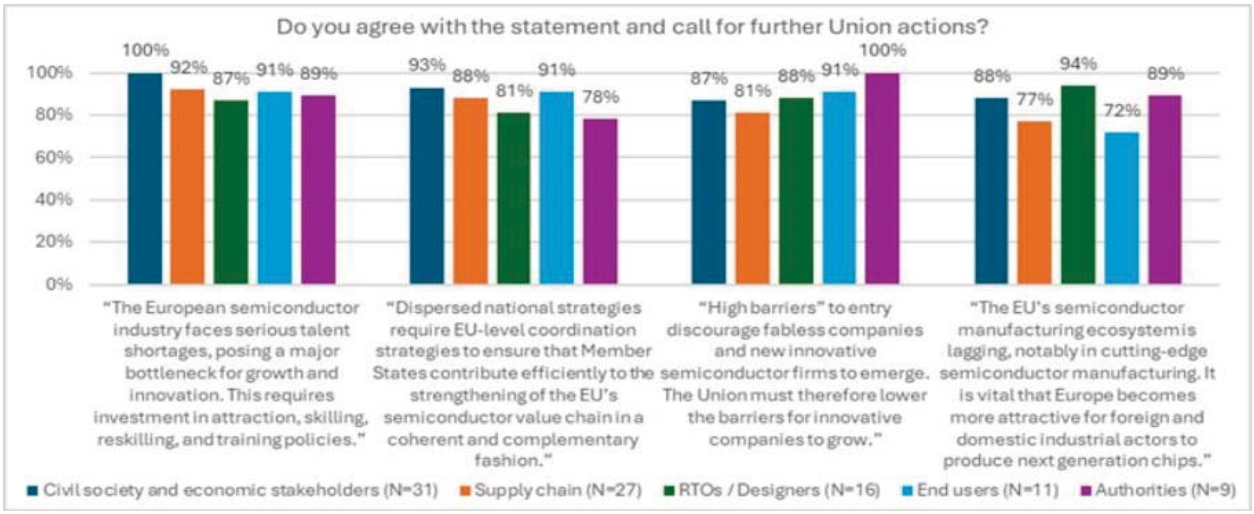


Figure 7. Areas for further Union action (sum of strongly agree + agree)
Source: Consolidated public consultation of the review of the Chips Act, September–November 2025, Question 34.

Position papers provide detailed recommendations for a potential Chips Act 2.0. The core message is that the next phase requires strategic transformation rather than incremental adjustment, moving from a crisis-response instrument to a comprehensive industrial strategy aligned with European demand and competitive positioning.

Design capabilities emerge as one of the most frequently referenced priorities, particularly among supply-chain actors, with proposals for dedicated support to the fabless sector, investment in open-source architectures, and processor development. Stakeholders also call for targeted support for quantum computing, AI chips, and other emerging technologies. Pilot line expansion and lab-to-fab pathways received particular emphasis from RTOs and user industries, building on the recognised success of Pillar I activities. Stakeholders call for enhanced pilot line infrastructure and clearer pathways from research to industrial production across different technology readiness levels.

Scope expansion beyond front-end chip manufacturing to encompass the full electronics value chain received strong emphasis, particularly from business associations. Respondents underlined

the need to widen the FOAK definition under Pillar II to better support the broader semiconductor supply chain and address gaps in PCBs and back-end manufacturing.

Governance and funding reforms feature prominently across stakeholder groups. Proposals include dedicated leadership positions, streamlined procedures through one-stop-shop mechanisms, and strengthened dialogue between policymakers and the European electronics ecosystem. On funding, stakeholders call for structural changes including, consolidated budgets to ensure consistency, dedicated EU budget lines for semiconductors in the next Multiannual Financial Framework and tax incentives to enhance investment attractiveness.

5. SUMMARISED RESULTS OF THE CALL FOR EVIDENCE

The call for evidence was conducted in parallel with the public consultation from **5 September 2025 to 28 November 2025**. Stakeholders were invited to provide open-text responses as well as position papers. In total, **209 responses** were received, including 85 position papers. All inputs were analysed using a hybrid approach combining LLM-driven topic modelling with expert human validation.

The public consultation was answered predominantly by **organisations** (87%, 181/209), with individual citizen respondents comprising 13% (28/209). The largest stakeholder groups were companies/businesses (32%, 66/209), academic/research institutions (26%, 55/209), and business associations (15%, 31/209), followed by NGOs (5%, 10/209), other stakeholders including consumer organisations and trade unions (6%, 12/209), and public authorities (3%, 7/209). Most responding organisations were large enterprises with 250 or more employees (52%, 94/181), though medium (18%, 32/181), small (16%, 29/181), and micro enterprises (14%, 26/181) were also represented.

Geographically, responses came predominantly from **EU Member States** (90%, 188/209), with Germany contributing the highest number (41), followed by France (31), Belgium (21), Spain (19), and Italy (17). Non-EU participation totalled 21 responses, primarily from Switzerland (5), the United Kingdom (5), and the United States (4).

5.1. Effectiveness

Responses and position papers present a nuanced view of the Chips Act's effectiveness. The Act is widely credited with **generating political attention, mobilising substantial investment, and establishing foundational infrastructure**, while stakeholders also identify areas where further progress is needed to achieve intended targets.

On **investment and strategic vulnerabilities**, stakeholders acknowledge substantial investment announcements but question whether current volumes are sufficient to shift Europe's competitive position. Dependence on external suppliers, particularly for advanced nodes, is seen as a continuing area requiring attention. Regarding **specific pillars**, Pillar III monitoring mechanisms are seen as requiring further development to deliver effective supply chain visibility. For Pillars I and II, stakeholders identify considerations related to technology readiness level coverage and project execution. While Pillar I is credited with tangible achievements, the lab-to-fab transition remains an area for improvement, with respondents calling for stronger mechanisms to translate research excellence into industrial-scale production. Several **cross-cutting enablers** emerge. Respondents stress that infrastructure investments should be matched with sustained human-capital development, with academic institutions underscoring the interdependence between skills, research, and industrial capability. Stakeholders also emphasise that improved accessibility and

distribution of support instruments would help maximise the Act's effectiveness, particularly for SMEs and start-ups.

5.2. Efficiency

Responses addressing this criterion primarily focus on **procedural complexity and approval timescales across Chips Act instruments**. Stakeholders across groups identify lengthy approval timelines, administrative burdens, fragmented approaches between EU and national levels, and implementation capacity constraints as areas for improvement.

Approval speed emerges as a prominent concern, with stakeholders noting that European timelines compare unfavourably with other semiconductor-producing regions. These concerns centre particularly on Pillar II instruments, where state aid procedures are seen as lengthy relative to the pace required for timely support, as noted by business associations including DIGITALEUROPE, SEMI Europe, and ESIA. The Important Projects of Common European Interest (IPCEI) mechanism is recognised as important for mobilising large-scale investment, though approval processes are seen as an area for streamlining. **Administrative burden** is closely related. Companies in particular identify multiple sources including complex application procedures and demanding reporting requirements, with smaller companies noting that these pose particular challenges for SMEs and start-ups. For Pillar I, stakeholders call for simpler access mechanisms to the Chips Fund and pilot lines, while for Pillar III, respondents emphasise the need to balance supply chain visibility against reporting burden considerations. **Fragmentation** between EU and national procedures is also identified, with respondents describing parallel processes, inconsistent requirements across Member States, and unclear coordination mechanisms.

5.3. Coherence

Respondents identify coherence as a multi-dimensional criterion spanning internal pillar integration, external policy alignment, and coordination across governance levels – themes that closely mirror those highlighted in the public consultation.

Internally, stakeholders identify scope for stronger alignment between Pillar I innovation activities and Pillar II manufacturing support through dedicated bridging mechanisms to ensure that innovation outputs from pilot lines translate into European manufacturing capabilities. **Externally**, respondents see room for stronger coordination with other EU frameworks such as the AI Act, the Quantum Act, and the Cyber Resilience Act. Stakeholders call for explicit integration between semiconductor policy and broader digital strategies, as well as alignment with defence-industrial policy and economic security frameworks. Coordination across EU, national, and regional governance levels could be strengthened by streamlining funding streams, aligning national approaches, and enhancing central coordination. Reference is made to the European Semiconductor Board as a mechanism to support such alignment. Alignment with **Green Deal objectives** presents both synergies and considerations. Stakeholders recognise semiconductors as key enablers of the green and digital transitions, viewing the Chips Act as an opportunity to support greater circularity, energy efficiency, and sustainable manufacturing. At the same time, some respondents note that future iterations should address the relationship between environmental and industrial policy objectives.

5.4. EU added value

The key theme across responses is a **strong affirmation that EU-level action delivers benefits unattainable through national efforts alone**. Stakeholders consistently point to scale and critical

mass, reduced fragmentation through coordinated action, and shared cross-border infrastructure as core sources of EU added value.

A central element is Europe's ability to **achieve critical mass in investments** that no individual Member State could sustain. Stakeholders emphasise that the semiconductor sector's capital intensity and global competitive dynamics require pooled European resources. Coordination is viewed as equally important, with fragmented national approaches identified as a risk that EU-level action can help mitigate. Stakeholders, particularly academic and research institutions, highlight **shared infrastructure** such as pilot lines and research facilities under Pillar I as concrete examples of EU added value. Distributed manufacturing networks under Pillar III are viewed as requiring EU-level coordination to achieve both economic efficiency and crisis resilience. Citizens and NGOs tend to frame EU added value in terms of **collective resilience and geopolitical positioning**, while public authorities emphasise that EU added value emerges from **connecting regional ecosystems into interregional networks** and leveraging local strengths within a coherent EU framework.

5.5. Relevance

Stakeholders broadly agree that the Act **addresses the overarching challenge of semiconductor resilience and competitiveness but could more closely align solutions with sectoral needs**. Respondents highlight broader questions about whether the Act should shift from self-sufficiency toward indispensability, aligning policy more closely with demand-driven priorities.

Across stakeholder categories, respondents identify an **imbalance between support for leading-edge manufacturing and the needs of mature and mainstream nodes** where European industrial demand is concentrated. Academic and research institutions particularly emphasise that this imbalance "risks weakening Europe's competitive position in the mainstream segments where it already leads" (European University Institute). Stakeholders also identify **value-chain segments** that could benefit from greater attention, including advanced packaging and assembly, printed circuit boards, upstream materials and chemicals, and design capabilities. These observations intersect with Pillar II and the definition of FOAK facilities, with business associations calling for broader FOAK eligibility. Design emerges as the most frequently mentioned area, with stakeholders noting that the current manufacturing emphasis could be complemented by strengthened support for Europe's design ecosystem. Respondents further highlight the **importance of balanced support distribution across stakeholder types**, particularly in addressing barriers faced by SMEs, start-ups, and research institutions.

5.6. Prospective

Respondents provided comprehensive recommendations for a potential Chips Act 2.0, closely linked to the areas for improvement identified under the evaluation criteria and broadly aligned with themes emerging from the public consultation. A cross-cutting message is the need **for sustained, long-term strategic commitment to achieve European semiconductor objectives**.

On **funding**, stakeholders call for a dedicated EU semiconductor budget at substantially increased scale. Closely related is the recommendation to **expand value-chain scope** beyond front-end manufacturing to include packaging, materials, equipment, and back-end processes, accompanied by a revision of FOAK criteria to reflect this broader definition. **Strengthening European design capabilities** emerges as a key priority, with recommendations focusing on architecture sovereignty, open design platforms, and improved access to design tools and infrastructure. Regarding **implementation**, stakeholders advocate for enhanced pilot lines more closely aligned

with industrial scaling requirements, alongside financing mechanisms better suited to SMEs and start-ups. Comprehensive workforce programmes spanning education, training, and talent attraction are emphasised as essential to address skills needs. Strategic international partnerships with trusted partners feature prominently, as does dedicated support for emerging technologies such as quantum, photonics, and AI chips. On **governance**, business associations and public authorities call for strengthened industry-government dialogue and a strengthened European Semiconductor Board to improve strategic coordination.

6. SUMMARISED RESULTS OF THE SURVEY

The survey was administered through Alchemer email campaigns targeting stakeholders identified via desk research and MILD.AI mapping. The initial survey invitation was sent on 24 October 2025, followed by two reminder campaigns: one on November 3rd, a week after initial contact, and a final reminder on 21 November, before survey closure on 24 November 2025. Survey dissemination was further supported by the Austrian Institute of Technology (AIT) and project experts to maximise stakeholder reach across the European semiconductor ecosystem.

The targeted stakeholder survey collected responses from 64 stakeholders. Four tailored questionnaires were designed to capture the specific perspectives of distinct stakeholder groups: national and regional authorities, industry users, supply chain, and research and design organisations. Questions primarily utilised Likert scales (5-point agreement and importance scales) and rating scales, with limited open-ended questions for qualitative feedback. Response options included 'Don't know', 'Too early to tell', and 'Not applicable' where relevant to ensure data quality and avoid forced responses.

National and Regional Authorities constituted the largest share of respondents (37.5%, 24/64), followed by Research and Design organisations (26.6%, 17/64) and Supply Chain actors (25.0%, 16/64). Industry Users represented the smallest group (10.9%, 7/64).

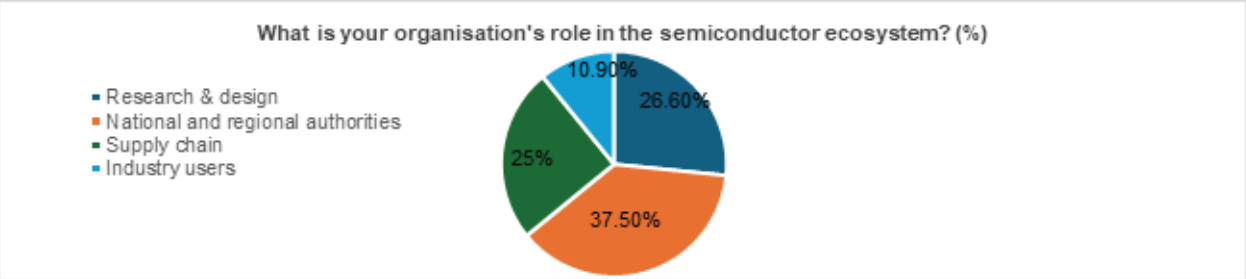


Figure 8. Breakdown of respondent profiles by stakeholder category

Source: Surveys with EU Chips Act stakeholders (research and design organisations N=17, supply chain organisations N=16, industry users N=7, national authorities N=24), conducted by PPMI, October–November 2024).

6.1. Effectiveness

National authorities consistently reported the highest levels of positive effects (75% across most dimensions), which suggests that policy-level coordination benefits are materialising more rapidly than operational effects. RTOs reported the lowest levels of positive effects (35-41%), with 35% reporting 'no effects' on several dimensions. This gap warrants further investigation to understand barriers to research organisation engagement.

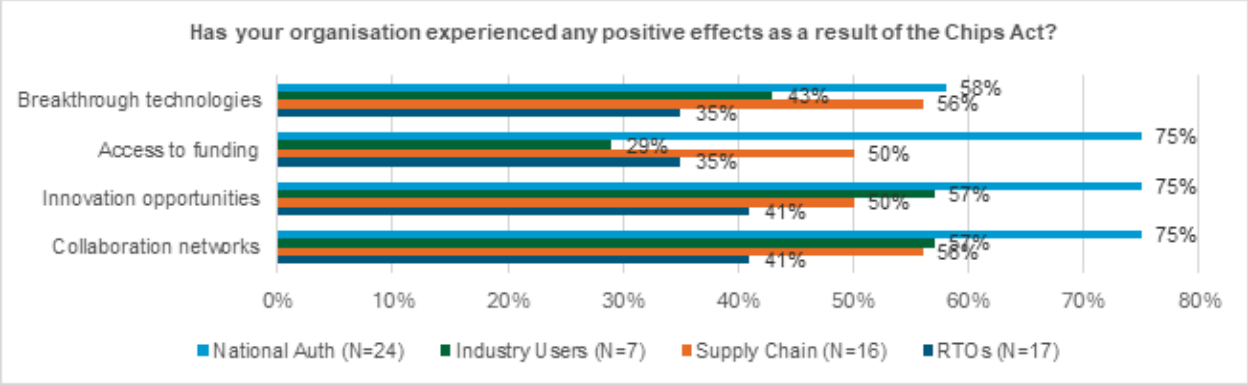


Figure 9. Positive effects experienced (% reporting moderate to very significant effects)

Source: Surveys with EU Chips Act stakeholders (research and design organisations N=17, supply chain organisations N=16, industry users N=7, national authorities N=24), conducted by PPMI, October–November 2024).

Progress assessments varied significantly across the three pillars. Pillar 1 (research-industry link) received the strongest positive assessment, with 58% of National Authorities (14/24) agreeing progress has been made. Pillar 2 (investment and capacity) showed more mixed results (42% agreeing, 10/24), while Pillar 3 (supply chain resilience) received the lowest positive assessment (17% agreeing, 4/24) with 25% (6/24) indicating it was too early to tell. These findings suggest that Pillar 3 mechanisms may require more time to demonstrate observable effects on supply chain resilience.

6.2. Efficiency

National authority responses indicate that **46% (11/24) have encountered significant implementation challenges**, whilst 21% (5/24) reported it was too early to tell and 13% (3/24) indicated no significant challenges. Among those reporting challenges, the most frequently cited were insufficient national co-funding capacity, competing national priorities, and complex EU-national coordination.

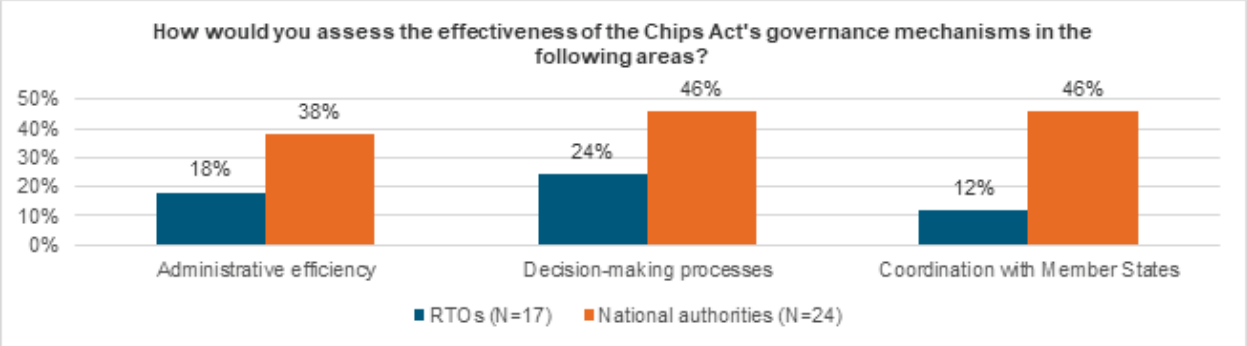


Figure 10. Governance effectiveness assessments (% rating somewhat effective to very effective)

Source: Surveys with EU Chips Act stakeholders (research and design organisations N=17, supply chain organisations N=16, industry users N=7, national authorities N=24), conducted by PPMI, October–November 2024).

A **notable divergence exists between stakeholder groups**: National Authorities assessed governance mechanisms more favourably (38-46% effective) compared to RTOs (12-24%). RTOs showed higher rates of 'very ineffective' assessments (18-29%), particularly for administrative

efficiency and Member State coordination, which suggests that research organisations face more acute administrative frictions when engaging with Chips Act instruments.

Among RTOs, 47% (8/17) reported facing significant barriers to commercialisation. **Insufficient risk capital and lack of industry partnerships were the most frequently cited barriers**, consistent with the broader concern about the lab-to-fab gap identified in the relevance section.

6.3. Coherence

Regarding external coherence with national strategies, responses from **national authorities indicated mixed alignment**. Of 24 respondents, 33% reported the Chips Act was 'fully aligned' with their national semiconductor strategy, 21% 'somewhat aligned', and 21% indicated no national strategy exists. **The importance of addressing the misalignment between research priorities and market needs was recognised across all groups**, though with varying intensity. Survey respondents, particularly national authorities, further noted that coordination and investment across the EU, national and regional levels was challenging and more fragmented.

6.4. EU added value

Strengthening the EU's global position received the highest agreement (68%, 28/41), followed by pooling resources for greater scale (66%, 27/41). This suggests that stakeholders recognise the value of collective European action in the globally competitive semiconductor landscape. However, responses were not uniformly positive: 18-29% of RTOs expressed strong disagreement that these benefits were materialising, indicating a cohort of research organisations that have not yet experienced the expected EU-level synergies.

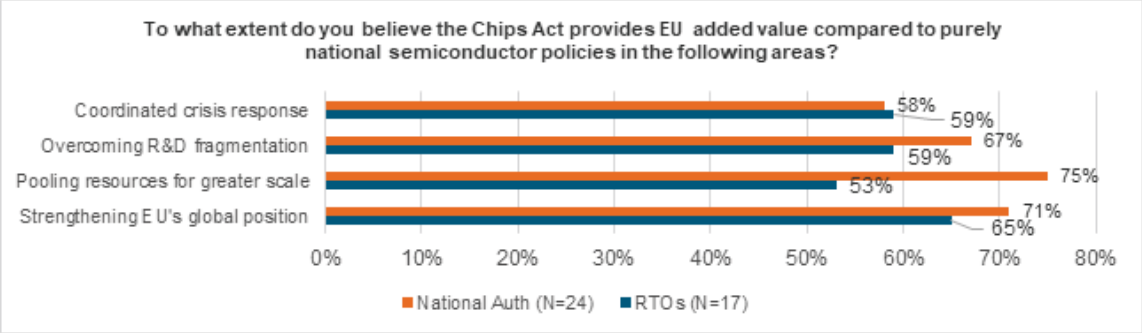


Figure 11. EU added value perceptions (% agreeing or strongly agreeing)
Source: Surveys with EU Chips Act stakeholders (research and design organisations N=17 and national authorities N=24), conducted by PPMI, October–November 2024).

National Authorities consistently assessed EU added value more positively than RTOs, **particularly for pooling resources (75% vs 53%)**. This 22-percentage point gap suggests that the benefits of resource pooling may be more visible at the policy coordination level than at the research operational level. The relatively similar ratings for coordinated crisis response (59% for RTOs vs 58% for National Authorities) indicate that crisis preparedness benefits are perceived more evenly across stakeholder types.

6.5. Relevance

The survey results demonstrate strong and consistent support for continued EU-level action across all stakeholder groups. Agreement rates on the need for EU-level coordination ranged from 75% (monitoring and crisis response) to 86% (investment and manufacturing capacity),

indicating broad endorsement of the subsidiarity rationale underpinning the Act. Supply chain stakeholders demonstrated the strongest support for EU-level coordination in R&D (100%, 16/16) and investment (94%, 15/16), reflecting their direct dependence on ecosystem-wide infrastructure.

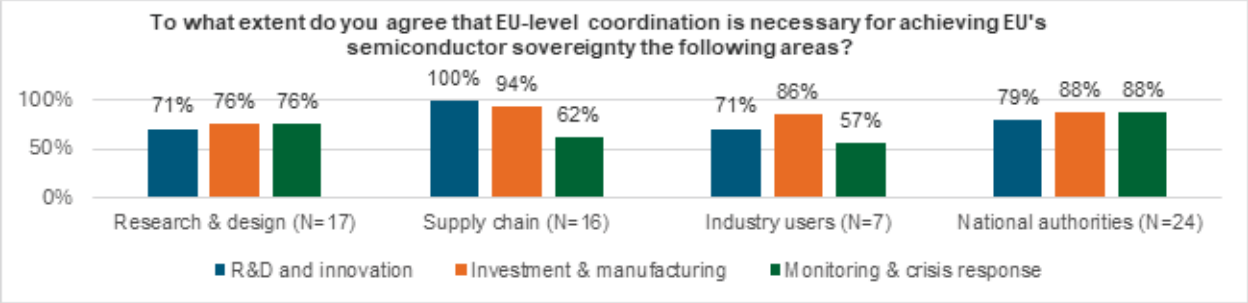


Figure 12. Need for EU-level coordination by policy area (% agreeing or strongly agreeing)
Source: Surveys with EU Chips Act stakeholders (research and design organisations N=17, supply chain organisations N=16, industry users N=7, national authorities N=24), conducted by PPMI, October-November 2024.

However, support for monitoring coordination was comparatively lower among supply chain (62%) and industry users (57%), possibly reflecting concerns about reporting obligations. National authorities showed highest support for monitoring coordination (88%), consistent with their role in crisis response mechanisms and their greater familiarity with Pillar 3 instruments.

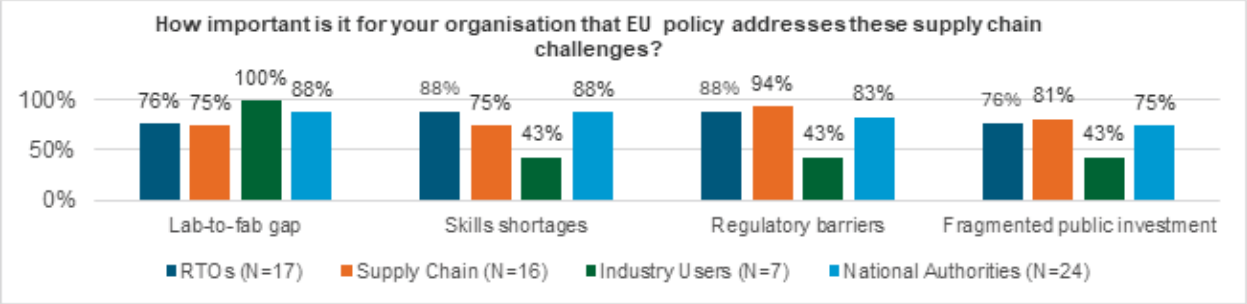


Figure 13. Importance of addressing key challenges (% rating important or very important)
Source: Surveys with EU Chips Act stakeholders (research and design organisations N=17, supply chain organisations N=16, industry users N=7, national authorities N=24), conducted by PPMI, October-November 2024.

Regulatory barriers emerged as the highest-rated challenge overall, with near-unanimous concern from supply chain stakeholders (94%, 15/16). The lab-to-fab gap was unanimously prioritised by industry users (100%, 7/7), whilst RTOs and National Authorities prioritised skills shortages (88% each). These differentiated priorities reflect the varying operational contexts and immediate concerns of each stakeholder group.

6.6. Prospective

Simplified and faster state aid emerged as the top priority (58% ranking first), with particularly strong support from National Authorities (83% ranking first), consistent with their direct experience of notification and approval processes. More direct EU-level funding ranked second (51% ranking first), with strongest support from industry users (80%). Large-scale skills development was also highly prioritised (44% ranking first).

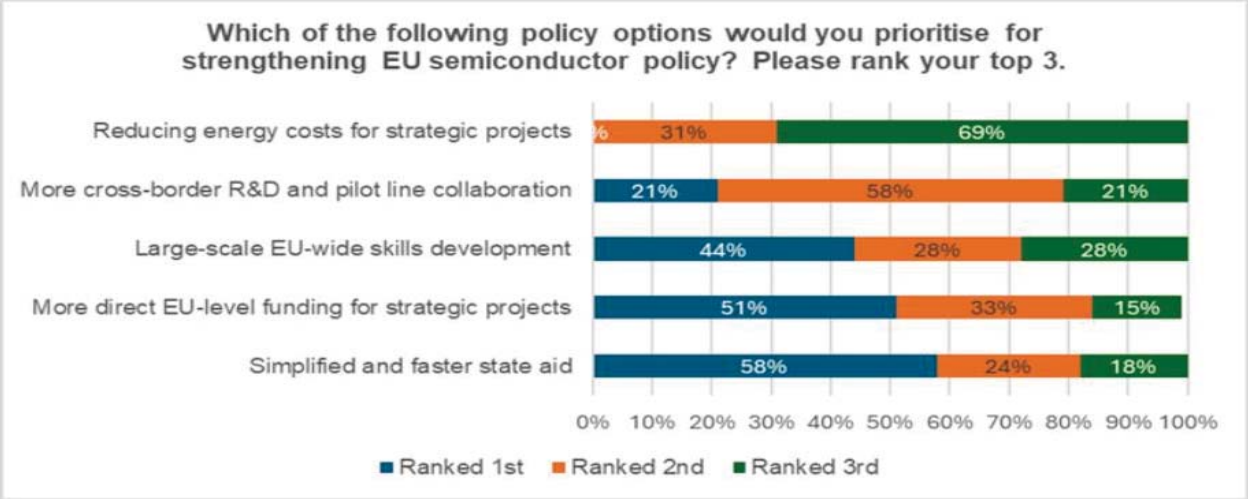


Figure 14. Policy option priorities (% of responses ranking option in top 3)

Source: Surveys with EU Chips Act stakeholders (research and design organisations N=17, supply chain organisations N=16, industry users N=7, national authorities N=24), conducted by PPMI, October–November 2024).

Regarding ambition levels for cutting-edge manufacturing, National Authorities showed diverse views: 29% favoured establishing at least one high-volume leading-edge fab, 21% preferred focusing on pilot lines, 13% supported building multiple leading-edge fabs, and 13% advocated focusing on R&D without new commercial fabs.

7. SUMMARISED RESULTS OF THE EXPERT INTERVIEWS

The interviews were conducted using a semi-structured interview format. The interview guide was developed specifically for this evaluation and was directly aligned with the objectives, pillars, and policy instruments of the Chips Act. This ensured that all discussions systematically addressed themes relevant to the Act while allowing respondents the flexibility to elaborate on issues they considered most significant.

Each interview was fully transcribed and subsequently examined through a structured qualitative analysis process. The analysis focused on identifying recurring themes, points of convergence and divergence, and insights relevant to the evaluation questions. Artificial intelligence tools were used to support the organisation and comparison of the interview material, helping to cluster related content and reveal patterns across stakeholder groups. These AI-assisted steps complemented the manual review of transcripts and improved the consistency and transparency of the analytical process. The material was reviewed iteratively to ensure coherence and completeness.

Respondents represented a broad, strategically selected spectrum of organisations involved in or affected by the European semiconductor ecosystem. The sample included actors from European institutions, industry associations, manufacturing companies, investors, research and innovation bodies, and supply-chain specialists (**Table 2**). This diversity ensured the inclusion of both supply-side and demand-side viewpoints, as well as short-term operational and long-term strategic considerations. The resulting dataset reflects a balanced mix of technical, economic, policy, and strategic insights relevant to assessing the relevance and implementation of the Chips Act.

Table 2. Interview coding[1]

Stakeholder group	Code	Stakeholder group	Code
Public Investor	1	Industry (EMS & PCB)	8

EU Financial Institution	2	Industry Association	9
Private Investor	3	EU Agency / End-User (Space)	10
EU Policymaker (European Commission)	4	Industry (Semiconductor Manufacturer / IDM)	11
Industry Association	5	Policy officer	12
EU Policymaker (European Commission)	6	Trade union	13
EU Implementation Body / Public-Private Partnership	7	Industry Association	14

7.1. Effectiveness

Interviewed stakeholders widely reported that Pillar I instruments had been successful. The EIC's €300M Chips Fund mandate was described as effective in building a portfolio of deep-tech start-ups and in crowding in private investment by validating risky companies. Stakeholders characterised the Design Platform as a standout success for fabless start-ups, offering easier and cheaper access to design tools. Research-oriented interviewees agreed that Europe remained a global research hub, with IPCEIs and pilot lines supporting innovation along the value chain. First-of-a-kind manufacturing projects and cooperation models such as the TSMC Dresden project (ESMC) were viewed as promising steps towards greater sovereignty and more coordinated European action.

However, perceived **effectiveness dropped sharply at the transition from research to industrialisation and scaling,** creating a pronounced "valley of death" between early-stage innovation and commercialisation. Access to and involvement in pilot lines for start-ups and SMEs was described as unclear and costly and was perceived as a missed opportunity, particularly for equipment and hardware start-ups that needed real testing environments. Stakeholders generally judged Pillar II to be less effective due to weak coordination, the dominance of national budgets (leading to concentration in large Member States), and a lack of clear metrics. They argued that the system mainly supported incremental, rather than disruptive, innovation and that project timelines (3–4 years) were too short for breakthrough technologies that might require seven years or more.

Interviewees identified the investment and market environment as key structural constraints. They claimed that without significantly larger funding, Europe could not expect meaningful independence in advanced CMOS nodes or a competitive position in AI-related hardware. Limited VC and capital markets, the lack of advanced fabs, and the absence of strong European end-users in key sectors such as consumer electronics and AI hardware were said to push start-ups to relocate or raise funds in the US, where both public and private capital moved faster and at much larger scale. While the Chips Act was considered helpful at the seed and early stages, stakeholders argued that it did not yet solve the "valley of death" for follow-on financing. SME representatives pointed out complex and demanding procedures that made it practically impossible for them to benefit, and some interviewees felt that the Chips Act had not made Europe more attractive for semiconductor start-ups.

Views on supply-chain resilience and governance effects were described as mixed. Interviewees acknowledged that, on paper, the Act had improved sovereignty and triggered new projects, but they also emphasised that Europe still relied heavily on Asian, especially Taiwanese, suppliers and that current investment volumes were viewed as "cosmetic" compared to Asia's.

Stakeholders involved in Pillar III reported that data collection had shown voluntary mechanisms could work technically, but effectiveness had been undermined because the information gathered was not meaningfully used, which they said damaged trust and future cooperation.

Finally, some stakeholders argued that supply-side support alone was insufficient. In their view, **effectiveness required stronger demand-side measures** (e.g., "buy European" clauses in public procurement for initiatives such as the Pilot Lines, AI Factories, and EuroHPC) to counter the tendency for purchases to come predominantly from US or Japanese suppliers.

7.2. Efficiency

Stakeholders reported that the Chips Act was seen as strategically important but at times operationally challenging. They generally argued that some instruments were not well aligned with the capital intensity and timelines of semiconductors, and that governance across funding streams and administrative levels could be difficult to navigate. Several companies reported duplicated procedures for the same project, which increased costs and slowed decisions, while smaller players often relied on consultants to manage similar application requirements.

Interviewees pointed to the design and sequencing of funding instruments as a key issue. Existing innovation and scale-up tools were described as insufficiently tailored to the cost structure of chip development. **Grants were often too small for major steps such as a tape-out, while the next-tier instruments required higher technological maturity than many firms had reached**. This contributed to a "valley of death" between programmes and, in scale-up support, to difficulties meeting requirements for significant prior investment commitments. Stakeholders argued that more flexible ticket sizes, smoother transitions across technology readiness levels and clearer rules for co-investment with trusted non-EU partners would improve alignment with sector needs.

Procedures were frequently described as slower and more burdensome than in competing regions. Validation and approval for first-of-a-kind investments could take many months, and the gap between political announcements and the first calls was occasionally long. Interviewees also noted repeated documentation requests, digital platforms that did not always function as intended and limited administrative capacity. Stakeholders also highlighted limited transparency on application status, criteria and decision-making, which made planning difficult. They noted the absence of an EU-level overview of firms and investment activity, reducing visibility for effective policy steering. These experiences indicated, in their view, room for simplification, clearer timelines and more consistent once-only submission practices.

Finally, several stakeholders commented that the Act had been assembled under time pressure with limited early industry input, resulting in instruments layered onto administrative systems not fully adapted to semiconductor needs. Decisions to fund many parallel technology areas, such as in quantum, were viewed as spreading resources thinly. Interviewees also noted that for the most financially robust global semiconductor firms, bottlenecks related less to subsidies than to broader framework conditions such as predictable permitting, skilled labour availability and competitive operating costs.

7.3. Coherence

Stakeholders generally indicated that coherence had been a recurring challenge in the implementation of the Chips Act, both within the EU policy system and across Member States. They noted that internal coherence between innovation funding instruments and top-down policy design had sometimes been limited. Bottom-up work with start-ups was seen as insufficiently

connected to the design or adjustment of large-scale instruments. Interviewees reported that operational services collected valuable insights from start-ups, but these were not always fed back into policymaking.

Stakeholders also observed that coherence across instruments and programmes had been uneven. Although synergies in principle existed between frontier research, proof-of-concept funding, transition mechanisms, and later-stage innovation support, interviewees suggested that these links tended to depend on individual initiative rather than structured coordination. **The intended pathway from research to pilot lines and then to production was not widely perceived as an integrated continuum**. The first pillar was viewed as largely research-driven, with limited mechanisms to support the translation of results into industrial innovation or manufacturing scale-up.

Interviewees further noted that coordination across Member States had sometimes been fragmented. **National and regional semiconductor initiatives were often developed independently**, without a clear framework to bring them together into a more strategic European approach. Governance structures intended to facilitate coordination were described as offering limited visibility into other countries' activities, which stakeholders felt could hinder mutual learning and risk duplication. According to several interviewees, parts of the value chain, such as electronic manufacturing services and PCB industries, were receiving comparatively less attention.

Stakeholders also pointed to areas where **legal and policy scope had been unclear** or not fully aligned with other regulatory instruments. Definitions such as what constituted first-of-a-kind were considered difficult to interpret, and some critical segments (e.g., materials suppliers, testing, metrology equipment) were not always clearly addressed. Interviewees also noted potential tensions with other frameworks, including foreign subsidy rules. Environmental and energy-efficiency considerations, prominent in State aid rules, were not seen as strongly integrated into the Chips Act.

Finally, stakeholders described **data collection and monitoring as an area where coherence could be strengthened**. Multiple Commission services, Member States, and private actors carried out parallel semiconductor-related data exercises, sometimes overlapping and targeting the same firms. Interviewees reported a lack of a shared framework or one-stop-shop, which they felt increased administrative burden and reduced transparency. They also saw limited evidence that collected data was systematically pooled or used to support coordinated policy development, noting that effective monitoring, particularly under the third pillar, would require both legal provisions and sufficient institutional capacity.

7.4. EU added value

Stakeholders generally indicated that European funding instruments had played a crucial role for deep-tech start-ups in semiconductors and related fields. Many interviewees believed that companies supported through Union programmes would have struggled to survive on national or private funding alone, especially at very early and capital-intensive stages. European-level public investment, combined with national support, was described as "genuinely additional", enabling rounds and growth that many Member States could not have achieved independently.

Interviewees noted important signalling and ecosystem effects too. The Chips Act was seen as demonstrating institutional commitment, helping build investor trust and a more visible European semiconductor community. Events and portfolio efforts were viewed as contributing to **"a**

recognisable European semiconductor ecosystem" rather than a set of disconnected national efforts.

On regulation and coordination, stakeholders argued that the EU offered value that Member States could not replicate alone. The state aid framework linked to the Chips Act and IPCEI experience was perceived as creating "a common playing field", giving Europe clearer rules for competing in global subsidy environments, even though most investment came from national budgets.

The joint undertaking structure was viewed as another source of added value through its matching-fund model. Interviewees saw this "money-doubling mechanism" that encouraged national mobilisation. At the same time, they noted that the Act continued to rely heavily on national fiscal capacity, limiting the extent to which EU-level funding could reduce disparities between larger and smaller Member States. Stakeholders also highlighted added value in market intelligence. They reported that only an EU-level effort could generate comprehensive cross-border data on semiconductor use and revenues, which companies valued as a neutral reference point. Yet, they stressed that this advantage depended on such information being visibly used in policy design; otherwise, the case for centralised monitoring weakened.

Interviewees also mentioned several limits. Slow funding roll-out, shaped by the Multiannual Financial Framework and procedural complexity, was perceived as reducing the Act's competitiveness relative to faster support schemes elsewhere. Stakeholders additionally noted that full semiconductor autonomy was unrealistic. **They saw the EU's most feasible contribution as reinforcing existing industrial strengths, attracting inward investment, and supporting competitive European firms within global supply chains** rather than pursuing full localisation.

7.5. Relevance

Stakeholders indicated that the European Chips Act addressed several important needs within Europe's semiconductor ecosystem, though assessments of its overall relevance varied. Many noted that its initial focus did not fully reflect Europe's structural strengths, long-term vulnerabilities, or the realities of global markets. While the Act provided a framework for investment and technological development**, interviewees stressed the need to refine priorities, strengthen demand-side integration, and better align with industrial capabilities and geopolitical constraints**.

Several stakeholders observed that early instruments overlooked **emerging needs, particularly the strategic roles of fabless design companies.** End-user industries and parts of the supply chain, such as electronic manufacturing services, printed circuit boards, packaging, testing, metrology tools, and raw materials, were not adequately considered, creating uncertainty for investors and leaving European strengths underexploited.

A recurring theme was **the need to focus on areas of competitive advantage**, including lithography and other production equipment, photonics, power electronics, sensors, and imaging technologies. Interviewees suggested that political emphasis on the most advanced manufacturing nodes was unlikely to be realistic without significantly larger budgets. They recommended building on existing ecosystems and concentrating on niches where Europe can lead. Long-term relevance was also linked to AI hardware and related technologies, where innovations risked remaining underutilised without strategies ensuring domestic deployment. Ignoring these areas could leave Europe economically marginalised.

Stakeholders highlighted that monitoring and intelligence functions required clearer design. Effective data collection needed to be tied to specific policy purposes, with aggregated intelligence shared back to contributors to inform assessments and foster long-term cooperation. Interviewees emphasised the importance of integrating industrial policy across the full electronics value chain. Declines in European printed circuit board manufacturing, for instance, were seen as threatening commercial sectors as well as space and defence autonomy, underscoring the need for sustained support to maintain critical suppliers.

7.6. Prospective

Interviewees suggested that the future of **the Chips Act would require a strategic refocus**. Some argued that Europe should concentrate on its real strengths, such as equipment, photonics, sensors, power electronics, and specific AI-related hardware, while providing better support for fabless design and the full electronics value chain. Monitoring and data collection were expected to evolve into a more purposeful intelligence function, with information clearly linked to policy choices, shared with contributors, and used to guide priorities and risk assessments.

Looking ahead, stakeholders called for more flexible and faster funding tools to bridge the "valley of death" from research to industrial scale-up, alongside simpler procedures and clearer access for start-ups and SMEs. They also highlighted the need for smoother pathways across technology readiness levels, and clearer rules for co-investment with trusted non-EU partners. At the same time, they anticipated a stronger EU role in coordinating national initiatives, aligning the Chips Act with other regulatory frameworks, and complementing supply-side subsidies with demand-side measures such as strategic public procurement.

A distinctive perspective emphasised that before pursuing ambitious expansion, Europe should secure existing facilities, as remaining backend capacity faces significant pressure. Recommendations included integrating social conditions (job creation quality, health and safety standards, collective bargaining requirements) and environmental criteria (PFAS substitution, renewable energy incentives) to position Europe as a leader in sustainable semiconductor manufacturing.

Stakeholders emphasised that **Europe should not aim for full semiconductor autonomy but a realistic position**: reinforcing existing strengths, attracting foreign investment, supporting competitive European application companies, and increasing agile EU-level funding to remain relevant in AI chips and advanced computing.

8. SUMMARISED RESULTS OF THE WORKSHOPS

Sixteen thematic evaluation workshops (**Table 3**) were conducted between September and December 2025 with the participation of diverse stakeholders across the European semiconductor ecosystem. Structured summary reports were developed for each of the workshops, including sections 1) Summary of Stakeholders' Perspectives; 2) Key messages per evaluation criteria; and 3) Prospective Reflections for Chips Act 2.0. These summaries have been analysed and compared across the workshops.

Table 3. Workshop coding

Workshop title	Code	Workshop title	Code
Health	1	Automotives	10
Telecoms	2	PCB & EMS	11

RTOs & Academia	3	SMEs & Start-ups	12
ESRA & Regional clusters	4	Industrial Alliance on Processors and Semiconductor Technologies Plenary	13
Technology, Innovation and Skills	5	PAB Workshop	14
Defence & Space	6	PMB Workshop	15
Supply chains	7	Semiconductor equipment and its components	16
Advanced Chips Design for Data Centres	8	Stakeholder's validation workshop	17
Materials	9		

This diverse participation ensured comprehensive coverage of the semiconductor value chain and other stakeholders. They included:

- **Industry representatives:** Major telecoms and industrial equipment manufacturers (Ericsson, Nokia, Philips, Siemens), manufacturer of semiconductors and equipment (ASM, ASML, ST Microelectronics, Cologne Chip), fabless companies, design service providers and other firms (e.g., cloud providers).
- **Regional and institutional actors:** Regional authorities from Saxony, Catalonia, and Finland; industrial clusters (Silicon Europe, MESAP); competence centres; and implementation practitioners managing major projects like Saxony's TSMC facility.
- **Research and academic organisations:** Research Technology Organisations (RTOs) including IMEC, Fraunhofer, CSEM, and CRT/LETI; universities (TU Graz, University of Delft); and academic consortia involved in pilot lines and research projects.
- **Supporting ecosystem:** Organisations dealing with education (European Chips Skills Academy, EIT Digital, aCCCess), material suppliers, manufacturing technology suppliers, investors, and national talent initiatives.
- **European Commission**: Representatives from DG CNECT, DG DEFIS, DG SANTE, DG RTD, and the Joint Research Centre participated to provide policy context and gather feedback.

8.1. Effectiveness

Across the workshops, stakeholders recognised that the Chips Act had **mobilised significant investment and accelerated progress in design, pilot-line development and early manufacturing capacity**, yet they also emphasised that **critical structural gaps persisted** across the value chain. Many noted that Europe still depended heavily on non-EU suppliers, and recent disruptions in the medical, industrial and telecoms sectors illustrated the **ongoing vulnerability of supply chains**. Participants also warned that component obsolescence, particularly of specialised FPGAs, posed rising risks for sectors requiring long validation cycles.

Stakeholders broadly agreed that **Europe lacked viable high-performance manufacturing options**, especially for AI, HPC and advanced automotive applications. With nearly all cloud-grade chips sourced from Asia, concentration risks remained extremely high. Several workshops highlighted that the absence of a sufficiently large and coordinated European demand base limited incentives for large-scale investment in cutting-edge capacity.

SME access emerged as a consistent concern. While many welcomed the ambition of pilot lines, design platforms and competence centres, stakeholders reported barriers related to cost, administrative complexity, and timing. Pilot-line access was still unaffordable for early-stage innovators, the design platform remained oriented toward firms already active in microelectronics, and in several Member States competence centres had only recently become operational, limiting early benefits for SMEs and start-ups. A lack of effectiveness was also noted by equipment

manufacturers who pointed out that their business model would require higher R&D support, not investment incentives.

A cross-cutting theme was the lack of demand aggregation, especially in sectors relying on customised or low-volume chips (health technologies, telecoms, data centres, automotive, PCB/EMS). Participants described this as a fundamental structural weakness: fragmented demand prevented economies of scale and slowed the transition from "lab to fab", limiting Europe's ability to industrialise emerging technologies.

Workshops also noted that **skills shortages remained a major bottleneck**, with current initiatives seen as insufficient relative to projected shortages of 70,000-80,000 professionals. Acute gaps were reported in analogue design, system architecture, advanced packaging and testing, profiles essential for scaling many of the technologies supported under the Act.

Finally, **stakeholders stressed that back-end and supporting ecosystem capabilities**, notably packaging, testing, materials, and PCBs/EMS, **remained underdeveloped and insufficiently addressed** by the Chips Act. Several workshops argued that progress in front-end capacity would not translate into ecosystem resilience unless downstream and adjacent segments were strengthened in parallel, particularly for strategic sectors such as defence, automotive and industrial automation.

8.2. Efficiency

Across the workshops, stakeholders emphasised that suggested that while the Chips Act created valuable instruments, **administrative processes were at times perceived as slow, complex, and misaligned with industry timelines**. Participants highlighted long funding cycles, multi-stage application procedures, and lengthy State-aid approvals as recurring sources of inefficiency. Timing mismatches were frequently cited – industry projects often required multi-year lead times, while some public-funding deadlines operated on six-month windows, creating uncertainty and deterring participation. Stakeholders across sectors therefore prioritised reduced administrative burden, clearer guidance, and streamlined multi-instrument processes as key conditions for improving efficiency.

Another broad theme was **fragmentation across parallel EU and national initiatives**. Workshops pointed to multiple programmes operating with limited coordination, leading to duplication, inconsistent cost models, and unclear complementarities. Participants expressed a preference for a more unified and predictable framework, with several arguing that the Chips Act would function more efficiently if structured as a **single, coordinated programme with clearer interfaces between instruments** rather than a collection of separately governed schemes. Gaps in day-to-day coordination between entities offering similar expertise—such as competence centres, research infrastructures, and national innovation agencies—were also reported as reducing the overall efficiency of investment.

Some workshops raised concerns regarding the **tension between efficiency and geographical cohesion**. While many stakeholders acknowledged that semiconductor manufacturing benefits from concentration in strong industrial clusters, regional authorities emphasised that they played a critical role in training talent, supporting SMEs, and anchoring local innovation ecosystems. Participants noted that overly centralised investment risks overlooking regional capabilities and slowing implementation, underscoring the need for better multilevel coordination rather than simply broader dispersion of funds.

Mobilising **private capital, particularly European venture capital, was repeatedly identified as a structural bottleneck**. Stakeholders argued that despite the availability of public funding, many semiconductor and deep-tech companies faced difficulties raising private investment at scale. Pension-fund rules and conservative investment mandates were frequently mentioned constraints, alongside the limited depth of European VC markets compared to the United States. As a result, participants stressed that the binding constraint for scale-up was often not public-funding volume but insufficient private-capital mobilisation, which reduced Europe's ability to translate R&I outputs into industrial impact.

8.3. Coherence

Workshop discussions suggested that stakeholders saw the main coherence gap in the Chips Act's **imbalance between its strong emphasis on manufacturing capacity and comparatively weaker support for design ecosystems, downstream integration, and demand-creation mechanisms**. Participants across sectors argued that these elements needed to evolve together for the strategy to be coherent, yet this alignment had not fully materialised. Although seen a setting a great foundation, intended synergies across the three pillars were seen as only partially realised, due to fragmented funding streams, misaligned timelines, and weak operational linkage between Pillars I and II, especially in the transition from pilot-line validation to industrial deployment.

A cross-cutting theme from multiple workshops was the scale mismatch between European demand and the investment requirements of semiconductor manufacturing. Even where European technology alternatives existed, participants noted that providers struggled to achieve cost competitiveness because the scale of demand was insufficient. Sectors such as telecommunications, automotive, industrial automation, and medical technologies individually lacked the volume to justify major fabs, and participants across several workshops stressed that scale cannot be reached without coordinated, aggregated demand. This structural constraint was linked to cases where European components were technically available but not adopted widely due to higher cost and fragmented purchasing.

Stakeholders also pointed to regulatory and policy incoherence affecting implementation. Tensions emerged between ambitions for greater use of European technology and EU state-aid and procurement rules that restricted preferential treatment. Materials and equipment suppliers noted path dependencies that made it difficult for European pilot lines to adopt EU-produced chemicals or tools, as certification systems were aligned with non-EU inputs. Emerging environmental regulations, particularly PFAS restrictions, were also described as misaligned with Europe's manufacturing ambitions, given the absence of economically viable substitutes for certain fabrication processes.

Participants highlighted fragmentation across EU instruments, including Chips JU, Horizon Europe, EIC, IPCEIs, and InvestEU. While individually valuable, these initiatives were perceived as lacking a unifying architecture, creating duplication of administrative effort and insufficiently coordinated investment logic. IPCEIs were viewed as coherent with the Act at a strategic level but still favouring large incumbents, with limited mechanisms to ensure collaboration with smaller innovators. Some challenges were also noted as stemming from **temporal misalignment**. Stakeholders noted that multi-year project cycles and programme start dates were out of sync with industry time-to-market pressures, with initiatives planned for 2026 already perceived as too late for emerging technological windows. Similarly, semiconductor skills pipelines required decade-long investment horizons, yet relevant programmes operated on shorter budgetary cycles, limiting structural impact.

8.4. EU added value

Across the workshops, participants broadly agreed that **EU-level coordination was essential** for achieving outcomes that individual Member States could not deliver alone. Stakeholders highlighted that only the EU could coordinate dispersed national strategies, facilitate cross-border collaboration, and create economies of scale needed for shared infrastructures such as pilot lines, competence centres, and the European Chips Design Platform. If implemented effectively, these platforms were seen as providing globally distinctive EU added value, particularly by enabling SMEs and start-ups to access design tools and advanced prototyping environments that no single country could sustain.

EU-level action was also viewed as necessary for advancing strategic autonomy, not through full self-sufficiency, which participants widely considered unrealistic, but **by reinforcing Europe's strongest technological niches**. Workshops consistently pointed to European advantages in areas such as manufacturing equipment including advanced packaging tools and lithography, to photonics, silicon photonics, power electronics, sensors, and energy-efficient design. Participants emphasised that strengthening these capabilities, combined with targeted international partnerships, could create mutual dependencies where global supply chains rely on European technologies. This was seen as an EU-level task, as no Member State could negotiate such strategic partnerships alone.

Stakeholders also noted EU added value in **coordinating shared investments, particularly through Chips JU and IPCEI mechanisms**. Participants observed that these programmes enabled joint funding and collaboration across borders, giving smaller Member States access to research infrastructures and reducing duplication of national efforts. For many SMEs, universities, and RTOs, the EU framework offered opportunities that national schemes could not provide.

However, workshops also highlighted several areas where EU added value remained largely unrealised. Fragmented decision-making and parallel national initiatives continued to dilute Europe's collective leverage. Participants stressed that while Europe possessed substantial potential demand, the absence of EU mechanisms for demand aggregation prevented this from translating into coordinated procurement or industrial scale. In sectors such as health, telecommunications, and data centres, regulatory fragmentation, such as the lack of a unified European counterpart to the FDA, pushed innovators to seek approval in the US first, weakening Europe's bargaining position and market cohesion.

Stakeholders also viewed **labour mobility and talent attraction** as a major unrealised opportunity for EU added value. Despite widespread skills shortages, there was no unified European framework for cross-border mobility, qualification recognition, or work permits for international talent. Participants argued that only EU-level action could meaningfully reduce these barriers and support semiconductor workforce development at the scale required.

8.5. Relevance

Across the workshops, **stakeholders broadly agreed that the Chips Act addressed several of the EU's most pressing semiconductor needs,** particularly the scarcity of mature-node manufacturing capacity, the fragmentation of design infrastructure, and the lack of coordinated investment in critical technologies. Participants consistently emphasised that Europe's most strategically important sectors, including automotive, health, defence, space, and telecommunications, continued to rely predominantly on mature and specialised technologies, making the Act's focus on securing and expanding such capacity highly relevant. Defence and

space relied on radiation-tolerant 7-12 nm nodes; automotive applications required long-lifecycle components; and healthcare depended on parts requiring multi-decade availability, which standard global semiconductor lifecycles do not support. **Participants therefore viewed the Chips Act as filling a gap that individual Member States could not address alone.**

At the same time, workshops highlighted that several structural needs remained only partially reflected in the Act's design, especially as new vulnerabilities were arising. Many sectors stressed that **relevance depended not only on front-end capacity** but on strengthening packaging, testing, assembly, and PCB/EMS capabilities, which were described as Europe's most acute bottlenecks. Stakeholders across telecoms, automotive, and materials workshops argued that without these back-end and integration capabilities, the Chips Act risked reinforcing Europe's dependence on non-EU suppliers even as wafer-fabrication capacity expanded.

Another recurring theme concerned the **Lab-to-Fab gap**, **which stakeholders described as not merely an implementation issue but a design-relevance challenge.** Pilot lines were judged valuable for TRL 5-6 development but insufficiently connected to pathways for high-volume manufacturing. Universities and RTOs pointed to wafer-size mismatches, limited access to industrial equipment, and weak technology-transfer channels, all of which limited the relevance of pilot-line investments for early-stage innovation ecosystems.

SMEs repeatedly noted that the Chips Act's architecture was not fully aligned with their needs, despite the central role SMEs play in design, IP development, and manufacturing technology supply. Barriers included cost-prohibitive pilot-line access, consortium structures that favoured incumbents, and an absence of mechanisms to test equipment within industrial fabrication environments. For fabless companies and design start-ups, the Act was seen as insufficiently tailored to address Europe's limited availability of EDA tools, high design costs, and lack of early-stage risk capital – factors that were identified as core relevance gaps.

Workshops also underscored that Europe's design ecosystem and architectural IP capabilities represented a more fundamental sovereignty constraint than manufacturing alone. Stakeholders emphasised that relevance would depend on strengthening software-heavy chip design, system integration, and access to state-of-the-art EDA tools. Telecommunications and data-centre actors, for instance, stressed that controlling architectural design flows and system-level integration was just as important as building fabs, yet this dimension was underrepresented in the Chips Act's current scope.

Finally, **skills needs emerged as a cross-cutting relevance issue**. Participants across design, R&I, manufacturing, packaging, automotive, telecoms, and materials workshops reported shortages in applied engineering, analogue design, advanced packaging, and system integration skills. Some stakeholders argued the Chips Act's skills measures were insufficiently aligned with where shortages were most acute and did not yet match the pace of technological change in AI, chiplet architectures, and power electronics.

8.6. Prospective

Across the workshops, stakeholders underscored that any future iteration of the Chips Act should move beyond a predominantly supply-driven focus toward a more systemic, integrated, value-chain approach. Participants emphasised the need for a framework that supports not only front-end manufacturing but also design ecosystems, advanced packaging, testing and system integration, which remain essential bottlenecks for Europe's competitiveness.

Stakeholders also pointed to a series of structural reforms. A recurrent theme was the need for dedicated mechanisms for SMEs and fabless companies, including accessible pilot-line pathways, equipment-testing environments, lighter consortium requirements, and dedicated equipment development infrastructure with confidentiality protections, R&D tax credits and TRL 7-9 fast-track funding, and equipment sector representation in governance structures.

Another widely supported proposal was the introduction of demand-aggregation frameworks, enabling coordinated procurement across high-impact sectors such as defence, telecommunications, automotive, health and space. Participants suggested that publicly funded projects could embed demand-side instruments to strengthen the position of European suppliers. They also stressed the need for faster, more flexible funding instruments, streamlined administration, and longer funding horizons aligned with the 10–15 year timescales typical of semiconductor innovation. Predictable, multi-year funding was repeatedly described as critical for enabling companies to plan ahead and scale confidently.

Beyond procedural reforms, workshops identified several new technological and strategic priorities for a next phase of the Act. These included targeted support for advanced manufacturing capabilities, such as sub-2 nm processes and 3D/heterogeneous packaging, to reduce reliance on Taiwan and respond to the rapid rise in AI-driven demand. At the same time, participants stressed that expanding leading-edge capacity should not come at the expense of mature nodes, which remain indispensable for automotive, health, industrial and defence sectors.

To strengthen Europe’s long-term sovereignty in design, stakeholders proposed investments in reusable IP libraries, open design clouds, and European EDA tools, arguing that architectural and system-level control is as strategically important as manufacturing. Persistent talent shortages also prompted calls for common European curricula beginning in primary and secondary schools with teacher involvement, mobility schemes, and streamlined international recruitment pathways. Workshop discussions also highlighted the importance of purposeful international partnerships, particularly a more formalised high-level cooperation framework with Taiwan, alongside selective strategic collaborations with Japan, South Korea and other trusted partners in areas where Europe is unlikely to develop full domestic capacity in the near term.

9. COMPARISON OF THE RESULTS OF CONSULTATION ACTIVITIES

The table presents the key results per consultation activity, organised by evaluation criteria, and by the level of consistency, complementarity, and contradiction of the results across consultation activities. Overall, there was a high convergence in the results of different consultation activities, in particular, over the need to align the Chips Act with emerging vulnerabilities, speeding-up and simplifying procedures, and the need to foster SME participation and design activities. Dissent, if any, emerged over the priorities of the Chips Act.

Evaluation criterion	**Open public consultation and call for evidence**	**Survey**	**Interviews**	**Workshops**	**Consistency**	**Complementarity**	**Contradiction**
Effectiveness	Pillar I received strong positive assessments, with a majority considering pilot lines meet their objectives. Pillar II was viewed positively by three quarters of respondents, who considered it has made the EU a more attractive location for semiconductor manufacturing. However, stakeholders question whether investment volumes are sufficient to shift Europe's competitive position and highlight structural vulnerabilities in PCBs and back-end manufacturing. Pillar III received notably lower only around a third considering objectives met; two-thirds of respondents	National authorities report highest positive effects (75% across most dimensions); RTOs report lowest (35-41%), with 35% reporting "no effects" on several dimensions. Progress varies by pillar: Pillar 1 (research-industry link) strongest at 58%; Pillar 2 (investment/capacity) mixed at 42%; Pillar 3 (supply chain resilience) weakest at only 17%, with 25% of respondents stating it too early to tell.	Pillar I is widely viewed as successful. However, effectiveness is lacking in the commercialisation of knowledge. Pilot line access for start-ups and SMEs is unclear, costly, and a missed opportunity. First-of-a-kind manufacturing projects are promising steps, but overall Pillar II suffers from weak coordination, national budget dominance, and lack of clear metrics. Effects of the Chips Act on supply chain resilience are mixed. The Act has triggered new projects, but Europe still relies heavily on Asian, especially Taiwanese, suppliers, with current investment volumes "cosmetic" compared	Workshop participants confirmed that the Chips Act delivered its main outputs. However, critical gaps remain, and large dependencies persist. Europe lacks production capacities for high-performance chip; early 100% of chips for data centres are manufactured in Taiwan. SME participation in the Chips Act remains weak. The Design Platform came only late and excludes electronics companies wishing to integrate chips; pilot line access remains cost prohibitive. Talent programmes operate at insufficient scale. Vulnerabilities persist in packaging, testing, and commodity components, with	High	High	Low

Evaluation criterion	Open public consultation and call for evidence	Survey	Interviews	Workshops	Consistency	Complementarity	Contradiction
	had not developed monitoring systems or engaged with disruption alerts. A large majority anticipate further supply disruptions, citing geopolitical risks and trade barriers as primary threats. The lab-to-fab gap remains a key barrier, and the 20% market share target is widely seen as unrealistic. SME and start-up accessibility to support instruments requires improvement.		to Asia's. Pillar 3 data collection showed voluntary mechanisms can work technically, but effectiveness was undermined because information was not meaningfully used, damaging trust. Supply-side support alone is insufficient.	PCB and packaging firms remaining outside the Act's scope.			
Efficiency	Experiences with implementation mechanisms varied considerably, with mixed perceptions among fabless companies and most foundries not having applied for facility status. Procedural complexity and slow timelines are dominant concerns; state aid approval delays are characterised as a competitive disadvantage. IPCEI is valued but undermined by	46% of national authorities encountered significant implementation challenges; 21% said too early to tell. Most frequent challenges: insufficient national co-funding capacity, competing national priorities, complex EU-national coordination, and skills/workforce limitations. Notable governance effectiveness gap: national authorities rate relevant	The Chips Act was assembled under time pressure which may explain some of its shortcomings. Stakeholders describe instruments too rigid for semiconductor capital intensity and timelines, fragmented governance across funding streams and administration levels, and procedures that are slow, untransparent, and administratively heavy. Companies face duplicated, overlapping	Processes are too slow (two years between application and funding), and favour very large projects create systematic inefficiencies. Programme coordination between DGs and the EU and national level could be improved, causing duplication and missed synergies. The most critical bottleneck is mobilising European venture capital.	High	High	Low

Evaluation criterion	Open public consultation and call for evidence	Survey	Interviews	Workshops	Consistency	Complementarity	Contradiction
	lengthy processes and less competitive funding rates. Three quarters of respondents support EU-level coordination for strategic project selection, and favour combined funding sources. Administrative burdens pose barriers, in particular for SMEs and start-ups. Fragmentation between EU and national procedures (parallel processes, inconsistent requirements, and unclear coordination) are perceived as impeding delivery.	mechanisms 38-46% effective vs RTOs only 12-24%. RTOs show higher "very ineffective" assessments (18-29%), particularly for administrative efficiency and Member State coordination. 47% of RTOs face commercialisation barriers, with insufficient risk capital and lack of industry partnerships being the most cited elements.	procedures for the same project. Complicated governance forces newer or smaller players to rely on expensive consultants. validation can take ten to twelve months versus roughly half that time or weeks in competitor countries. Time between announcement and first call has been around one year. Documentation must be submitted multiple times, digital platforms do not function as intended, and understaffed bodies are overwhelmed. Limited visibility on application progress, evaluation criteria, and decision-making makes planning difficult. Data collected from industry is perceived as one-way exercise.				

Evaluation criterion	Open public consultation and call for evidence	Survey	Interviews	Workshops	Consistency	Complementarity	Contradiction
Coherence	A large majority reported the Chips Act has contributed to improving governance and coordination between national and regional authorities. However, internal coherence gaps persist between Pillar I innovation and Pillar II manufacturing support, with stakeholders calling for bridging mechanisms. External alignment with adjacent EU frameworks (AI Act, Quantum Act, Cyber Resilience Act, defence policy) requires strengthening. Multi-level coordination across EU, national, and regional governance led through streamlined funding streams. Most respondents reported sustainable practices in place, but tensions exist between environmental regulations and semiconductor	Mixed national strategy alignment: only 33% fully aligned with Chips Act, 21% somewhat aligned, 21% reported no national strategy exists. Significant clarity gap between high-level objectives (70% clear) and application procedures (only 31% clear). Industry users reported 0% clarity on application procedure.	Coherence across instruments and programmes could be improved. Potential synergies between frontier research, proof-of-concept funding, and later-stage support function mainly because individual researchers and programme managers push them forward, not through formal coordination mechanisms. The intended continuum from R&D to pilot lines to large-scale production is not perceived as a real, functioning pathway. Another challenge is that coordination across member states is fragmented. National and regional initiatives are developed in isolation with no clear framework for aggregating efforts into strategically coherent European action. Uncertainty around definitions (first-of-a-kind), exclusion or unclear treatment of critical	The fundamental incoherence lies in expanding manufacturing capacity while underinvesting in design ecosystems and back-end manufacturing. A recurring problem is that European alternatives exist but cannot achieve cost-competitiveness due to lack of scale, yet cannot achieve scale without initial demand. “Buy European” procurement clashes with state-aid restrictions; material suppliers report pilot lines using Asian chemicals despite European alternatives; PFAS restrictions conflict with fabrication equipment needs.	High	High	Low

Evaluation criterion	Open public consultation and call for evidence	Survey	Interviews	Workshops	Consistency	Complementarity	Contradiction
	manufacturing requirements.		segments (materials suppliers, testing, metrology equipment) are obstacles to investment.				
EU added value	Strong consensus that EU-level action delivers benefits unattainable through national efforts alone, particularly scale, critical mass, and reduced fragmentation. Shared infrastructure under Pillar I is cited as a concrete example. The European Semiconductor Board is highlighted as a key coordination platform to prevent subsidy races. Views on extending information mandates were divided, with around half supporting expanded reporting. International cooperation received strong support across all stakeholder groups, with collaborative R&D and supply chain diversification as top	Strengthening EU global position received highest agreement (68%); pooling resources second (66%). National authorities were consistently more positive than RTOs, particularly on resource pooling (75% vs 53%), suggesting benefits were more visible at policy level than research operational level. Crisis response benefits were perceived more evenly across groups (RTOs 59%, National authorities 58%). However, 18-29% of RTOs strongly disagree that EU-level benefits are materialising.	The Chips Act sends a strong message of EU commitment, creating trust among investors and industry. By providing a framework for large-scale investments in semiconductor production and R&D, it fills a role Member States cannot perform and adds momentum by encouraging Member States to mobilise national resources. Only European-level efforts can collect comprehensive market intelligence across sectors and borders. Slow funding roll-out reduces attractiveness compared to more agile schemes in other regions. The state aid framework is seen as too restrictive to allow Europe to participate in global	The EU's distinctive contribution lies in coordinating across member states. The EU level is also relevant because strategic autonomy cannot be achieved at member states level. The EU also provides a collective voice for negotiating strategic partnerships. Shared infrastructure provides valuable access through pilot lines, competence centres, and EU-level consortia, with complementary IPCEI and Chips JU funding. However, the EU's greatest potential remains largely unrealised. Fragmentation undermines competitiveness; absence of mechanisms for aggregated procurement prevents leveraging market	High	High	Low

Evaluation criterion	Open public consultation and call for evidence	Survey	Interviews	Workshops	Consistency	Complementarity	Contradiction
	priorities; all public authorities reported engaging in bilateral or multilateral cooperation with third countries.		subsidy competition more effectively.	size; absence of unified work permit approach creates competitive disadvantages in talent attraction.			
Relevance	Views on framework adequacy were mixed: only one quarter agreed the current framework sufficiently addresses supply-side vulnerabilities, while almost half disagreed. The Act's scope is seen as too narrow, with excessive focus on production capacity over alignment with European industrial needs. Stakeholders identify an imbalance between leading-edge manufacturing support and mature nodes where demand is concentrated. Value-chain gaps in PCBs, packaging, back-end processes, and design s are under-addressed. For location decisions, funding access, administrative simplicity, and skilled	Strong consensus on EU-level coordination: 86% for investment/ manufacturing, 81% for R&D, 75% for monitoring. Supply chain stakeholders were the most supportive (100% for R&D, 94% for investment). Lower support for monitoring among supply chain (62%) and industry users (57%), possibly reflecting concerns about reporting obligations. Lab-to-fab gap emerged as highest priority (83%); unanimous among industry users (100%). Skills shortages (80%), supply chain disruptions (78%), and energy costs (77%) widely Recognised. Regulatory barriers	The Chips Act addresses important needs, but its initial focus did not sufficiently reflect Europe's structural strengths, long-term vulnerabilities, or global semiconductor market realities. Moreover, the Act lacked attention to emerging needs, particularly fabless design companies' strategic roles, and did not adequately consider end-user industries or the broader supply chain, creating uncertainty for investors and leaving European strengths underexploited. A recurring theme in the interviews is the need to focus on Europe's competitive advantages. The political emphasis on competing at the most	The Chips Act is relevant, in particular because of its investments in mature node production and in R&D. Stakeholders emphasised the need to move from chip-centric focus to systemic approach including packaging, testing, and assembly. The Lab-to-Fab Gap persists, with pilot lines reaching TRL6 but lacking pathways to high-volume production. Critical across all sectors.	High	High	Low

Evaluation criterion	Open public consultation and call for evidence	Survey	Interviews	Workshops	Consistency	Complementarity	Contradiction
	workforce availability emerged as most important factors. Semiconductor equipment and mainstream chip manufacturing were identified as strongest areas for EU leadership potential, with defence/aerospace and automotive as priority end-user sectors.	particularly concern supply chain actors (94%). RTOs and National Authorities both prioritised skills shortages (88% each).	advanced manufacturing nodes is unrealistic without far larger budgets.				

ANNEX 3: WHO IS AFFECTED AND HOW?

1. PRACTICAL IMPLICATIONS OF THE INITIATIVE

The proposed initiative would establish a regulatory framework to ensure the functioning of the internal market for semiconductors, secure the competitiveness of the sector, and strengthen the resilience of the semiconductor supply chain across the Union.

The measures concern a few principal stakeholder groups: the semiconductor industry, research organisations and public authorities. On the industry side, the initiative covers a broad cross-section of the semiconductor value chain, including IDMs, fabless companies, design houses, equipment manufacturers, and suppliers, as well as industrial users in sectors such as automotive, telecom, healthcare, energy, industrial robotics, defence, and security. Research organisations refers to the wider research and innovation ecosystem including Research and Technology Organisations (RTOs), academia, and scientific associations. Public authorities encompass national competent authorities in Member States and regions and the European Commission.

Benefits to industry and research organisations

Industry and research organisations stand to benefit from enhanced regulatory predictability through a clarified FoaK framework, accelerated permitting procedures, and the establishment of a Chips Fund 2.0 targeting start-ups and scale-ups. These measures are designed to support capacity expansion by large firms while facilitating technology diffusion from the world of research to SMEs and the broader industry thus bridging the lab-to-fab gap. The introduction of Strategic Projects and targeted demand-side measures would reduce investment risk for advanced facilities, stimulate demand for specialised inputs, and improve access to design and production capabilities. Proposed information-gathering measures would improve supply chain visibility across the value chain.

Furthermore, an example EUR 40 billion investment in Strategic Projects is estimated to generate EUR 6.6–11.5 billion in additional annual revenue for EU semiconductor manufacturers. (see further detail in Annex 4).

Demand-side measures are estimated to generate approximately EUR 0.35–0.46 billion in additional design-related demand for EU fabless firms in the AI Gigafactory context, assuming around 5% capture of the design value envelope, with further dynamic effects through scaling and learning. Innovation procurement (PM9) provides SMEs and start-ups with anchor customers, early revenues, and reference deployments: each euro of public demand is estimated to generate persistent revenue effects of up to EUR 0.5 and to crowd in approximately EUR 0.2 of private investment.

The proposed Business-to-Business Semiconductor Supply Chain Platform (PM5) delivers aggregated supply chain intelligence that would otherwise be prohibitively costly for individual firms to gather independently. Faster permitting (PM3) reduces delay-related capital costs by an estimated EUR 625 million for a representative EUR 20 billion fab.

Beyond direct financial returns, end-users would benefit from enhanced Union-level preparedness, particularly during emergency situations, through improved availability of crisis-prone semiconductors and more robust supply chain coordination mechanisms.

Costs and compliance burdens

Certain measures - particularly those aimed at supporting supply chain resilience - will also give rise to compliance costs. Large firms face one-off onboarding costs for the Platform (PM5) of approximately EUR 100,000 per firm, with recurrent annual costs of EUR 50,000. Across the 483 large firms in the EU semiconductor value chain, this corresponds to approximately a EUR 48 million one-off cost and EUR 24 million per year.

Information requests (PM6) are estimated at up to 10 person-days per firm per request, equivalent to EUR 2,782 per firm and up to EUR 1.34 million sector-wide per crisis request.

Project reporting under PM8 and PM2 runs at 1–2% of project value per year; procurement participation under PM9 at approximately 1.05% of contract value; and certification costs under PM10 are incremental and largely absorbed within existing schemes.

SMEs are fully exempt from reporting obligations, mitigating the risk of disproportionate administrative burdens on smaller actors. Proposed information-gathering measures may nonetheless result in additional obligations for SMEs unless proportionate mitigation mechanisms are applied in practice.

Taken together, the costs associated with these measures are substantially outweighed by the economic benefits brought by improved supply chain resilience.

Impacts on public authorities

For public authorities, Chips Act 2.0 clarifies the scope of permissible public support measures and ensures that the current framework is compatible with the co-financing of Strategic Projects from the Union budget. These changes are designed to foster more complementary and strategically oriented investments across the Union. Member States would also benefit from a strengthened Union-level crisis monitoring and preparedness mechanism, underpinned by a dedicated governance structure to ensure coordination within the single market. National public authorities are, however, expected to incur administrative and adjustment costs associated with assessing applications for support measures.

At EU level, implementation of the preferred option requires a one-off investment of approximately EUR 70 million to develop the Business-to-Business Semiconductor Supply Chain Platform (PM5), alongside staffing of 19 FTEs (additional and redeployment) to administer Strategic Projects, operate the Platform, oversee information requirements, and manage innovation procurement. Here, total annual administrative costs for the Union are approximately EUR 3 686 000[2].

The proposed framework would, for the first time, allow the EU budget to directly co-fund industrial-scale semiconductor manufacturing, design, and supply chain resilience activities, unlocking a coordinated, cross-border investment pipeline that goes beyond the reach of the current framework.

Enhanced coordination of public support through Strategic Projects would promote deeper integration across design, manufacturing, and advanced packaging activities. Critically, access to

[2] Full Time Equivalents (FTEs) were established based on internal Commission analysis. The hourly wage for Member States and businesses was estimated at EUR 29.4 /h. The European Commission costs per FTE are EUR 194 000/year.

supply chain information outside of a crisis context would allow the Commission to identify specific bottlenecks, dependencies, or disruptions before they reach crisis activation thresholds, thereby shifting focus towards proactive anticipation and mitigation measures. The aforementioned Platform and mandatory information tools (PM5, PM6) would give the Commission an early-warning and crisis-response capability that currently does not exist. At the same time, appropriate safeguards would be applied throughout to ensure strict protection of business-confidential information, proportionality of requests, and full compliance with EU data protection and competition rules.

For Member States, recurrent costs for accelerating permitting (PM3) and validation of mandatory information submissions (PM5, PM6) are moderate and largely absorbable within existing administrative structures.

Impacts on society

Society at large stands to benefit from wider availability of supply of both leading-edge and mainstream semiconductor technologies. Improved Union-level crisis preparedness would benefit consumers and citizens directly, including through better continuity of essential services such as healthcare, energy, communications, and defence during supply disruptions. Reduced reliance on concentrated third-country supply chains lowers the Union's exposure to geopolitical coercion and supply weaponisation. Domestic sourcing criteria under PM10 reduce the risk of embedded vulnerabilities in critical systems. Citizens would also benefit as workers, with the creation of new high-skilled positions and increased labour mobility. Over time, a stronger EU semiconductor ecosystem is expected to contribute to greater product choice, higher quality, and more competitive pricing for all downstream users of semiconductor-enabled goods. No direct costs to citizens are anticipated.

Methodology

The assessment of impacts draws on multiple data sources, including the targeted stakeholder consultation, comprising interviews and surveys, the open public consultation, the Call for Evidence, and desk research. Where possible, impacts have been quantified on the basis of available assessments or modelling. Where dedicated modelling was not feasible due to data or tooling constraints, a qualitative assessment was carried out drawing on existing studies and stakeholder input. Further details on the methodological approach, including detailed tables and estimates, are provided in Annex 4.

2. SUMMARY OF COSTS AND BENEFITS

I. Overview of Benefits (total for all provisions) – Preferred Option		
Description	***Amount***	***Comments***
Direct benefits		
Structural expansion and rebalancing of the EU semiconductor industrial base	Qualitative and quantitative; high strategic significance EUR 6.6-11.5 billion additional annual manufacturing revenue; up to EUR 7-9 billion potential design revenues	Assuming EUR 15 billion in public support, PO2 increases EU semiconductor manufacturing capacity through Strategic Projects, generating an estimated EUR 6.6–11.5 billion in additional annual revenue depending on the technology mix. Furthermore, capacity expansion is estimated at approximately 108,000 to 222,000 wafers per month. In addition, expanded manufacturing capacity generates recurring fiscal returns for Member States. Applying a

		value-added ratio of 34% and an average fiscal capture rate of 16.5%, annual direct tax revenues are estimated at EUR 380-662 million once full operational capacity is reached. In parallel, demand-side measures such as innovation procurement may in the short- term generate approximately EUR 0.35–0.46 billion in additional design-related demand for EU-based fabless semiconductor firms, with further indirect benefits through learning effects, scaling and improved investment conditions. *Main beneficiaries: EU industry (fabless firms, foundries, end using industry), Member States.*
Enhanced investment viability and capital efficiency for large-scale semiconductor projects	Quantitative and qualitative; high significance Indicative avoided delay costs of ~EUR 600–650 million per EUR 20 billion fab	Under PO2, EU co-funding, alignment of FoaK/IPF/OEF procedures, fast-track permitting and demand-side measures jointly improve the bankability of large-scale semiconductor projects. EU co-funding lowers the effective cost of capital, and shortens time to break even. Demand-side instruments such as innovation-oriented public procurement increase revenue predictability. Empirical evidence suggests that each euro of public demand can generate persistent revenue effects of up to EUR 0.5 and crowd in approximately EUR 0.2 of additional private investment. Streamlined and faster permitting further reduces delay-related capital costs. Permitting and design phases in the EU are on average around 7.5 months longer than in leading Asian jurisdictions. Assuming that each year of delay increases total project costs by approximately 5%, this corresponds to an additional cost of around 3.1% of total investment, or approximately EUR 625 million for a representative EUR 20 billion advanced fabrication plant. Earlier and more predictable utilisation of new facilities enhances financial viability, particularly for specialised and application-specific production lines. *Main beneficiaries: EU Industry (semiconductor investors), Member States, regional authorities.*
Enhanced supply chain resilience and crisis preparedness	Qualitative; high economic significance Up to EUR 1.53 trillion in downstream production value exposed in worst-case disruption scenario	PO2 strengthens monitoring, demand stability and crisis coordination through the Business-to-Business Semiconductor Supply Chain Platform. Improved visibility of structural vulnerabilities enables earlier risk detection and coordinated response, reducing the likelihood and duration of supply bottlenecks. In 2023, motor vehicles and transport equipment (EUR 934 billion) and machinery and equipment (EUR 600 billion) together generated over EUR 1.53 trillion in production value. In the absence of coordinated monitoring and mitigation, this output remains exposed to semiconductor supply shocks.

		PO2 safeguards the functioning of the Single Market during crises by supporting the free flow and availability of semiconductors needed by critical supply chains. *Main beneficiaries: End user industries, Member States*.
Strengthened EU economic security, resilience and crisis management capacity	Qualitative; high strategic and societal significance	By promoting dual semiconductor sourcing from domestic undertakings, PO2 reduces the risk of embedded vulnerabilities, malicious interference and geopolitical coercion in critical systems. This enhances the integrity of defence, telecommunications, healthcare, energy and digital infrastructure. Reduced reliance on externally concentrated supply chains lowers exposure to supply weaponisation and strengthens the EU's strategic autonomy in vital technologies for competitiveness, security and defence. . In severe disruption scenarios, improved semiconductor availability may contribute to protecting public safety and mitigating life-threatening risks. *Main beneficiaries: citizens, public authorities, end user industries (e.g. defence and telecom sectors), and EU industry in general.*
Strengthened semiconductor EU innovation ecosystem and accelerated industrial deployment	Qualitative; medium–high significance	PO2 enhances R&D and innovation outputs through expanded pilot lines, a strengthened Chips Fund, and R&D components embedded within Strategic Projects. Increased co-location of research and manufacturing improves knowledge transfer, scale-up capacity and innovation intensity across the value chain. Innovation-oriented public procurement further stimulates technological development. Empirical evidence (see Annex 4 Section 6) suggests that firms participating in such procurement experience 10–20 percentage point higher probabilities of product innovation and approximately 6 percentage point higher probabilities of process innovation compared to otherwise similar firms. Shorter and more secure design-to-fabrication cycles within the EU reduce lead times, improve protection of sensitive intellectual property and increase customer trust. This particularly benefits SMEs and start-ups seeking to scale innovative semiconductor solutions. *Main beneficiaries: universities, RTOs, EU Industry (SMEs, start-ups, semiconductor firms).*
Structural expansion and rebalancing of the EU semiconductor industrial base	Qualitative and quantitative; high strategic significance EUR 6.6–11.5 billion additional annual manufacturing revenue; up to EUR 7–9 billion potential design revenues	PO2 increases EU semiconductor manufacturing capacity through Strategic Projects, generating an estimated EUR 6.6–11.5 billion in additional annual revenue depending on the technology mix. With EUR 15 billion in public support, capacity expansion is estimated at approximately 108,000 to 222,000 wafers per month, in comparison, under the baseline conditions additional capacity of 321,500 wafers per month is announced to date (projections till 2030).

		In addition, expanded manufacturing capacity generates recurring fiscal returns for Member States. Applying a value-added ratio of 34% and an average fiscal capture rate of 16.5%, annual direct tax revenues are estimated at EUR 380–662 million should the aforementioned projects be realised. *Main beneficiaries: EU industry (fabless firms, foundries, end using industry), Member States.*
Enhanced investment viability and capital efficiency for large-scale semiconductor projects	Quantitative and qualitative; high significance Indicative avoided delay costs of ~EUR 600–650 million per EUR 20 billion fab	Under PO2, EU co-funding, alignment of FOAK/IPF/OEF procedures, fast-track permitting and demand-side measures jointly improve the bankability of large semiconductor projects. EU co-funding lowers the effective cost of capital, stabilises expected utilisation rates and shortens time to break even. Demand-side instruments such as innovation-oriented public procurement increase revenue predictability. Empirical evidence suggests that each euro of public demand can generate persistent revenue effects of up to EUR 0.5 and crowd in approximately EUR 0.2 of additional private investment. Streamlined and faster permitting further reduces delay-related capital costs. Permitting and design phases in the EU are on average around 7.5 months longer than in leading Asian jurisdictions. Assuming that each year of delay increases total project costs by approximately 5%, this corresponds to an additional cost of around 3.1% of total investment, or approximately EUR 625 million for a representative EUR 20 billion advanced fabrication plant. *Main beneficiaries: EU Industry (semiconductor investors), Member States, regional authorities.*
Indirect benefits		
Job creation across the semiconductor value chain	Around 4,700 to 7,300 direct jobs Approximately 10,000 to 36,500 indirect and induced jobs	Employment grows due to construction, operation of new fabs, supply chain expansion, and design-centred SME activity. Stabilised supply reduces disruption-related job losses in dependent industries Strategic Projects are estimated to create **around 4,700 to 7,300 direct jobs,** depending on the technology mix ([3]). Applying conservative employment multipliers consistent with open and globalised value chains, this corresponds to approximately **10,000 to 36,500 indirect and induced jobs**. Higher employment outcomes are associated with capacity expansion following the current wafer mix, while leading-edge manufacturing delivers fewer but more capital- and skill-intensive direct jobs. *Main beneficiaries: workers, regional labour markets.*
Broader economic spillovers	Qualitative and quantitative; medium–high significance	Investment in semiconductor capacity generates wider spillovers across the value chain, including for equipment manufacturers, materials suppliers, engineering services and

[3] Assuming public support of EUR 15 billion from the Union and Member States

		other specialised suppliers. Regional economies benefit from clustering effects, technology diffusion and increased productivity in downstream sectors. Over time, these spillovers contribute to sustained value creation and tax revenues beyond the directly supported projects. *Main beneficiaries: Member States, upstream and downstream industries.*
Administrative cost savings related to the 'one in, one out' approach		
Administrative cost savings due to the Strategic Projects (simplification effects)	Qualitative (administrative efficiency gain)	Semiconductor firms and national authorities benefit from reduced duplication of administrative steps when compared to fragmented national processes under the baseline. Strategic Projects create a coordinated EU-level project pipeline, simplifying interactions and streamlining procedural handling for a select number of projects that qualify as Strategic Projects. *Main beneficiaries: EU industry, public authorities.*
Administrative cost savings due to faster and more predictable permitting processes	Qualitative (reduced administrative effort)	Firms benefit from fewer iterative exchanges with permitting authorities and clearer procedural timelines. While not removing obligations, PO2 reduces the time and administrative workload associated with managing complex investment dossiers. *Main beneficiaries: EU industry, public authorities.*
Administrative cost savings due to reduced ad hoc crisis information requests	Qualitative (reduction of repeated, urgent data calls)	Through the Business-to-Business Semiconductor Supply Chain Platform, companies and national authorities face fewer uncoordinated, last-minute requests. The structured, recurrent mechanism replaces fragmented information demands that currently generate high administrative burden. *Main beneficiaries: EU industry, public authorities.*

II. Overview of costs – Preferred option							
		Citizens/Consumers		**Businesses**		**Administrations**	
		One-off	**Recurrent**	**One-off**	**Recurrent**	**One-off**	**Recurrent**
Action (a)	Direct adjustment costs	None	None	None	None	Administrative capacity upgrades for accelerated permitting (**PM3**) • Expected to be largely absorbed within existing structures • Includes: temporary staff reinforcement, digitalisation of permitting procedures, streamlining and planning workflows. Establishment of governance and procedural systems for Strategic Projects (PM8) • Costs related to the development of selection procedures, evaluation criteria, monitoring frameworks, reporting templates etc.. Platform development and initial IT infrastructure (PM5)	EU-level/Member State co-funding for Strategic Projects (**PM8**) • Requires Union and Member States contributions of at least EUR 15 billion to co-fund Strategic Projects of importance to Europe's technological sovereignty, including leading-edge fabs, packaging hubs, design facilities and supply chain resilience investments.

						• EUR 70 million for platform setup and development which includes the development and deployment of the platform and IT infrastructure, security infrastructure and interoperability tools.	
	Direct administrative costs (to the 'one in, one out' approach)	None	None	Technical IT integration with the Business-to-Business Platform (PM5) • Voluntary cost for large companies themselves would be ~€ 100K for the initial year ([4]) Administrative onboarding and integration with the Platform (PM5) • **Voluntary low-medium cost of circa 3 person-days** which are required to establish compliance with new regulatory obligations. Involves account creation,	Mandatory disclosures of supply chain vulnerabilities based on qualitative assessment (PM6) • Approximately **10 person-days** are required for large firms for reporting ([5]). Which can be translated into **EUR 2782,** per year ([6]) In the case of anticipated crisis and assuming **all companies** are requested to submit data the total effort might cost up to **EUR 1.34 million per request** across the entire value chain in Europe.	None	Processing and validating mandatory information submissions (PM5, PM6) • Moderate costs to sustain the capacity of the Commission and national competent authorities to review, classify, and validate firm-level vulnerability data on a continuous basis. Administrative coordination under the Platform (PM5). • Low-medium cost for regular coordination between Member States and the Commission to manage queries, update procedures,

([4]) Estimation from the Supply chain Working Group of the Industrial Alliance on Processors and Semiconductor Technologies
([5]) Reporting obligations
([6]) Assuming an annual salary of a supply chain analyst of EUR 60k.

				internal procedural setup, and alignment of data formats.	Annual Platform operational participation costs (PM5) • The cost for the large companies themselves would be ~€ 50K for the yearly operations. ([7]) • The cost covers ongoing data sharing; system maintenance; and internal monitoring alignment. Administrative reporting linked to Strategic Projects and FoaK (PM8, PM2) • 1–3 FTE/year, corresponding to 1-2% of the project value ([8]).Here, cost includes monitoring reports, compliance documentation, EU-level coordination reporting		and issue formal information requests. Administrative reporting and coordination for Strategic Projects (PM8) • 12 FTEs at EU level to supervise Strategic Projects which covers administrative (non-fiscal) tasks such as monitoring, reporting, compliance checks, and cross-border coordination linked to Strategic Projects (11). • Total costs: EUR 2 328 000 Increased administrative burden from demand-side instruments (PM9) Medium cost to the EU and other administrations for the administration of innovation procurement, early-stage offtake programmes and Chip Innovation Partnerships

([7]) Estimation from the Supply chain Working Group of the Industrial Alliance on Processors and Semiconductor Technologies

([8]) The administrative burden observed in Horizon Europe projects (typically estimated at 6–10% of project budgets) is used as a reference point; this roughly corresponds to approximately 0.5–1 full-time equivalent (FTE) of administrative effort per project per year. IPCEI reporting and compliance obligations are assumed to require approximately two to three times higher effort than Horizon Europe projects, reflecting additional State aid requirements, dual reporting to national and EU authorities, and longer monitoring periods. This implies an estimated administrative effort in the order of 1–3 FTE per year for a typical IPCEI participant. When scaled to the substantially larger investment volumes of IPCEI projects, this level of effort corresponds to only a small fraction of total project budgets (typically around or below 1–2%). These figures should be interpreted as indicative.

([11])In the current Chips JU, 18 FTEs supervise a budget of around EUR 4.175 billion EU funding.

					Administrative participation costs under innovation procurement (PM9) • Approx. 1.05% of contract value ([9]), [10] which includes: bid preparation, compliance documentation.		requires additional staffing and contracting capacity. Operating the Business-to-Business Platform (PM5) • EU-level cost of 6 FTEs for monitoring, analysis and crisis preparedness functions; handling the RFI's; additional IT maintenance and security costs. • Total costs: EUR 1 164 000
	Direct regulatory fees and charges	None	None	None	None	None	None
	Direct enforcement costs	None	None	None	Adaptation of production processes to meet technological and resilience requirements in Strategic Projects (PM8) • Costs likely to be negligible as the Strategic Projects' designation is only for projects meeting the criteria at the moment of application. .		Oversight of mandatory information requirements (PM5, PM6). • Approximately 2 FTEs for the Commission and Member States to review compliance, validate data, flag inconsistencies.

([9]) PwC, London Economics, & Ecorys. (2011). Public procurement in Europe: Cost and effectiveness. European Commission, Directorate-General for Enterprise and Industry.
([10]) Rodionova, Y., Balaeva, O., Yakovlev, A., & Esaulov, D. (2018). Public procurement transaction costs: A country-level assessment. Public Sector Studies, 20(4), 66–81.

	Indirect costs	Opportunity cost of public money being directed elsewhere	None	Opportunity cost of capital allocation • Firms may decide to redirect investment away from other activities to invest in Strategic Projects.	Increased competition for skilled labour • Strategic Projects intensify demand for technicians, engineers, and specialised operators, increasing hiring and wage pressures.	None	Long-term fiscal exposure from Strategic Projects (PM8) • High costs which, despite being classified as investment expenditure, generate significant fiscal pressure. Transitional dual-system administrative burden (PM5, PM6) • Low-medium (and diminishing) cost. Until the Platform and governance system reach maturity, public administrations handle both legacy crisis tools and new mechanisms.

III. Application of the 'one in, one out' approach – Preferred option(s)			
[M€]	**One-off** (annualised total net present value over the relevant period)	**Recurrent** (nominal values per year)	**Total**
Industry and enterprises			
New administrative burdens (INs)		Mandatory disclosures of supply chain vulnerabilities. • **Medium-low cost** expected, estimated at **up to 10 person-days/year** for large firms (benchmarked to costs of reporting) per request. Can be translated into **EUR 2783** cost per request ([12]).	The additional administrative costs for businesses likely will not exceed 0.1 FTE.
Removed administrative burdens (OUTs)		Simplification from Strategic Projects • Reduced duplication of administrative steps during initial project preparation. • Clearer EU-level project pipeline reduces time spent identifying relevant authorities and procedures. Faster and more predictable permitting procedures	.

([12]) Assuming an annual salary of a supply chain analyst of EUR 60k.

		• Fewer iterative exchanges with permitting authorities. Assuming that delays add around 5% of total project value per year, a 7.5-month delay (about 0.625 years) translates into a cost penalty of approximately 3.1% of project value. In Taiwan, these phases typically take between 6 and 13 months, whereas in the EU they usually require 16 to 18 months ([13]). This implies that permitting and design in the EU are approximately 3 to 10 months longer than in Taiwan. Using midpoint estimates, ([14]) the average amounts **to roughly 7.5 months additional time**. As set out in Annex 3, und the assumption that each year of delay adds around 5 % of total project value ([15]), this implies an additional cost equivalent to 3.125 % of overall investment. For a representative EUR 20 billion advanced semiconductor fabrication plant, this corresponds to **roughly EUR 625 million** in additional expenditure • Smoother administrative handling of investment dossiers throughout project lifecycle. Fewer ad hoc crisis-related information requests • Companies no longer need to respond to urgent, unstructured, duplicative	

([13]) Figure 16 - Average duration of projects for building wafer fabs (Source: Exyte, 2025)
([14]) Around 9.5 months for Taiwan and 17 months for the EU
([15]) https://www.csis.org/analysis/streamlining-permitting-process-fab-construction

		requests from multiple authorities during disruptions. Partial outsourcing of market-intelligence activities	
Net administrative burdens*	One-off cost for onboarding and integration with the Business-to-Business Supply Chain Platform is not offset by any one-off benefits.	Small net administrative burden, as mandatory disclosures are largely offset by simplification gains (permitting, crisis data calls, reduced monitoring needs).	
Adjustment costs**		• Companies no longer need to respond to urgent, unstructured, duplicative requests from multiple authorities during disruptions. • Firms (especially SMEs) rely on aggregated insights from the Business-to-Business Platform, reducing time spent on internal analysis and monitoring tasks.	
Public administrations (European Commission and Member States)			
New administrative burdens (INs)	None	Processing and validating mandatory information submissions. • Moderate cost for national competent authorities who must review, classify, and validate firm-level vulnerability data on a continuous basis. Recurrent administrative coordination under the Platform..	

		• Low to moderate costs for public authorities due to regular coordination between Member States and the Commission to manage queries, update procedures, and issue formal information requests. Administrative reporting and coordination for Strategic Projects • Moderate costs covering administrative (non-fiscal) tasks such as monitoring, reporting, compliance checks, and cross-border coordination linked to Strategic Projects. Increased administrative burden from demand-side instruments. • **Moderate cost for the Commission in the** administration of innovation procurement, early-stage offtake programmes requires additional staffing and contracting capacity.	
Removed administrative burdens (OUTs)	None	Simplification due to Strategic Projects • Reduced duplication of administrative steps during initial project preparation Reduced ad hoc crisis information requests • Member States receive a steady stream of structured, standardised data and fewer emergency data calls need to be issued to industry. National competent	Administrations would incur a moderate recurrent cost from processing mandatory information, coordinating the Platform, fulfilling Strategic Project reporting tasks, and administering demand-side instruments.

		authorities benefit from centralised information flows, reducing the need to run parallel national reporting channels. The shared EU governance framework lowers duplication across Member States, especially for cross-border projects. Streamlined information exchange among Member States • Centralised Platform removes the need for parallel national reporting channels. • Less duplication in sharing and validating supply chain intelligence across borders. More predictable permitting processes • Clearer permitting pathways reduce back-and-forth between national authorities and firms.	
Net administrative burdens*	None	Moderate net burden, partly offset by structural simplifications.	
Adjustment costs**			
Total administrative burdens***			

(*) Net administrative burdens = INs – OUTs;

(**) Adjustment costs falling under the scope of the OIOO approach are the same as reported in Table 2 above. Non-annualised values;

(***) Total administrative burdens = Net administrative burdens for businesses + net administrative burdens for citizens

3. RELEVANT SUSTAINABLE DEVELOPMENT GOALS

IV. Overview of relevant Sustainable Development Goals – Preferred Option(s)		
Relevant SDG	**Expected progress towards the Goal**	**Comments**
SDG 4: Quality education	Chips Act 2.0 will result in an increase in training opportunities for enhancing digital skills, particularly those related to semiconductor technologies, thus contributing to quality education and lifelong learning.	
SDG 8: Decent work and economic growth	Chips Act 2.0 would contribute to the sustainable development goal of decent work and economic growth by ensuring a well-functioning Single Market in times of crisis and therefore mitigate severe economic repercussions through loss of business opportunities and crisis-related redundancies. It is expected that this initiative will result in an increase in employment due to the spurring of additional chip design and manufacturing capacities in the EU and the increase in SMEs and startups thanks to a renewed Chips Fund.	
SDG 9: Industry, innovation and infrastructure	Chips Act 2.0 is expected to increase the number of semiconductor facilities and support the development of next generation semiconductor technologies in Europe.	

ANNEX 4: ANALYTICAL METHODS

1. MODELLING ECONOMIC IMPACTS

1.1. EU semiconductor market size estimation

1.1.1. Establishing a starting point for BAU scenario

This section establishes the baseline for the market size of Europe's semiconductor industry by quantifying the total **revenue generated** by firms headquartered **within the EU27 in 2023**. The analysis draws on the IDC 2030 Semiconductor Market and Global Value Chain Study, which provides harmonised data across the principal value chain segments and global regions. In this section we focus only on devices, for overall value chain analysis refer to the sections below.

The IDC dataset reports industry revenues at market (transaction) prices. Consequently, the figures represent the economic activity of semiconductor firms based in the EU27. Within this device-focused perspective (chip-level), **Europe generated EUR 50.52 billion in semiconductor device revenues in 2023**. This mostly reflects the activity of Europe's major integrated device manufacturers (IDMs), including Infineon, NXP and STMicroelectronics, whose portfolios span automotive, industrial, power and application-specific devices.

To provide further granularity, Table 1 presents the device-level composition of semiconductor revenues in the EU27 in 2023. This breakdown will serve as the basis for modelling differential growth dynamics, as each device type follows a distinct global demand and pricing trajectory.

Table 1. EU27 semiconductor revenue by device category, 2023 (EUR million and % share). *Source: IDC 2030 study reporting.*

Device category	2023 revenue (EUR million)	Share of total EU semiconductor revenue (%) ([16])
Application-specific (ASIC, ASSP, etc.)	14 871	29.4
Micro-components (MCUs, MPUs, DSPs)	12 691	25.1
Discretes, sensors, actuators	12 239	24.2
Analogue	6 441	12.7
Optoelectronics	2 611	5.2
Memory	1 460	2.9
Logic	204	0.4
Total	**50 518**	**100.0**

The device-level composition confirms that Europe's semiconductor industry is dominated by mainstream semiconductors, i.e. in the application-specific devices, micro component, and analogue market segments. Together these 3 categories account for nearly 80% of total semiconductor manufacturing revenue in Europe. These areas align closely with Europe's

([16]) Includes revenues generated in production capacity outside the EU by European semiconductor firms.

comparative advantages in automotive, industrial, and power electronics. **Memory and logic represent marginal shares (below 4% combined)**, whereas globally these two market segments represent the bulk of revenue growth in the coming decade, driven by artificial intelligence.

This product structure is critical for later-stage modelling, as different device types exhibit distinct price elasticity, innovation cycles, and capital intensity. For instance:

- Analogue and power devices have stable long-run demand linked to electrification and automotive transition, but lower revenue growth per wafer.
- Micro-components and application-specific devices capture system-level integration gains and drive mid-range revenue growth.
- Logic and memory, while minor in EU output, tend to experience high global price volatility and cyclical dynamics that are more visible in the more mature and commoditised segments, particularly older-generation logic and memory.

1.1.2. Modelling the BAU scenario

The modelling draws primarily on IDC's **2023–2030 forecast series**,([17]) which captures verified investment pipelines, corporate announcements, and regional growth expectations. The dataset reflects both global market recovery after the 2022 downturn and strong European capital formation driven by public subsidies and private investment in new fabs and equipment capacity.

According to IDC, **EU27 device revenues are expected to reach EUR 85.073 billion by 2030**, corresponding to a compound annual growth rate **(CAGR) of 7.7 %** over the period 2023–2030. This IDC forecast forms the baseline from which the post-2030 device projections are developed. This is **below the global CAGR of 8.75% and well below the US CAGR of 10.6%**.

This lagging growth rate is understandable when considering that Europe does not have significant players in AI which is the key driver of growth in the broader industry. ([18]) Furthermore, European companies do not benefit from the price-setting capacity of foundries active in the 7nm and below process nodes typical of AI chips. ([19])

This AI boom is not volume-driven, unlike past cycles, but price-driven, fuelled by steep increases in average selling prices (ASPs) for AI devices ([20]). **Industry growth therefore reflects two dynamics**: one driven by AI logic and AI memory inflation, and another covering mature nodes, automotive, and analogue devices which is growing more slowly

Europe's semiconductor industry is largely absent from AI-intensive segments. Its industrial base is concentrated in analogue, power, microcontroller, and application-specific semiconductors, which are vital for automotive, energy, and industrial systems but do not benefit from AI-driven ASP inflation. In fact, the automotive and industrial applications end-market represent 70% of the EU's semiconductor revenues. ([21])

([17]) IDC, Semiconductors market data by feature size, sector and region, CNECT/2022/MVP/0084 – Second Interim Report

([18]) IBS Global Semiconductor Industry Service, May 2025

([19]) Future Horizons - The Global Semiconductor Monthly Report December 2025

([20]) EE Times Europe (2025), "The Recovery Base Is Fragile, Future Horizons' Penn Says", 15 April 2025, available at https://www.eetimes.eu/the-recovery-base-is-fragile-future-horizons-penn-says/.

([21]) IDC, Semiconductors market data by feature size, sector and region, CNECT/2022/MVP/0084 – Second Interim Report

Therefore, the figure by IDC on the EU's growth is in line with the **expectation that Europe's revenue trajectory will lag global averages beyond 2030** for structural reasons i.e. Europe's specialisation lies in mature nodes, notably analogue, power, and automotive semiconductors. These generate lower value added and grow more slowly in value than advanced logic and memory, where both demand and average selling prices are structurally higher. With AI-related products potentially reaching around 70 % of the global market by 2030, this divergence implies that Europe's growth could lag the global average more markedly.

Given these structural conditions, Europe's semiconductor device revenues under the BAU scenario are expected to grow in line with global foundry demand for mature and mid-range technology nodes.

Projections from IBS (International Business Strategies) indicate that, between 2030 and 2035, foundry revenues at technology nodes of 40 nm and above are expected to grow at annual rates ranging from negative 1.5 % to positive 7.5 % growth, depending on the node size, with most mature nodes clustering around at least 5 % (Table 2). This shows a clear divide in market growth for both advanced technology and mature nodes.

Table 2. Global Foundry market growth by technology node. *Source: IBS Analysis of Global Foundry Market, December 2025.*

Node	Growth rate around 2030–2035 (%)
45/40 nm	~6.25 – 6.72
65 nm	~5,46 – 7.54
90 nm	~(1.5) *negative growth*
130 nm	~5.60 – 5.78
180 nm	~5.29 – 5.59
250 nm	~6.27 – 6.67

Reflecting the EU's current wafer mix, which remains concentrated in these mature nodes and has limited exposure to leading-edge (the AI-driven market segments), **the BAU projection applies an average long-run revenue growth rate of approximately 5% per year for EU27 semiconductor device revenues over 2030–2035.** This rate lies below the global average but is consistent with the projected growth dynamics of the technology nodes most relevant to the European manufacturing base.

Table 3. Assumptions for the revenue growth model. *Source: Compiled by the authors.*

Parameter	Global market	Europe (BAU)	Comment
2030–2035 CAGR	~9 % (including all node sizes) ([22])	5%	Adjusted for limited exposure to AI-driven growth and mature product mix
Growth driver	AI logic, HBM, accelerators	Automotive, power, industrial semiconductors	ASP divergence

([22]) IBS, Global Semiconductor Industry Service, Analysis of Foundry Market, December 2025.

Relative global share	Concentration in Asia and US	Stable at 8–9 % ([23])	No structural capacity shift expected
Key risks	AI-cycle volatility, trade barriers, CAPEX constraints	Energy prices, project delays, limited AI participation	Structural, not cyclical

Using the IDC 2030 device value of **EUR 85.073 billion**, the following projections are obtained:

- 5% CAGR → $85.1\times(1.05)^5 \approx 85.1\times1.276 \approx$ EUR 108.6 billion

Therefore, under the BAU, EU27 device revenues increase from EUR 85.1 billion in 2030 to approximately EUR 108.6 billion in 2035. Furthermore, over the full 2023–2035 period, the EU27 semiconductor device segment is therefore projected to grow from EUR 50.5 billion to around EUR 108.6 billion. This corresponds to a cumulative increase of roughly 115 % and an implied **average annual growth rate of approximately 6.6%.** This shows a deceleration of the European revenue growth, from the period 2025-2030 (7.7%) to the period 2030-2035 (5%), where the importance of AI and leading-edge manufacturing will become more prominent.

1.2. EU Semiconductor manufacturing capacity estimation

1.2.1. Establishing a starting point for BAU scenario

The below estimate reflects **Europe's physical potential to manufacture semiconductor wafers in front-end fabs**, but it does not indicate how much is actually produced, nor the revenue or value chain contributions of other semiconductor segments.

Data anchors

Global installed capacity, 2023: 29.6 million wpm (wafers per month – 200 mm-equivalent). Source: SEMI World Fab Forecast release of 2 January 2024 ([24])202 **([25])**. The IDC report also states that all manufacturing currently located in the EU is at mature nodes (≥ 40 nm) and that no advanced or leading-edge manufacturing is available in the region.

The EU27 share (8.1 %)[26] is applied to SEMI's global installed capacity:

29.6 million wspm × 0.081 = 2.40 million wpm (200 mm-equivalent)

IDC expresses all manufacturing capacity in **300mm-equivalent** units.
Wafer-size normalisation follows surface-area ratios:

- Surface area of a 200 mm wafer: $\pi \times 100^2$
- Surface area of a 300 mm wafer: $\pi \times 150^2$
- Surface Ratio: 200 mm / 300 mm wafer = $4/9 \approx 0.444$

([23]) Europe's recent revenue share has shown short-term volatility due to downturns in automotive and industrial semiconductors, although its medium-term structural share typically remains within the 10–12 % range.
([24]) **SEMI (2024).** *Global Semiconductor Capacity Projected to Reach Record-High 30 Million Wafers per Month in 2024, SEMI Reports.* Press release, 2 January 2024. SEMI, Milpitas, CA. Available at: https://www.semi.org/en/news-media-press-releases/semi-press-releases/global-semiconductor-capacity-projected-to-reach-record-high-30-million-wafers-per-month-in-2024-semi-reports [Accessed: October 2, 2025].
([25]) IDC, Semiconductors market data by feature size, sector and region, CNECT/2022/MVP/0084 – Second Interim Report
([26]) IDC, Semiconductors market data by feature size, sector and region, CNECT/2022/MVP/0084 – Second Interim Report

Therefore: 2.40 million wspm × 0.444 ≈**1.07 million wpm (300mm-equivalent)**

1.2.2. Modelling the BAU scenario

The BAU scenario is anchored in a documented 2023 baseline and projected forward on that basis. Capacity projections are drawn from the IDC Semiconductor Fab database, which provides estimates of global and EU27 production capacity expressed in 300mm (12") wafer starts per month equivalents. As the dataset extends only to 2030, projections to 2035, the end of the next MFF, are derived by applying global production trends to the EU context..

Pipeline used in BAU

The construction of the BAU scenario relies on projections from the IDC Semiconductor Fab database. The figures in the table below reflect new projects that have already been announced (see Table 4).

Table 4. Projected new fab capacity resulting from the announced projects. *Source: IDC Semiconductor Fab database.*

Product Type	2023	2024	2025	2026	2027	2028	2029	2030	Total
MEMs								14,000	14,000
Analog/Mixed Signal			6,700		48,000				54,700
Discrete (incl. power)			50,000	20,000	48,000			28,900	146,900
Foundry					9,200				9,200
Logic	35,000			21,700		40,000			96,700
EU27 total	**35,000**	**0**	**56,700**	**41,700**	**105,200**	**40,000**	**0**	**42,900**	**321,500**

Based on announced and already committed semiconductor manufacturing projects in Europe, **the EU's installed wafer fabrication capacity is projected to rise from approximately 1.07 million wafers per month (12-inch, 300 mm equivalent) in 2023 to over 1.39 million by 2030**. This represents an overall increase of about 30%, **corresponding to an average annual growth rate of 3.9%** in capacity. These figures cover only projects that are publicly announced and sufficiently advanced to be included in the business-as-usual (BAU) scenario. They do not take into account potential future investments or investments currently under scrutiny for State aid. The estimate therefore provides a conservative baseline for Europe's manufacturing capacity under existing commitments.

The fastest market expansion is anticipated in leading-edge segments, where EU-headquartered players have limited presence. In this segment, growth in manufacturing capacity is expected to be more limited in Europe than in other world regions. Furthermore, any such increase is likely to serve an IDM model rather than operate as an open foundry.

In line with these findings, this BAU model assumes that all announced and already funded projects determine Europe's capacity growth up to 2030, which is already represented in the IDC projections data. **After 2030, capacity increases are assumed to result from incremental brownfield expansion, tool upgrades, and new projects yet to be announced. To represent this trend, and in line with the manufacturing vs. revenue growth over the period 2023-2030 summarised in the previous paragraph, scenarios of organic growth factors of +2 %, +3 %, and +4 % per year are envisaged from 2031 onwards** to the 2030 installed capacity level of 1

391 500 wafers per month (300 mm equivalent), in order to determine the manufacturing capacity by 2035 (Table 5).

Table 5. Projection of Europe's manufacturing capacity following the organic growth assumption.
Source: prepared by the authors.

Year	Known project path	+2 % p.a.	+3 % p.a.	+4 % p.a.
2031	1,391,500	1,419,330	1,433,245	1,447,160
2032	1,391,500	1,447,717	1,476,242	1,505,046
2033	1,391,500	1,476,671	1,520,530	1,565,248
2034	1,391,500	1,506,204	1,566,146	1,627,858
2035	1,391,500	1,536,328	1,613,130	1,692,973

The projection based on announced and committed projects indicates an installed manufacturing capacity of about 1.39 million wafers per month (300 mm equivalent) by 2030, representing an overall increase of approximately 30 % compared with 2023.

When an organic growth factor of +2–4 % per year is applied from 2030 onwards to capture incremental brownfield expansions and future, as yet unannounced, projects, the model yields 2035 capacity range of roughly 1.54–1.69 million wafers per month. This corresponds to an additional 10–22 % increase beyond the level implied by the current investment pipeline.

Hence, given all the above assumptions hold, under the business-as-usual (BAU) scenario, Europe's installed semiconductor manufacturing capacity is expected to reach at least 1.39 million wafers per month by 2030, and between 1.54 and 1.69 million by 2035.

1.3. EU positioning in the global value chain and EU value chain strength and resilience

The integrated circuit (IC) or chip is, in broad terms, an amalgamation of transistors, which can serve as either an electronically controlled switch or as a signal amplifier to perform a given function. Since the invention of the IC in the 1950s, a central driver of the semiconductor industry is the continuous push to increase the number of transistors that can be integrated onto a single chip, either through the classical approach of transistor miniaturisation or more recently through innovative packaging techniques such as chiplet architectures or three-dimensional integration.

This trend has been made possible by the division of the industry into highly specialised segments along the value chain, ranging from design and equipment manufacturing to fabrication, packaging and testing. No single region controls all stages and firms operate through complex, internationally dispersed networks that maximise expertise, efficiency and scale within complementary but independent production stages. In fact, the semiconductor industry is a direct result of globalisation, with a chip travelling over 50,000 km and crossing international borders over 70 times before reaching the end-customer ([27]). While globalisation and interdependence have

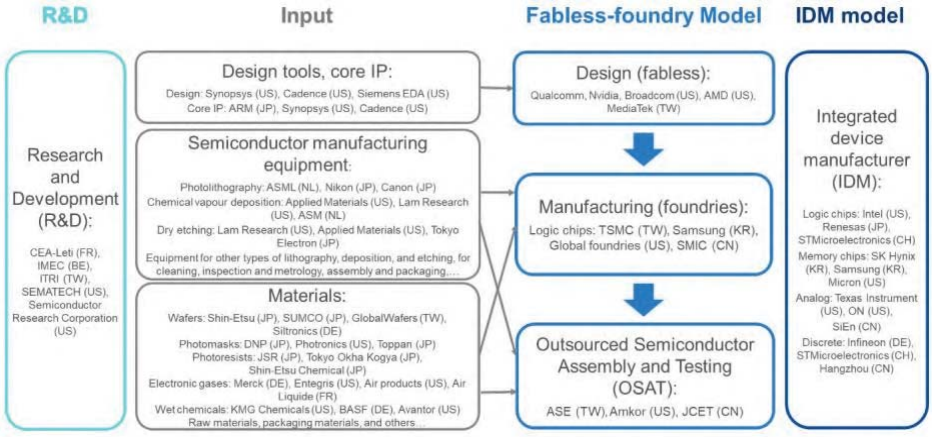
([27]) Chip Production's Ecological Footprint: Mapping Climate and Environmental Impact

enabled rapid innovation, they have also created structural vulnerabilities, as disruptions in any segment or geography can ripple across the entire ecosystem.

Figure 14 shows the many stages of semiconductor production, that go from manufacturing equipment, Intellectual Property (IP) to Electronic Design Automation (EDA) tools to raw materials to the design and manufacturing of semiconductors including final assembly, test and packaging.

The EU's position in the semiconductor value chain is strongest in upstream segments, particularly in manufacturing **equipment** and advanced **materials**. In lithography, ASML and its key suppliers, including Zeiss and Trumpf, form a globally indispensable cluster. The Union also hosts major players in back-end equipment such as Besi, EV Group, and SÜSS MicroTec, and is home to leading producers of specialty chemicals including BASF, Merck, and Solvay, alongside substrate manufacturers such as Siltronic and Soitec. The EU's **research** landscape further reinforces these strengths with institutions such as IMEC, CEA-Leti, Fraunhofer, VTT, Tyndall, and SAL contributing to advanced expertise across multiple semiconductor technology domains.

Figure 1 - Semiconductor supply chain and leader companies by segment ([28])



Source: JRC rearrangement based on the top firms listed in CSET (2021) on 2019 market share data; top manufacturers of wafers and fabless are from Statista[10] 2023; R&D listing is based on reported R&D centres in SIA (2016).

The EU also maintains a solid base of **integrated device manufacturers** (IDMs) that design and fabricate their own chips. Key firms include STMicroelectronics, Infineon, and NXP, followed by Bosch, ams-Osram, and Elmos. Although the EU accounted for around 8% of global wafer-fabrication capacity in 2023, its production is concentrated in relatively **mature nodes** for power electronics, microcontrollers, sensors, and other application-specific chips serving sectors such as automotive, industrial automation, and consumer appliances rather than in **leading-edge nodes**. The latter can be found in applications such as smartphones, high-performance computing, AI applications, 5G/6G infrastructure, or data centres. These advanced chips are almost all manufactured in Taiwan (for logic chips) and Korea (memory chips) ([29]). Since 2025, the US has

([28]) Cerutti, I. and Nardo, M., Semiconductors in the EU, Publications Office of the European Union, Luxembourg, 2023, doi:10.2760/038299, JRC133850.
([29]) https://www.oecd.org/content/dam/oecd/en/publications/reports/2025/12/the-chip-landscape_27ef5d87/02dbd028-en.pdf

secured its own leading-edge production capacity ([30]), with Japan expected to follow soon ([31]). This is primarily because leading-edge chips are concentrated in applications such as smartphones, high-performance computing, and data centres, sectors in which the EU has a relatively limited industrial footprint. Currently, **foundries** fabricating at the leading edge are largely based in Taiwan and South Korea, with the US ramping up its capacity. The EU has limited leading-edge capacity with Intel in Leixlip, Ireland, that is currently reserved for Intel's internal purposes and is not serving as an open foundry.

What remains limited in the EU is a comprehensive **chip design ecosystem** that includes both fabless design firms and large-scale foundries. Fabless companies, which design chips but outsource their manufacturing, generate roughly half of global chip revenues, yet the EU accounts for less than 1% of fabless revenues. The leading **software tools** and **IP** blocks needed to design chips are of US origin. The EU, lacking globally leading fabless "design houses" comparable to the major players in the US and Asia, misses the dense combination of big design firms and open foundries that underpins advanced chips leadership elsewhere.

As a result, the semiconductor value chain remains highly concentrated across a few global regions, and the EU's role, while critical upstream, depends on external partners for several downstream and high-volume manufacturing stages, including for AI chips. The US and several East Asian economies retain leading positions in chip design and leading-edge digital chip manufacturing, while Taiwan and South Korea account for the majority of global leading-edge wafer fabrication capacity. Japan remains a key supplier of essential materials and precision components. Assembly, packaging, and testing activities are largely concentrated in China and Southeast Asia, where significant high-volume back-end capacity has developed.

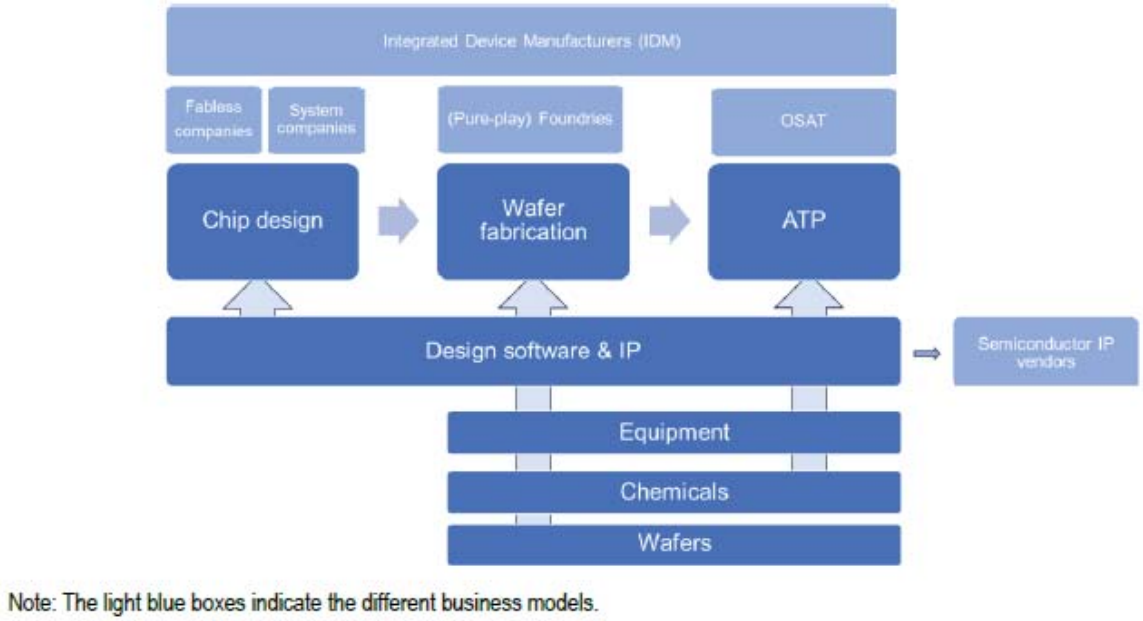
OECD (2025) ([32]) explains that the semiconductor (chips) value chain can be broadly structured into **three principal stages**: **design**, **wafer fabrication**, and **assembly, testing, and packaging (ATP)**. Each stage relies on specific inputs including wafers, manufacturing equipment, and specialised materials provided by dedicated suppliers, and all are characterised by a strong dependence on **research and development (R&D)** to sustain technological progress and competitiveness. The three stages can be further described as:

- **Chip design** is *skill- and research-intensive*, and increasingly capital-intensive, due to the significant cost of electronic design automation (EDA) tools, intellectual property (IP) blocks, verification environments and prototype testing. The complexity of state-of-the-art designs requires substantial upfront investment and contributes to high barriers to entry.
- **Wafer fabrication** (front-end manufacturing) is *capital-intensive*, requiring advanced equipment, cleanroom facilities, and economies of scale. It is also rooted in decades of accumulated experience and high R&D expenditure, which explains why the sector is highly concentrated and why catching up is particularly difficult for late entrants. Sustaining competitiveness at leading-edge process nodes requires continuous innovation, with firms such as Intel illustrating the challenges associated with keeping pace with rapid innovation cycles.

([30]) TSMC begins producing 4-nanometer chips in Arizona, Raimondo says | Reuters
([31]) Rapidus Achieves Significant Milestone at its State-of-the-Art Foundry with Prototyping of Leading-Edge 2nm GAA Transistors First prototypes successfully demonstrate electrical characteristics as the company continues to hit targets leading up to 2027 mass-production - Rapidus株式会社
([32]) OECD. (2025). *Mapping the semiconductor value chain: Working towards identifying dependencies and vulnerabilities* (OECD Science, Technology and Industry Policy Papers No. 182). OECD Publishing.

- **Assembly, Test, and Packaging (ATP)** (back-end manufacturing) is *labour-intensive* and less automated, providing lower added value compared to the first two stages. However, advances in heterogeneous integration and 2.5D/3D packaging have turned ATP into an important source of differentiation in performance, energy efficiency and miniaturisation. Moreover, advanced packaging requires close integration between front-end and back-end processes, reinforcing interdependencies across the value chain.

Figure 15. The Illustration of the chips value chain. *Source: OECD, 2025.*



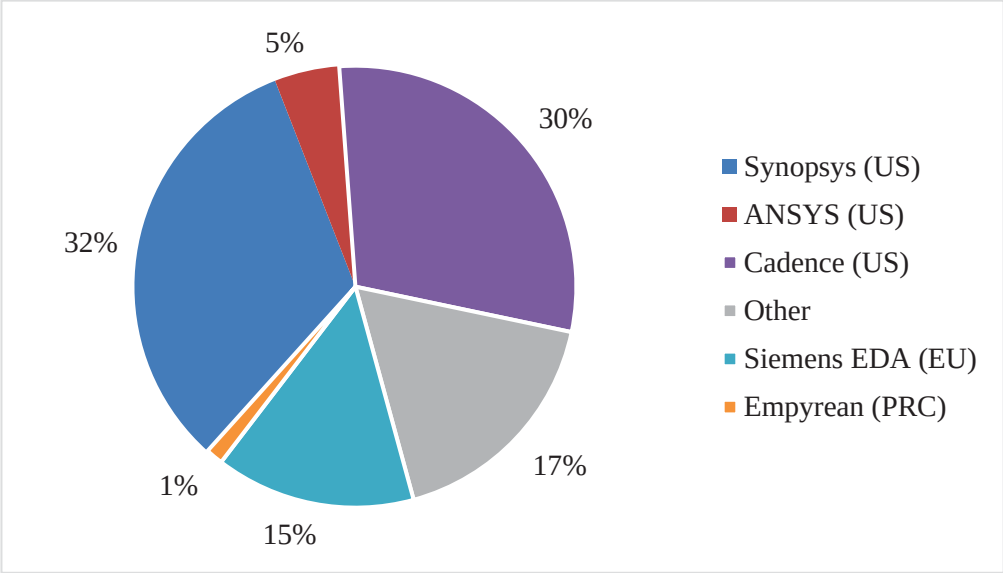
Note: The light blue boxes indicate the different business models.

As illustrated in the figure above, the principal value chain stages are supported by upstream segments such as chemicals and raw materials, wafers and substrates, and semiconductor manufacturing equipment. The produced and packaged chips are then ready for downstream integration and end-use applications.

1.3.1. Detailed analysis of semiconductor value chain

1.3.1.1 Electronic Design Automation

Figure 16. EDA vendors market share 2024 *Source: IDC*



Electronic Design Automation (EDA) tools are **the software tools used to design chips**. The EDA Market is dominated by three vendors i.e. Synopsys (US), Cadence (US), and Siemens EDA (EU). Data from 2024 shows that together they hold a market share north of 75%, the acquisition of Ansys by Synopsys in 2025 takes this up to 80%.([33])

Design automation software is not delivered as a single application but as an integrated suite of specialised tools that, taken together, constitute the end-to-end "design flow" required to develop an integrated circuit. This flow spans multiple stages and abstraction levels, including (i) front-end design and verification (RTL development, simulation, formal verification, and static checks), (ii) synthesis (translation of RTL into a gate-level netlist under timing, power and area constraints), (iii) physical implementation (floorplanning, placement, clock-tree synthesis, routing, and iterative optimisation), and (iv) sign-off analysis and physical verification (static timing analysis with extracted parasitics across Process, Voltage, Temperature (PVT) corners, signal-integrity analysis, power-integrity and reliability checks such as IR drop and electromigration, and rule-deck-based 'Design Rule Check'/'Layout versus Schematic'). The outputs of each stage are used as inputs to subsequent stages; as a result, effective operation depends on consistent constraints, compatible data models, and tight interoperability across tools. In practice, the design process is iterative rather than linear, with repeated loops between implementation and sign-off to resolve violations and converge on manufacturable results.

In practice, as attested by their market share, the three vendors exert total dominance over the Western semiconductor design tool market since the **remaining 20% is primarily** held by Empyrean Technology that is a China based EDA vendor. Empyrean targets Chinese companies

([33]) Market share also considers revenues generated from simulation software.

and is still catching up to the big three. Considering its Chinese ownership it also presents clear economic security risks and is not a viable substitute for the three main vendors.

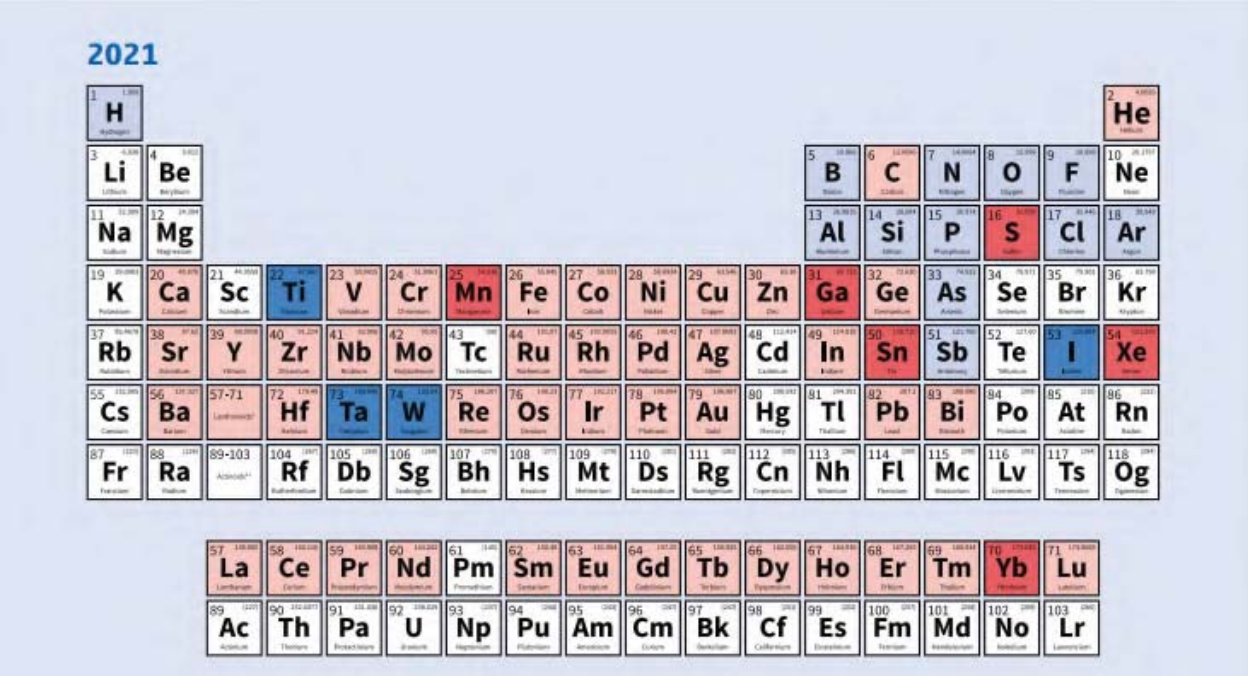
The rest of the market share is **split amongst smaller companies that cannot offer a complete suite of tools** for the development of chips, many of whom aspire to eventually be acquired by one of the big three. Some open-source alternatives are emerging, although these are not suitable for serious commercial chip designs and may only be reliably used for very mature technologies.

1.3.1.2 Materials

1.3.1.2.1 Critical raw materials

The raw materials required for semiconductor manufacturing span almost the entire periodic table and range from silicon, which is relatively abundant, to rare earth elements. According to analysis by ZVEI, over the last thirty years the number of elements used in the semiconductor industry has quadrupled. ([34])

Figure 17. Elements used in the semiconductor industry, where coloured elements denote use. *Source: ZVEI([35]).*



Key examples here include gallium (Ga) and germanium (Ge). These are metals that are not found naturally. They are instead formed, usually as a by-product of the refineries of other metals. Ge is formed as by-product of zinc and Ga is a by-product of processing bauxite and zinc ores.

([34]) Semiconductor-Strategy-for-Germany-and-Europe.pdf
([35]) Semiconductor-Strategy-for-Germany-and-Europe | ZVEI Light blue indicates elements in use in the 1980s; Dark blue indicates elements in use in the 1990s; Light red indicates elements in use in the 2000s; Dark red indicates elements in use in the 2010s.

35% of the gallium used in the EU is being refined in Germany, however raw gallium originates from China, which holds 94% of the world's production. ([36])

For **Gallium (Ga)** it is known that about 70% of the material imported to the EU is used to produce integrated circuits, 25% for lighting applications (mostly LED technology) and the rest for photovoltaic technology. In the US the shares of Ga consumption are similar (74% for ICs, the rest for LEDs and specific solar cells). However, increasingly Gallium is also being used in power electronics.

For **Germanium (Ge)** the main producer is China with 79% of world production followed by United States (16%) and United Kingdom (3%). The main uses of Germanium in the EU are infrared optics 52%, optical fibres 23% and satellite solar cells 12%. Ge supply appears to be less of an issue as diversification of sources is simpler compared to Gallium.

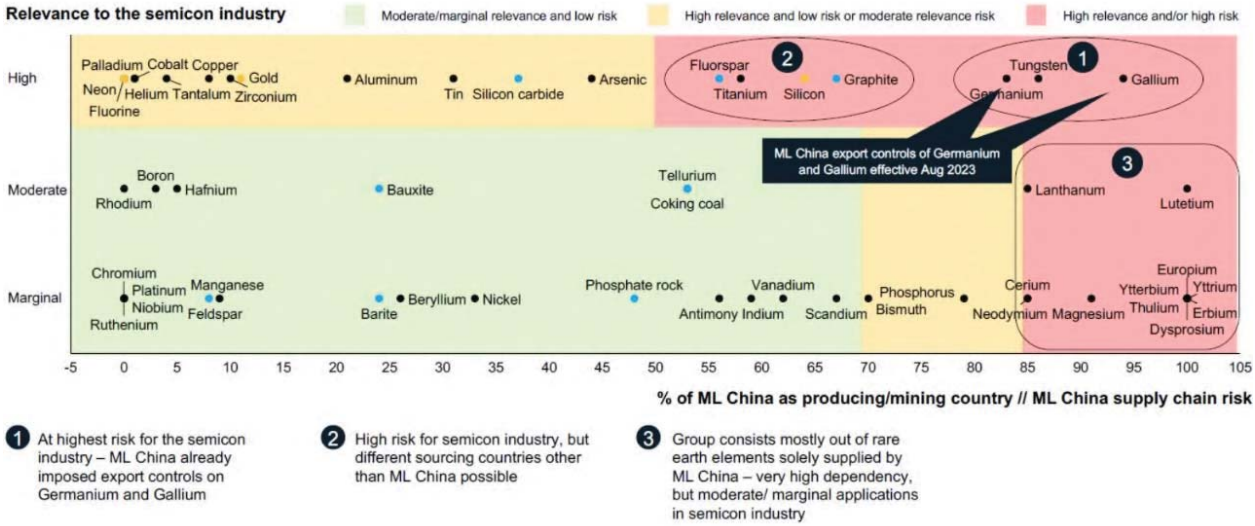
Gallium is used in the industry mainly to make **compound semiconductors,** crucial for RF, power and optoelectronics. Gallium Arsenide (GaAs) and Indium Gallium Arsenide (InGaAs) are some of the most widely used and researched III-V compound semiconductors. For example, **Gallium arsenide (GaAs)** is used for **high-frequency RF chips**, especially power amplifiers and low-noise components in wireless communications. **Gallium nitride (GaN)** is used for **high-power and high-voltage devices**, including power conversion (e.g., chargers, data-centre power supplies) and RF power devices (e.g., telecom infrastructure). Importantly, **GaN** is a potential substitute for **Silicon Carbide (SiC**) in next generation power devices. **Gallium-based optoelectronics** is used in **LEDs and laser diodes**, since these materials emit light efficiently.

Germanium is used in semiconductors mainly in three areas. For example, **SiGe (silicon–germanium) chips** are widely used for **high-frequency analogue/RF** (e.g., telecoms, radar, automotive sensing) since it improves transistor performance. Germanium is also crucial for **silicon photonics** and is used for **on-chip photodetectors** for fibre-optic wavelengths. Additionally, this compound has been used as growth material for transistors contacts since at least the 28nm technology node and as channel material for the 5nm node ([37]), making it a strategically critical element in leading edge technologies. Europe's Umicore is a large player in both Germanium and Gallium refining and recycling.

([36]) Cerutti, I., & Nardo, M. (2023). *Semiconductors in the EU: State of play, future trends and vulnerabilities of the semiconductor supply chain* (JRC133850, EUR 31625 EN). Luxembourg: Publications Office of the European Union. https://doi.org/10.2760/038299

([37]) The channel is the "active" part of a transistor and this was the first time a channel was not made in pure Silicon. https://fuse.wikichip.org/news/3398/tsmc-details-5-nm/

Figure 182. Critical raw materials in the semiconductor industry. *Source: McKinsey*



The examples of gallium and germanium are crucial since Chinese dominance over these materials have resulted in the introduction of export controls on gallium and germanium (and related compounds) from 1 August 2023, ([38]) requiring exporters to obtain licences. The measure is widely understood to be part of ongoing geopolitical rivalries and trade confrontation and is viewed as a response to the tightening of restrictions on China's access to advanced semiconductor manufacturing equipment and know-how, including lithography-related controls. These export controls have resulted in prices for these raw materials to increase by around 20%. ([39])

1.3.1.2.2 Compound semiconductor Substrates/Epiwafers

The compound semiconductor substrate supply chain is **highly concentrated and regionally segmented**, with leading players clustered in a small number of countries and individual firms specialising by material type.

The Yole Intelligence mapping of leading players worldwide in compound semiconductor substrates highlights that **Europe's visible footprint in substrates is relatively narrow**, with **Freiberger Compound Materials (EU)** identified for **GaAs** and **InP** substrate, both elements crucial for the photonics industry. A larger share of the global supplier base sits in **the United States** (e.g., **Wolfspeed, Coherent/II-VI, SK siltron CSS, AXT**) and **East Asia**, including **Japan** (e.g., **Sumitomo Electric, Resonac, SiCrystal (ROHM group), JX Nippon Mining & Metals**), **China** (e.g., **SICC, Tankeblue, Vital**), and **Taiwan** (e.g., **GlobalWafer**s, **Hermes-Epitek**). ([40])

However, Europe's exposure in SiC substrates is partially mitigated by the growing vertical integration of certain IDMs. In particular, **STMicroelectronics is building in-house SiC substrate capacity in Catania (Italy)** within its vertically integrated "Silicon Carbide Campus", supported by a **EUR 2 billion Italian state-aid measure approved under the EU Chips Act framework**. In addition, **onsemi is expanding SiC-related capacity at Rožnov (Czechia)**,

([38]) Yole, Status of the Compound Semiconductor Industry 2024
([39]) Yole, Status of the Compound Semiconductor Industry 2024
([40]) Yole, Status of the Compound Semiconductor Industry 2024

backed by a **€450 million Czech state-aid measure likewise approved in line with the objectives of the Chips Act**. ([41])

Therefore, while Europe does not have significant substrate suppliers, it has significant substrate manufacturing cability as part of vertically integrated IDMs.

The **epiwafer segment** sits immediately downstream of substrates. Here, suppliers take a base **substrate** (e.g., SiC, GaAs, InP, GaN-on-SiC) and grow **epitaxial layers** that determine device performance. This step is a critical dependency point since epitaxy is highly process-sensitive and qualification-heavy, making supplier switching slow and costly.

Based on Yole Intelligence's mapping of leading epiwafer players, the **EU's identifiable merchant epiwafer footprint** includes **Soitec (France)** and **Azur Space (Germany)**, alongside smaller specialised actors (e.g., **Allos** for uLED GaN-related activity). In contrast, a substantial portion of global capability is concentrated outside the EU, particularly in **Japan** (e.g., Sumitomo Electric and other major materials houses), **Taiwan** (a dense epiwafer ecosystem spanning several III–V platforms), **the United States** (e.g. Wolfspeed), and **China** (Enkris Semiconductor, Epiworld), with suppliers covering **SiC**, **GaN** variants (GaN-on-Si, GaN-on-SiC, GaN-on-sapphire), and **GaAs/InP** platforms. ([42])

1.3.1.3 Ultra-high-purity process gases and chemicals

1.3.1.3.1 Gases

Europe's semiconductor manufacturing ecosystem depends on a broad set of ultra-high-purity process gases and precursors that enable thin-film deposition, patterning (etch), doping, chamber cleaning, and surface/interface treatments, including lithography-support gases used for scanner/track purging and post-lithography resist processing. While several baseline gases remain manufactured within Europe, the EU is structurally dependent on external supply for many of the most critical electronics specialty gases. This dependency is significant because semiconductor production is serial and qualification-bound: the absence of a single qualified molecule at the required purity, packaging, and delivery specification can halt an entire process module and disrupt the operations of a whole fab.

1.3.1.3.1.1 Gases manufactured within Europe and principal functions

European production continues to cover a subset of widely used enabling gases, primarily supporting deposition, etch, and process conditioning. These include ammonia (NH_3) for nitride deposition and nitridation; chlorine (Cl_2) and hydrogen chloride (HCl) for etch, cleaning, and epitaxy process control; nitrous oxide (N_2O) and nitric oxide (NO) for oxide/oxynitride formation and interface engineering; and sulphur hexafluoride (SF_6) for silicon etch (including isotropic and MEMS applications). In addition, certain hydrocarbons (CH_4, C_2H_4, C_3H_8, C_3H_6) are used as carbon sources for specialised films (e.g., hardmasks and carbon-doped layers), while CO and SO_2 may appear in niche plasma or surface-chemistry contexts. Overall, domestic availability exists for several important gases; however, these are often comparatively standardised and, in many cases, less distinctive for advanced-node capability than gasses for dopants, high-value deposition precursors, and critical etch/clean.

([41]) Commission approves €450 million Czech State aid for Onsemi's new semiconductor manufacturing facili
([42]) Yole, Status of the Compound Semiconductor Industry 2024

1.3.1.3.1.2 Gases predominantly sourced from outside Europe and principal functions

Europe's most material external dependencies are concentrated on molecules that are tightly coupled to transistor formation, materials integration, and equipment availability:

- Dopant gases and diffusion sources: arsine (AsH_3), phosphine (PH_3), diborane (B_2H_6) and related boron chemistries (BBr_3, BF_3), as well as $POCl_3$, underpin formation of n-type and p-type regions and diffusion processes. ([43]) These inputs are not readily substitutable; alternative sourcing typically requires extensive requalification and may present yield and reliability risk.
- Deposition precursors: silane (SiH_4), ([44]) disilane (Si_2H_6), chlorosilanes (DCS/TCS) and $SiCl_4$, tetraethyl orthosilicate (TEOS), trimethylsilane (TMS), germane (GeH_4) and WF_6 enable deposition of key silicon, dielectric, SiGe/Ge, and tungsten films. Disruption can halt deposition modules and create cascading effects on work-in-progress wafers and cycle time.
- Etch and chamber-clean gases: HF (oxide removal), HBr (anisotropic silicon/polysilicon etch), NF_3 (remote plasma cleaning), F_2/ClF_3 (aggressive cleaning/fluorination), and multiple fluorocarbon/PFC/HFC gases (e.g., CF_4, CHF_3, C_2F_6, C_3F_8, C_4F_8, C_4F_6, C_5F_8, CH_3F, CH_2F_2) are essential for pattern transfer, selectivity/profile control, and maintaining tool uptime.
- Reliability/passivation inputs: deuterium (D_2) supports selected passivation and anneal processes; substitutability constraints may manifest through yield or reliability qualification impacts even where immediate production continues.

Furthermore, when considering the upstream sources of these gases, more than 50% of the Union's electronics speciality gases are heavily dependent on China.

1.3.1.3.1.3 Structural characteristics of the dependency

These dependencies are amplified by: (i) the serial nature of wafer fabrication (a blocked step halts downstream processing); (ii) qualification constraints (purity, impurity profile, packaging, and delivery stability are part of the specification);([45]) and (iii) limited substitutability, particularly for dopants and advanced deposition precursors;

External dependence for dopants, critical deposition precursors, and etch/clean chemistries, combined with qualification-bound production, creates a high risk profile. Even where Europe retains domestic production of several baseline gases, disruption affecting externally sourced molecules on the critical path is likely to result in discontinued outcomes: module stoppages, tool downtime, cycle-time extension, and potential yield degradation, with cascading effects across the European semiconductor value chain and downstream industrial users.

([43]) Chemicals Used in the Electronics Industry | OECD
([44]) Silane | Air Liquide
([45]) For semiconductor process gases, the applicable specification extends well beyond a nominal purity value (for example, 99.9999%). In practice, device manufacturers and equipment suppliers jointly qualify the gas as an integrated package, encompassing its detailed impurity profile, cylinder and valve materials, packaging configuration, and the performance of the associated delivery hardware. Any change in supplier, production site, or even cylinder type typically necessitates requalification, a process that can require several weeks to months and entails significant engineering effort and test-wafer consumption.

1.3.1.3.2 Chemicals

Semiconductor fabs rely on ultra-high-purity chemicals at every step, including cleaning acids (hydrofluoric acid, hydrochloric acid, sulphuric acid), bases (ammonium hydroxide), oxidisers (hydrogen peroxide), solvents (isopropyl alcohol), etch and deposition chemistries, and Chemical-Mechanical Planarisation (CMP) slurries used to polish wafers between layers. These inputs must meet tight purity specifications and are qualified to specific tools and recipes, therefore shortages or quality issues can halt production and are not quickly solved by switching supplier.

This section will focus on photoresists since these chemicals are a pronounced dependency. This is due to the fact that the supply base for high-end resists is very concentrated and switching costs are higher, with requalification often required and limited near-term alternatives are available once a process is determined. Polysilicon and precursor chemicals will also be considered.

1.3.1.3.2.1 Photoresist

Photoresist is a critical input to semiconductor photolithography. It is the chemically active film that receives the circuit pattern during lithographic exposure (DUV/EUV), enabling selective development, etching, and subsequent pattern transfer to the wafer. While lithography tools and masks are high-profile assets, photoresist performance directly governs pattern quality, throughput, and ultimately yield. Any sustained disruption in photoresist supply can therefore halt wafer output in fabs.

This dependency is amplified by stringent performance and integration requirements. Photoresists must be highly sensitive at the relevant wavelength to support acceptable scanner throughput, form uniform films with strong adhesion, and remain mechanically and chemically stable through downstream steps (etch, cleans, stripping). These materials are typically co-developed and qualified with fabs for specific process windows, tool settings, and patterning stacks. Once qualified for high-volume manufacturing, changing resist formulations or suppliers can trigger lengthy requalification and yield risk, creating high switching costs and practical vendor lock-in.

The supply base is highly concentrated, with Japanese suppliers holding an estimated ~90% share, notably JSR and Tokyo Ohka Kogyo (TOK). [46] This market structure increases systemic exposure to disruptions affecting a small set of producers (manufacturing incidents, quality excursions, logistics interruptions) and heightens sensitivity to policy or geopolitical events. The 2019 Japan–South Korea export licensing changes affecting certain semiconductor chemicals, including EUV photoresist, illustrate how regulatory actions can translate into near-term supply uncertainty for dependent manufacturing regions.([47]) Even where alternative sourcing exists, substitution is constrained by qualification timelines and by extreme purity requirements, where trace contamination can produce unacceptable defect rates and shipment rejections.

Although strategically significant, as attested by the acquisition of JSR by Japan's state-backed fund JIC, ([48]) the photoresist sector is comparatively small and specialised, requiring sustained R&D and high-purity manufacturing capabilities. This combination of high technical barriers,

([46]) Japan - Semiconductors | U.S. International Trade Administration
([47]) The South Korea-Japan Trade Dispute in Context: Semiconductor Manufacturing, Chemicals, and Concentrated Supply Chains | U.S. International Trade Commission
([48]) Japan-backed fund to buy chip materials maker JSR for $6.4 billion | Reuters

concentrated incumbency, and tight fab integration suggests persistent dependency risk, particularly for leading-edge nodes and EUV processes.

1.3.1.3.2.2 Polysilicon

High-purity polysilicon serves as feedstock for production of silicon wafers. Stringent purity requirements exist in order to ensure that resultant wafers have no deformities or impurities that would inhibit the function and performance of fabricated chips.

Today's polysilicon market is bifurcated. The vast majority (>90%) is manufactured to support relatively lower purity photovoltaic (PV) applications. The PV segment is dominated by Chinese suppliers.

That contrasts with electronic- or semiconductor-grade (EG) polysilicon, which has been historically produced outside of China at a more even supply-demand balance. In the EG segment, Germany's Wacker Chemie ("Wacker") is a market leader, alongside other key players from the U.S., Japan, and South Korea.

Additionally, the input material required to produce both PV and EG polysilicon is metallurgical-grade silicon (MG-Si), for which global supply is heavily dependent on China.

1.3.1.3.2.3 Precursors

Precursors are complex molecules used in Atomic Layer Deposition (ALD) and Chemical Vapor Deposition (CVD), which enable the atomic-scale precision essential for fabricating transistors, interconnects, and memory structures in advanced chips. They represent one of the most knowledge-intensive, high-value segments of the semiconductor materials chain, and their production requires deep expertise in molecular design, purification, and process integration.

The global precursor market, though modest in size at around USD 1.7 billion in annual revenues in 2024, is strategically critical and growing rapidly. The market is projected to exceed USD 2.5 billion by 2029, a 47% increase from 2024,([49]) driven by demand for advanced logic and 3D memory chips, and by the use of new materials such as cobalt, ruthenium, molybdenum, and ferroelectric high-k dielectrics. Metal and metal oxide precursors account for most of this growth, while dielectric and low-k materials are projected to remain large and stable segments.

The EU holds a globally leading position in the precursor market through its chemical champions Merck (Germany) and Air Liquide (France). These two companies together command over half of global market share in advanced precursors. Their strengths lie in chemical synthesis, purification, and integration with process equipment and fabs. Supporting firms such as BASF (Germany), Solvay (Belgium), Evonik (Germany), Umicore (Belgium) and DOCK Chemicals (Germany) complement this leadership through the development of specialised chemistries and R&D collaboration. These capabilities, backed by Europe's strong research ecosystem, make the region a cornerstone of global innovation in ALD and CVD materials. On the other hand, Chinese firms such as Huate Gas, Nata Opto, and Jingrui are rapidly scaling capacity.

([49])The Outlook For The Precursor Market Remains Strong | Semiconductor Digest

1.3.1.4 Manufactured inputs

1.3.1.4.1 Front-end manufacturing

1.3.1.4.1.1 Masks

Photomasks are **design-specific and critical input** to wafer fabrication: each product and process node requires a dedicated mask set, and delays in mask availability can directly gate tape-out schedules and production ramps. The supply base is structurally split between **captive production** (masks made in-house by leading foundries/IDMs) and the **merchant market** (external mask shops). Market analysis indicates that captive production increased from **35% - 65% of the global photomask market** between **2008 and 2020**, implying that firms without captive capability are increasingly reliant on a relatively smaller merchant capacity pool, which can tighten during upcycles. ([50])

In the merchant segment, key suppliers include **Tekscend Photomask (Japan)**, **Dai Nippon Printing, DNP (Japan)**, **Photronics (United States)**, **SK-Electronics (Japan)**, and **Taiwan Mask Corporation, TMC (Taiwan)**. While no E headquartered companies are in this market, Tekscend has a production facility in Dresden that supplies leading-edge photomasks including for EUV lithography.

Upstream of mask shops, supply is further concentrated in **EUV mask blanks**, where a recent market summary reports that the top two manufacturers, **AGC (Japan)** and **HOYA (Japan)**, account for **around 93%** of the market, creating an additional dependency that can propagate into mask availability even where mask-making capacity exists. ([51])

1.3.1.4.2 Advanced packaging

1.3.1.4.2.1 T-Glass

Nittobo's **T-glass** is a specialised glass cloth used in the **package substrates** that support and connect advanced chips (the "carrier" that links the silicon to the rest of the device). Its purpose is to improve **dimensional stability under heat**, which helps reduce substrate warpage and supports manufacturing yields and reliability in large, high-power packages.([52]) Nittobo explicitly positions this material as crucial for **semiconductor package substrates** used in **high-performance CPUs** and **AI semiconductors**, and also links it to **communications ASICs and switches**, making it relevant to data-centre compute and high-speed networking supply chains. ([53]) From a resilience perspective, the key impact driver is **market concentration**: industry reporting places Nittobo at **around 90% market share** in the relevant semiconductor-materials glass fibre cloth segment (often referenced specifically as low-CTE/T-glass), indicating limited redundancy and a heightened risk of bottlenecks if capacity, logistics, or qualification timelines are disrupted. ([54])

1.3.1.4.2.2 Dielectric polymer film

When it comes to dielectric polymer film, a key insulating material used in CPUs and GPUs, 95% of supply is dependent on one manufacturer in Japan, Ajinomoto, with its Ajinomoto Build-up

([50]) EUV mask technologies: evolution and ecosystem for devices
([51]) ASML Holding Before Q4 Earnings: How Should Investors Play the Stock?
([52]) A Critical AI Niche Is Dominated by One Little-Known Japanese Company - WSJ
([53]) https://www.nittobo.co.jp/eng/business/electronicmaterials/index.htm
([54]) https://www.digitimes.com/news/a20260204PD225/nittobo-nikkei-2028-launch-materials.html

Film (ABF). ([55]) This film is used in **build-up package substrates** that sit between the silicon die (e.g., CPU/GPU) and the printed circuit board, enabling the dense multilayer wiring and microvia structures needed to route signals from nanometre-scale on-chip circuitry to millimetre-scale system interconnects. ([56])

1.3.1.5 Manufacturing equipment ([57])

The manufacturing process for a chip is equipment intensive and as is the case across the semiconductor value chain, the equipment ecosystem is fragmented and highly specialised. For the purpose of simplicity, this analysis will group the equipment market in two - front-end and back-end manufacturing.

Front-end manufacturing (FEOL/BEOL wafer fabrication) comprises the processes used to form semiconductor devices and interconnect structures on a silicon wafer, including transistor formation, dielectric and metal layer deposition, patterning, etching, and planarisation. **Back-end manufacturing** (assembly, packaging, and test) comprises post-fabrication operations that separate the wafer into individual dies and integrate each die into a package, including die attach, electrical interconnection (e.g., wire bond or flip-chip), encapsulation, thermal/mechanical integration, and final electrical test.

1.3.1.5.1 Front end equipment

When it comes to front-end equipment, the EU's most significant lever is **lithography (approx.. 92%)**. This is a strong position in a critical process step, but it is also highly concentrated in one segment. In contrast, **front-end wafer-fab equipment as a whole** is led by the **United States** with a market share of approximately 40%, followed by **Japan** at approximately 28% and **Korea** at 24%, with the EU remaining in **single digits**.([58]) This distribution indicates that Europe's influence over upstream manufacturing capacity is not commensurate with its lithography strength.

1.3.1.5.1.1 Deposition

Deposition equipment comprises chemical vapour deposition (CVD) and plasma-enhanced CVD for dielectrics and spacers, physical vapour deposition (PVD, sputter) for metals and liners, atomic layer deposition (ALD) for ultra-thin conformal films (including high-k and barriers), and, in advanced FEOL, epitaxy reactors for selective Si/SiGe growth. Here, the leading vendors are primarily non-European, notably Applied Materials (US), Tokyo Electron (JP) and LAM (US), with a significant European position in ALD through ASM (NL).

In 2023, the deposition equipment market totalled USD 23.1bn in sales and was dominated by Applied Materials (US) at 54% market share and Lam Research (US) at 14%, Tokyo Electron at 13% and ASM (NL) at 10% representing the most significant EU position in this sub-segment. [(59)]

([55]) Ajinomoto pledges to invest millions to produce material that's vital to semiconductor packaging | TechRadar
([56]) Ajinomoto Build-up Film (ABF) | Innovation Story | Innovation | The Ajinomoto Group Global Website - Eat Well, Live Well.
([57]) Bonnet, P., Ciani, A., Molnar, J., & Nardo, M. (2025). EU's strengths and weaknesses in the global semiconductor sector (JRC141323, EUR 40253). Luxembourg: Publications Office of the European Union. https://doi.org/10.2760/6302476
([58]) Bonnet, P., Ciani, A., Molnar, J., & Nardo, M. (2025). EU's strengths and weaknesses in the global semiconductor sector (JRC141323, EUR 40253). Luxembourg: Publications Office of the European Union. https://doi.org/10.2760/6302476
([59]) Bonnet, P., Ciani, A., Molnar, J., & Nardo, M. (2025). EU's strengths and weaknesses in the global semiconductor sector (JRC141323, EUR 40253). Luxembourg: Publications Office of the European Union. https://doi.org/10.2760/6302476

1.3.1.5.1.2 Lithography

Lithography is the manufacturing step that transfers a circuit pattern onto a silicon wafer. A photomask contains the pattern for one layer. The wafer is coated with a light-sensitive film (photoresist), then a lithography tool projects light through the reticle to expose the resist. The wafer is developed so parts of the resist are removed, leaving a temporary patterned layer that acts as a stencil.

Lithography combines the exposure tool (i.e. optical exposure) with resist processing (coater/developer tracks) to transfer mask patterns into photoresist, which subsequently guides etch or implant.

In 2023, lithography sales were at USD 25.1bn and were overwhelmingly concentrated in ASML (NL) with a 92% market share, with small EU shares held by SUSS MicroTec (DE, 0.5%) and EV Group (AT, 0.2%). Within the Extreme Ultraviolet (EUV) segment, required for the most leading-edge chips, ASML holds 100% market share, with Canon (JP) and Nikon (JP) being competitors in Deep Ultraviolet (DUV) machines.

Resist processing equipment sales in 2023 were USD 3.4bn and were highly concentrated in Tokyo Electron (JP) with a market share of 92%, with SUSS MicroTec (DE) the only EU player with a measurable share of 2.3%.

1.3.1.5.1.3 Etch

Etch is the manufacturing step that selectively removes material from the wafer to transfer a pattern into an underlying layer. After lithography creates a patterned photoresist “stencil”, etch removes exposed regions of a target film (or silicon) while protected regions remain, thereby forming features such as trenches, holes, and device structures.

Etch is performed using either dry (plasma) etching, which offers high precision and vertical sidewalls, or wet chemical etching, which is used where high selectivity is required. Etch is critical because it determines the shape and dimensions of features and must stop accurately on the intended layer to avoid defects and yield loss.

The dry processing segment reached USD 15.6bn in 2023, with market leadership held by Lam Research (US) with a market share of 44.5%, followed by Tokyo Electron (JP) with a market share of 21% and Applied Materials (US) with a market share of 18%. EU presence was marginal (for example PVA TePla (DE) with a marginal market share of 0.3%).

When it comes to wet wafer processing systems, sales were USD 6.0bn in 2023, led by SCREEN (JP) with a market share of 35%, Tokyo Electron (JP) with a market share of 21% and Lam Research (US) with a market share of 16%. EU suppliers in this segment have a small market share with for example Siconnex (AT) at 0.3% of etch revenues and 0.1% market share for RENA (DE).

1.3.1.5.1.4 Clean

Clean is the manufacturing step that removes contamination and process residues from the wafer to prevent defects and enable reliable subsequent processing. It is used throughout FEOL and BEOL, including after lithography and etch (to remove photoresist and etch by-products), before deposition (to prepare surfaces), and after CMP (to remove slurry particles).

Cleaning is carried out using wet chemical processes (on batch wet benches or single-wafer tools) and, where needed, dry cleaning/ashing (often plasma-based) for resist and organic removal. Clean is yield-critical because microscopic particles or residual films can cause shorts, opens, poor adhesion, or increased leakage.

In the wet processing segment, 2023 market share data indicate the predominant role of Japanese suppliers. Here, SCREEN (JP) leads with a market share of 35%, followed by Tokyo Electron (JP) with market share of 21% and to a lesser extent by Lam (US) with a market share of 16%. In this segment EU suppliers (Siconnex (AT), RENA (DE), SEMYSCO (DE)) are present but play a relatively minor role.

When it comes to dry processing, LAM (US) in 2023 a market share of 44.5%, Tokyo Electron (JP) had a market share of 21% and Applied Materials (US) at 18%.

1.3.1.5.1.5 Metrology and inspection

Metrology and inspection are the manufacturing activities that measure features on a wafer and detect defects so the process can be controlled, and yield can be maintained.

The market for this segment amounted to USD 10.3bn in 2023 and was highly concentrated in KLA (US) with a market share of 60% and Applied Materials (US) at 12%, with EU suppliers holding smaller but relevant shares, including ASML (NL) with a market share of 6%, Bruker AXS (DE, 1%) and Semilab (HU, 1%).

For reticle inspection and repair (a critical enabler for lithography yield), the 2023 market was led by Lasertec (JP) with 50% market and KLA (US) with 43% market share. Zeiss (DE) accounts for a 5% market share and represents the principal EU presence in this segment

1.3.1.5.1.6 Planarisation

Planarisation is the process of flattening the wafer surface to ensure subsequent lithography and layer integration remain within focus and uniformity tolerances. In semiconductor manufacturing it is implemented primarily through chemical mechanical planarisation (CMP), which removes material using a combination of chemical reactions and mechanical polishing to restore a controlled, planar surface.

CMP equipment sales were USD 2.7bn in 2023 and were concentrated in Applied Materials (US) with a market share of 56% and Ebara (JP) at 30%, with no EU supplier reported as having a material global share in this segment.

1.3.1.5.2 Back-end

Assembly and packaging are the final steps in turning finished wafers into packaged chips and boards for end users. Assembly typically includes **wafer dicing and thinning**, **bonding and interconnect**, **moulding and sealing** (**encapsulation)**, **inspection and handling** and **test equipment**. Packaging provides the electrical connections needed for signal transmission, power

delivery, and voltage regulation, while also managing heat dissipation and providing the physical protection required for long-term reliability. ([60]).

In 2023, Japan accounted for 48% of the global market (up from 33% in 2017) and recorded the highest compound annual growth rate (15%) among the leading countries during the COVID-19 period and its aftermath. Japan also held a dominant position in dicing equipment, controlling over 92% of the market in 2023. In packaging equipment, Japan captured 51.4% of the global market in 2023, increasing to 75.3% in moulding and sealing systems.[61] Singapore's global market share declined to 21% in 2023 (from 35% in 2017), reflecting its concentrated specialisation in bonding equipment, particularly wire bonding. In 2023, Singapore accounted for over 81% of global wire bonding sales (up from 7 5% in 2017). Singapore also held an effective monopoly in integrated assembly systems, with a 97% market share in 2023; the remaining 3% was held by Grohmann Engineering (DE). [62]

In 2023, the European Union held 14.5% of the global market for assembly and packaging equipment, down from 16% in 2017. The EU had limited to no presence in the dicing and assembly equipment segments. However, it maintained a significant position in bonding equipment, holding 26% of the global market in 2023, driven in particular by die attaching, where the EU's market share reached 43%. The EU was also a leading supplier in lead-finishing and marking systems, together with the Republic of Korea, jointly accounting for 34% of the global market in 2023. Finally, in moulding and sealing systems, the EU held 13% of the global market in 2023, ranking second to Japan. ([63])

1.3.1.5.2.1 Wafer dicing and thinning

Wafer dicing is the process of separating the wafer into individual dies after wafer processing. It is executed by blade sawing or laser dicing, depending on materials and edge-quality requirements. Wafer thinning is the process of reducing wafer thickness to meet packaging requirements. It is performed primarily by backside grinding, often followed by polishing or stress-relief treatments, with the wafer supported on a carrier to prevent mechanical damage.

In dicing and wafer thinning, dependence is structurally high. In 2023, DISCO (JP) has a market share of 83% in blade sawing. In laser sawing, DISCO (JP) has a market share of 78% and ACCRETECH/Tokyo Seimitsu (JP) has a market share of 14%. Backside grinding is similarly concentrated, with DISCO (JP) having a market share of 86%, while European participation is limited - for example G&N (DE) has a market share of 1.2%.

1.3.1.5.2.2 Bonding and interconnect

Bonding and interconnect equipment comprises the tools used to attach the semiconductor die to a package substrate and create the electrical connections between the die and the package.

([60]) Bonnet, P., Ciani, A., Molnar, J., & Nardo, M. (2025). EU's strengths and weaknesses in the global semiconductor sector (JRC141323, EUR 40253). Luxembourg: Publications Office of the European Union. https://doi.org/10.2760/6302476
([61]) Bonnet, P., Ciani, A., Molnar, J., & Nardo, M. (2025). EU's strengths and weaknesses in the global semiconductor sector (JRC141323, EUR 40253). Luxembourg: Publications Office of the European Union. https://doi.org/10.2760/6302476
([62]) Bonnet, P., Ciani, A., Molnar, J., & Nardo, M. (2025). EU's strengths and weaknesses in the global semiconductor sector (JRC141323, EUR 40253). Luxembourg: Publications Office of the European Union. https://doi.org/10.2760/6302476
([63]) Bonnet, P., Ciani, A., Molnar, J., & Nardo, M. (2025). EU's strengths and weaknesses in the global semiconductor sector (JRC141323, EUR 40253). Luxembourg: Publications Office of the European Union. https://doi.org/10.2760/6302476

Here, Europe's strongest position is in die attach (die attaching equipment). BESI (NL) has a global market share of 43% in 2023, followed by ASMPT (SG) with a market share of 21%. This concentration implies that a meaningful portion of global die attach capability is European-origin. However, Europe's position weakens in wire bonding. Kulicke & Soffa (SG) has a market share of 53% and ASMPT (SG) has a market share of 29%, while German suppliers Hesse (DE) has a market share of 5% and F&K Delvotec (DE) has a market share of 2%.

1.3.1.5.2.3 Moulding, sealing and finishing

Moulding, sealing and finishing equipment comprises the tools used to encapsulate and complete packaged semiconductor devices after the die has been attached and electrically connected.

In this segment, the dependency is again concentrated outside Europe. TOWA (JP) has a market share of 61% in moulding and sealing systems and APIC Yamada (JP) has a market share of 14%, while BESI (BE) has a market share of 13%, indicating a meaningful European position. In lead finishing and marking, BESI (BE) has a market share of 32%, alongside EO Technics (KR) with a market share of 26%. Smaller European presences include ROFIN (DE) with a market share of 1.3% and PacTech (DE) with a market share of 0.6%.

1.3.1.5.2.4 Inspection and handling

Inspection and handling equipment comprises the tools used to detect defects and manage product movement through packaging and test operations.

In this segment, the equipment ecosystem shows mixed dependency with only minor European footholds. In wafer-level packaging inspection systems, Onto Innovation (US) has a market share of 42%, Camtek (IL) has a market share of 28%, and KLA (US) has a market share of 27%, while Unity SC (FR) has a market share of 3%. In package handling equipment, Cohu (US) has a market share of 27% and Pentamaster (MY) has a market share of 10%. Europe is represented by SPEA (IT) with a market share of 3.2%, alongside marginal shares for German suppliers.

1.3.1.5.2.5 Test equipment

Test equipment comprises the tools used to verify that semiconductor devices meet electrical performance and reliability requirements before shipment and, in some cases, during intermediate production stages.

In test equipment, Europe's presence is concentrated in specific niches rather than the largest-volume segments. For system-on-chip test systems, Advantest (JP) has a market share of 59% and Teradyne (US) has a market share of 31%, while SPEA (IT) has a market share of 1.5%. In burn-in test systems, European suppliers have more material positions: ELES (IT) has a market share of 5% and EDA Industries (IT) has a market share of 1.5%.

In handlers and probers (including wafer probing), leadership is again non-European, with ACCRETECH/Tokyo Seimitsu (JP) having a market share of 43% and Tokyo Electron (JP) having a market share of 29%.

1.3.2. Establishing a starting point for BAU scenario

a) Upstream segments

Table 6. Mapping of the upstream segments in the chips value chain. *Source: compiled by the authors.*

GVC segment	Value added characteristics	EU strengths	EU gaps	EU share in the global market	Chips Act relevance
IP **EDA**	Low-to-moderate capital intensity, very high R&D intensity. Value created through innovation, IP, and system integration. Profit margins typically 20–40%, driven by IP licensing and high switching costs.	One of the 3 EDA market leaders, Mentor Graphics, has been acquired by Siemens EDA, reducing EU's overdependence on US software tools ([64]), ([65])	The EU is dependent on the US, the UK, and Japan for Intellectual Property (IP) providers, which are vital for semiconductor design, with companies such as Cadence, Synopsys, or ARM being prominent in this area ([66]). Many EU companies rely on Cadence and Synopsys due to long-term engagements and the significant costs and delays associated with switching EDA suppliers ([67]).	EU27 share of the global semiconductor EDA market in 2023: 20.6 % ([68]) EU27 share of the global semiconductor IP/licensing market in 2023: 0 % (the EU27 currently has no market share in this segment; the leading player is ARM in the United Kingdom). ([69])	Pillar I: European Design Platform enables fabless SMEs and start-ups to design chips without incurring high software licensing costs. Offers collaborative prototyping environments. Competence Centres give fabless firms practical support, technical advice, and networking with foundries or integrators. Pilot Lines allow fabless companies to validate and prototype their designs on

([64]) DECISION Études & Conseil. (2024). *Economic analysis of the EU and global chips ecosystem*
([65]) Ebrahimi, A. (2024). *Groundbreaking chip sovereignty: Europe's strategic push in the semiconductor race.* Ifri Memos, Institut français des relations internationales (IFRI). ISBN 979-10-373-0874-0.
([66]) DECISION Études & Conseil. (2024). *Economic analysis of the EU and global chips ecosystem*
([67]) DECISION Études & Conseil. (2024). *Economic analysis of the EU and global chips ecosystem*
([68]) IDC (2025). Semiconductors D3: Second interim study report (Version 3.0). Prepared for the European Commission.
([69]) IDC. (2025). Semiconductors D3: Second interim study report (Version 3.0)

GVC segment	Value added characteristics	EU strengths	EU gaps	EU share in the global market	Chips Act relevance
					European technology nodes Chips Fund (EIB/EIF instrument) provides access to capital for fabless start-ups, which often face large funding gaps in the design-to-tape-out stage. Also indirectly related to Pillar II and Pillar III.

GVC segment	Value added characteristics	EU strengths	EU gaps	EU share in the global market	Chips Act relevance
Chemicals and raw materials	High technological barriers, stringent purity standards. Relatively **moderate profit margins (10–15%),** but materials quality (e.g. purity) critically determines chip yield and performance.	The EU holds a competitive edge in the supply of gases and chemicals necessary for advanced semiconductor manufacturing processes including etching and cleaning chemicals, fluorinated process gases, and CMP slurries. European suppliers are global leaders in several of these segments, underscoring chemicals as a core and indispensable strength of the EU ecosystem. ([70]) The EU has significant domestic capacity for ultra-purified silicon, which is the most widely used material for producing silicon wafers, and is a net exporter of this material ([71])	Raw materials essential for semiconductor production are scarce and not necessarily extracted or produced within the EU, leading to heavy reliance on foreign imports ([72]) The EU is reliant on critical materials like gallium, with 35% of the gallium used in the EU being refined in Germany from raw gallium originating in China, which holds 98% of the world's production ([73])	The EU benefits from a strong industrial ecosystem, with leading players such as Merck, Air Liquide, BASF, Umicore, Atlas Copco (including Edwards Vacuum), and Linde. These EU players accounted for EUR 12 billion in sales on the global semiconductor materials market in 2021, representing a 24% market share ([75])	Linked to Pillar III*:* Tracking of raw material dependencies and activation of emergency mechanisms.

([70]) DECISION Études & Conseil. (2024). *Economic analysis of the EU and global chips ecosystem.* Study for the European Commission, Directorate-General for Communications Networks, Content and Technology (DG CNECT).
([71]) Bonnet, P., Ciani, A., Molnar, J., & Nardo, M. (2025). *EU's strengths and weaknesses in the global semiconductor sector* (JRC141323, EUR 40253). Luxembourg: Publications Office of the European Union. https://doi.org/10.2760/6302476
([72]) European Court of Auditors. (2025). *The EU's strategy for microchips: Reasonable progress in its implementation, but the Chips Act is very unlikely to be sufficient to reach the overly ambitious Digital Decade target* (Special Report No. 12/2025). Publications Office of the European Union. https://www.eca.europa.eu/en/publications/SR-2025-12
([73]) Cerutti, I., & Nardo, M. (2023). *Semiconductors in the EU: State of play, future trends and vulnerabilities of the semiconductor supply chain* (JRC133850, EUR 31625 EN). Luxembourg: Publications Office of the European Union. https://doi.org/10.2760/038299
([75]) DECISION Études & Conseil. (2024). *Economic analysis of the EU and global chips ecosystem.*

GVC segment	Value added characteristics	EU strengths	EU gaps	EU share in the global market	Chips Act relevance
	Strategic sensitivity: supply chains concentrated in East Asia and the US; Europe is vulnerable in **raw material extraction and refining,** yet it holds strong and often market-leading positions in high-purity chemicals and specialty gases, which are indispensable for global semiconductor production.		The EU faces potential foreign dependencies and risks of import disruption for other input products related to front-end manufacturing processes, including Bromine (with imports concentrated from Israel at 51%), Phosphorus (from Kazakhstan at 88%), Halides (from the US at 57%), Artificial Corundum (from China at 67%), and Chlorides (from Argentina at 60%) ([74])		
Wafers and substrates	Moderate capital intensity but high precision; margins typically **15–25%**. Key differentiator for advanced nodes and power semiconductors.	**The EU has a relatively strong global position in SOI wafers, with Soitec and Siltronic being notable players**	Limited production scale compared to Asian competitors. Japan leads the market with 56% ([76])	Europe's overall Europe's share in wafer production is 14% ([78])	Linked to Pillar II (Funds new wafer fabs (Si, SiC, GaN) and advanced substrate production) and Pillar III, but with important limitations in direct intervention on substrate materials production.

([74]) Cerutti, I., & Nardo, M. (2023). *Semiconductors in the EU: State of play, future trends and vulnerabilities of the semiconductor supply chain*
([76]) Cerutti, I., & Nardo, M. (2023). *Semiconductors in the EU: State of play, future trends and vulnerabilities of the semiconductor supply chain*
([78]) Cerutti, I., & Nardo, M. (2023). *Semiconductors in the EU: State of play, future trends and vulnerabilities of the semiconductor supply chain*

GVC segment	Value added characteristics	EU strengths	EU gaps	EU share in the global market	Chips Act relevance
	Bottlenecks can constrain the entire manufacturing chain; wafer supply has long lead times (12–24 months).		China holds large shares in key materials for wafers, such as silicon, accounting for 64% of the global supply ([77]) and is also the dominant source of primary gallium, which is critical for GaN wafer and substrate manufacturing.		
Semiconductor manufacturing equipment	Extremely high technological and IP barriers; cumulative R&D intensity >10 % of revenue. Profit margins relatively high (20–30 %), driven by after-sales service and installed base. Equipment defines achievable process nodes and is a main determinant of competitive advantage.	The EU holds a strong global position in front-end equipment, particularly in photolithography ([79]) ASML, an EU-based company, has a monopolistic position in EUV lithography and a strong position in lithography equipment holding an 88% market share in 2022. ASML is also a significant supplier of metrology & inspection equipment, with a 12% global market share ([50])	The EU is reliant on foreign suppliers, mostly from the US and partly from Japan, for etching and cleaning (e.g., LAM Research), metrology & quality control (e.g., KLA Tencor), and other front-end segments (e.g. Applied Materials) ([80])	For front-end equipment in 2022, EU companies held a 24.4% market share ([81]) The EU's market share in the total equipment market was 26.4% in 2023 ([82])	Linked with Pillar I: Providing public-funded pilot lines, prototyping and testing facilities. Linked with Pillar II: Equipment is essential for scaling domestic fabs. *Indirectly supporting the demand for the equipment*

([77]) Cerutti, I., & Nardo, M. (2023). *Semiconductors in the EU: State of play, future trends and vulnerabilities of the semiconductor supply chain*
([79]) DECISION Études & Conseil. (2024). *Economic analysis of the EU and global chips ecosystem*
([80]) DECISION Études & Conseil. (2024). *Economic analysis of the EU and global chips ecosystem*
([81]) DECISION Études & Conseil. (2024). *Economic analysis of the EU and global chips ecosystem*
([82]) Bonnet, P., Ciani, A., Molnar, J., & Nardo, M. (2025). *EU's strengths and weaknesses in the global semiconductor sector* (JRC141323, EUR 40253)

GVC segment	Value added characteristics	EU strengths	EU gaps	EU share in the global market	Chips Act relevance
		Overall, the EU is well-positioned in the equipment segment, acting as a net exporter with significant domestic production capacity in specialised machines for wafers and semiconductors	Due to the absence of advanced manufacturing in Europe, sales of advanced equipment such as EUV machines in the EU is close to null.		

1.3.3. Semiconductor design, production and packaging

GVC segment	Value added characteristics	EU strengths	EU gaps	EU share in the global market	Chips Act importance
Fabless **Fab-lite design**	Very high R&D intensity with strong dependence on advanced EDA and IP. Value created through innovation, system integration, and differentiated architectures. Profit margins typically 20–40 %, supported by design differentiation and IP ownership. High productivity, skilled employment,	The EU has important expertise in designing analogue chips, radio frequency (RF) components, sensors & MEMS, power semiconductors, microcontrollers, and silicon photonics ([83]) Major fabless companies such as Qualcomm, Apple and Nvidia have well-established design centres with a considerable number	The EU is not as strong in designing digital logic components, which are increasingly critical due to the rise of AI ([84]), ([85]). The EU has no leading pure-play fabless players ([86]).	Total EU27 semiconductor device companies' world market share in 2023: 10.1 %. Within EU27 semiconductor company revenue, 97 % comes from companies with fabs and 3 % from fabless companies. ([87])	Pillar I support mechanisms (European Design Platform, Competence Centres, Pilot Lines) reduce design costs and provide access to prototyping and integration support for fabless firms. Chips Fund provides capital to fabless start-ups, which face large funding gaps in the design-to-tape-out stage.

([83]) DECISION Études & Conseil. (2024). *Economic analysis of the EU and global chips ecosystem*
([84]) DECISION Études & Conseil. (2024). *Economic analysis of the EU and global chips ecosystem*
([85]) Cerutti, Isabella & Nardo, Michela (2023). *Semiconductors in the EU: State of play, future trends and vulnerabilities of the semiconductor supply chain*. JRC Technical Report, JRC133850.
([86]) DECISION Études & Conseil. (2024). *Economic analysis of the EU and global chips ecosystem*
([87]) IDC (2025). Semiconductors D3: Second interim study report (Version 3.0). Prepared for the European Commission.

GVC segment	Value added characteristics	EU strengths	EU gaps	EU share in the global market	Chips Act importance
	spillovers to research and digital industries.	of employees located in the EU.			Also indirectly connected to Pillar II and Pillar III.
Manufacturing and Production **Integrated Design Manufacturers/Fab-lite**	Very high capital intensity (fabs, equipment, cleanrooms). Value created through process know-how, yield optimisation, and scale. Margins typically 15–30 %, depending on node and utilisation rates. Economic contribution through	The EU has expertise in designing and manufacturing analog chips, radio frequency (RF) components, sensors & MEMS, power semiconductors, microcontrollers, and silicon photonics ([88]).	The EU has capacity in ASICs (Application-Specific Integrated Circuits) and has limited manufacturing capacity for mature nodes (22 nm) and none for cutting-edge microchips (7 nm and below) ([89]) The EU does not have any prominent pure-play foundry that focuses on	EU27 semiconductor manufacturing revenue in 2023: EUR 51 billion; EU27 global market share in semiconductor device manufacturing (IDM + fabless + memory) in 2023: 10.1 %; 97 % of all EU27 semiconductor device revenue comes from IDMs ([92]) EU27 global foundry market share in 2023: 0.9 %, equal to EUR	Pillar II: first-of-a-kind facilities and state aid, which enable large-scale investments in front-end manufacturing. Complementary actions under Pillar I (pilot lines and competence centres) strengthen R&D–manufacturing linkages, while Pillar III ensures supply

([88]) DECISION Études & Conseil. (2024). *Economic analysis of the EU and global chips ecosystem.*
([89]) European Court of Auditors. (2025). *The EU's strategy for microchips: Reasonable progress in its implementation, but the Chips Act is very unlikely to be sufficient to reach the overly ambitious Digital Decade target* (Special Report No. 12/2025). Publications Office of the European Union. https://www.eca.europa.eu/en/publications/SR-2025-12
([92]) IDC. (2025). Semiconductors D3: Second interim study report (Version 3.0). Prepared for the European Commission.

GVC segment	Value added characteristics	EU strengths	EU gaps	EU share in the global market	Chips Act importance
	large-scale investment, supply chain anchoring, and regional employment multipliers.		manufacturing of advanced chipa([90]). The only companies manufacturing advanced process nodes of 16nm and below in the EU are foreign companies such as Intel, GlobalFoundries, and TSMC ([91]).	0.8 billion out of a EUR 96 billion global foundry market ([93])	chain coordination and crisis response.
Assembly, Test, and Packaging (ATP)	Moderate capital intensity; margins typically 10–20 %. Value created through precision, yield optimisation, and reliability assurance.	Europe has developed advanced Photonic Integrated Circuit (PIC) assembly and packaging capabilities, supported by pilot lines such as PIXAPP and	The EU has no relevant OSAT company headquartered in Europe, and back-end manufacturing is largely located in Asia due to its labour-intensive and scale-	The EU's share in global ATP capacity was 3% in 2022 and is projected to remain 3% in 2032 ([97])	Pillar I, through advanced packaging pilot lines and under Pillar II, which enables industrial deployment of FOAK back-end facilities.

([90]) DECISION Études & Conseil. (2024). *Economic analysis of the EU and global chips ecosystem.*
([91]) DECISION Études & Conseil. (2024). *Economic analysis of the EU and global chips ecosystem.*
([93]) IDC. (2025). Semiconductors D3: Second interim study report (Version 3.0). Prepared for the European Commission.
([97]) **Boston Consulting Group (BCG) & Semiconductor Industry Association (SIA) (2024).** *Emerging Resilience in the Semiconductor Supply Chain.* May 2024.

GVC segment	Value added characteristics	EU strengths	EU gaps	EU share in the global market	Chips Act importance
	Labour- and process-intensive, but increasingly automated and digitised. Final stage of value capture which determines chip performance, thermal management, and system integration quality.	specialised facilities like PHIX. European SMEs hold strong global positions in the design and production of packaging and assembly tools for photonic ICs. Extensive know-how in PIC packaging, assembly, and testing provides Europe with a solid technological and industrial base in this niche segment ([94]). The APECS pilot line funded through Pillar I	driven cost structure. As a result, even European firms active in assembly and testing typically operate their high-volume production sites outside the EU, leaving only limited domestic capacity for advanced or high-volume ATP processes. ([95]) Most packaging solutions available in Europe rely on legacy approaches.([96])		ATP stakeholders also benefit from R&D funding under the Chips Joint Undertaking.

([94]) DECISION Études & Conseil. (2024). *Economic analysis of the EU and global chips ecosystem.*
([95]) DECISION Études & Conseil. (2024). *Economic analysis of the EU and global chips ecosystem.*
([96]) Rosati, N., Bonnet, P., Ciani, A., Duch Brown, N., Miguez, S., & Zaurino, E. (2023). *The EC consultation on the semiconductors' value chain* (JRC133892, EUR 31585 EN)

GVC segment	Value added characteristics	EU strengths	EU gaps	EU share in the global market	Chips Act importance
		of the Chips Act is also stimulating the development of advanced packaging competences in Europe.			

1.3.4. Downstream integration and end-use applications

GVC segment	Value added characteristics	EU strengths	EU gaps	EU share in the global market	Chips Act importance
Downstream integration	Integration requires high engineering and software competence and often represents 15–25% of the final system value. Value capture depends on the sophistication of system design, intellectual property, and brand reputation. Economies of scope matter more than economies of scale: integrators that control software–hardware co-design (e.g. Tesla, Apple) capture disproportionate margins.	The EU benefits from strong vertical integration and close collaboration between European automakers and domestic chipmakers, such as NXP, Infineon, and STMicroelectronics, which has enabled European firms to become global leaders in semiconductors for key end-markets such as automotive and industrial automation. This collaboration fosters a robust domestic ecosystem for application-specific semiconductors, particularly in the automotive and wider	Collaboration between semiconductor producers and Tier-1 system suppliers remains fragmented, meaning that outside the automotive sector there are few structured co-development mechanisms, shared technology roadmaps, or early-stage joint design cycles. This limits the ability to translate semiconductor innovations into competitive system-level products in	No single figure available EU companies owned 34% of the global semiconductor market for automotive in 2021. European suppliers are leading in "embedded systems" for applications such as Automotive, Industrial & robotics, Energies, Health & Care, Aerospace / Defence / Security, and telecommunications infrastructures. Infineon, NXP, and STMicroelectronics collectively own approximately 60% of	Pillar I (R&D and pilot lines for heterogeneous integration), Competence Centres that connect chipmakers with system integrators and OEMs Pillar II measures that promote regional coordination and supply chain completeness.

GVC segment	Value added characteristics	EU strengths	EU gaps	EU share in the global market	Chips Act importance
	Increasingly, integration involves vertical collaboration with chipmakers to co-optimise designs (e.g. automotive OEMs specifying chip architectures for autonomous driving).	embedded-systems industries. ([98]). European public-private partnerships (PPPs), chipmakers, and Original Equipment Manufacturers (OEMs) have effectively utilised a vertically integrated cost-and-risk-sharing ecosystem in the automotive sector ([99]). European suppliers are leaders in "embedded systems"	several EU end-markets. ([101]). Europe lags in co-design capabilities for AI accelerators, cloud, and edge-computing hardware, constraining its competitiveness in next-generation data-driven applications ([102]), ([103]). Most European integration capacity focuses on mature embedded systems (automotive,	the global market shares for SIM cards and identity documents ([105]).	

([98]) Ebrahimi, A. (2024). *Groundbreaking chip sovereignty: Europe's strategic push in the semiconductor race.* Institut français des relations internationales (IFRI). ISBN 979-10-373-0874-0.
([99]) Ebrahimi, A. (2024). *Groundbreaking chip sovereignty: Europe's strategic push in the semiconductor race.* Institut français des relations internationales (IFRI). ISBN 979-10-373-0874-0.
([101]) Ebrahimi, A. (2024). *Groundbreaking chip sovereignty: Europe's strategic push in the semiconductor race.* Institut français des relations internationales (IFRI). ISBN 979-10-373-0874-0.
([102]) European Semiconductor Industry Association. (2025). *Position paper on EU Chips Act 2*. Brussels: ESIA.
([103]) McKinsey & Company. (2024). McKinsey on semiconductors: *Creating value, pursuing innovation, and optimizing operations*. New York: McKinsey & Company.
([105]) DECISION Études & Conseil. (2024). *Economic analysis of the EU and global chips ecosystem.*

GVC segment	Value added characteristics	EU strengths	EU gaps	EU share in the global market	Chips Act importance
		for key downstream applications including Automotive, Industrial & robotics, Energy, Health & Care, Aerospace / Defence / Security, and telecommunications infrastructures ([100]).	industrial). There is little domestic infrastructure for advanced packaging-to-system integration or prototyping of heterogeneous modules ([104]).		
End-use applications	Represents the largest aggregate economic value in the semiconductor chain, although distributed across many industries. Chips are also increasingly the key enabler of innovation in a digital and AI-driven economy, since they	EU companies held 34% of the global semiconductor market for automotive in 2021. The EU's semiconductor demand is aligned with its embedded electronic production, with power &		The EU has a strong market position in "embedded electronics industries," which accounted for 64% of its semiconductor consumption in 2022, compared to 22% globally ([107]).	Pillar I supports application-oriented R&D and competence centres. Pillar II secures manufacturing capacity for critical sectors such as automotive, energy, and defence.

([100]) DECISION Études & Conseil. (2024). *Economic analysis of the EU and global chips ecosystem.*
([104]) DECISION Études & Conseil. (2024). *Economic analysis of the EU and global chips ecosystem.*
([107]) DECISION Études & Conseil. (2024). *Economic analysis of the EU and global chips ecosystem.*

GVC segment	Value added characteristics	EU strengths	EU gaps	EU share in the global market	Chips Act importance
	determine the performance, efficiency, and functionality of products ranging from vehicles and industrial machinery to consumer electronics and AI systems. Chips account for 10–40% of the total cost of complex products (e.g. 35% in electric vehicles, ~25% in smartphones, ~15% in industrial machinery). Value capture at this stage depends on product differentiation, brand equity, and software-enabled services (e.g.	analogue, optoelectronics and sensors, and microcontrollers accounting for 63% of EU semiconductor consumption in 2022, compared to 39% globally ([106]).			Pillar III includes end-user industries in supply chain monitoring and crisis response.

([106]) DECISION Études & Conseil. (2024). *Economic analysis of the EU and global chips ecosystem.*

GVC segment	Value added characteristics	EU strengths	EU gaps	EU share in the global market	Chips Act importance
	mobility platforms, IoT ecosystems). Strong spill-over effects to employment, R&D intensity, and regional competitiveness.				

Overall view

Table 7 below summarises the European Union's position along the global semiconductor value chain, combining quantitative indicators of market share and import dependency with a qualitative assessment of resilience and strategic importance. The figures illustrate that dependencies vary significantly by stage: while the EU holds strong positions in manufacturing equipment it remains heavily reliant on non-EU suppliers for wafer substrates, chip manufacturing, and especially assembly, test, and packaging (ATP). The resilience profile column highlights the nature of vulnerabilities that range from geopolitical and supply chain concentration risks; whereas the final column identifies each segment's strategic relevance for achieving the objectives of the EU Chips Act.

IDC 2023 revenue data confirm this asymmetric positioning. EU27-headquartered firms account for roughly 28 % of global capital-equipment revenues, around 21 % of the EDA market (largely reflecting the role of Siemens following its acquisition of Mentor Graphics), and about 17 % of semiconductor materials sales. By contrast, Europe's share of global foundry revenues is below 1 %, and OSAT and IP/licensing activities are negligible. The semiconductor device segment itself represents about 10 % of worldwide device revenues, driven mainly by IDMs such as Infineon, NXP and STMicroelectronics. This pattern underscores that the EU's comparative advantages lie upstream in equipment, design tools and materials, whereas it remains structurally weak in pure-play foundry, back-end services and leading-edge logic production, with important implications for resilience and policy design.

Table 7. The overview table of the EU semiconductors value chain. *Source: compiled by the authors.*

GVC Segment	EU Market Share	Dependency (imports)	Resilience profile	EU strategic importance
Materials	16.8 % in Materials as reported by IDC	39.5 % ([108])	High exposure to geopolitical risks and export restrictions. Fundamental input for the entire semiconductor chain; disruption affects all downstream segments. Core enabler for front-end manufacturing and new wafers (SiC, GaN). Vulnerable to external shocks and capacity bottlenecks.	Ensuring access to high-purity materials and gases is **essential for resilience and security of supply**. Identified as a priority for strategic reserves and mandatory monitoring.
IP	~0% global share	Not applicable	Dominated by US providers, and ARM (UK-based, but owned by Softbank group, JP); structural dependency in key logic & AI IP	**Critical upstream input**; absence of EU IP limits autonomy in advanced logic design
EDA	~20.6% (2023, IDC)	Not applicable (software)	Low → Moderate: EU presence exists (Siemens EDA), but ~80% dependency on US vendors	**Essential for sovereign chip design capability**; limited EU presence, although significant

([108]) Cerutti, Isabella & Nardo, Michela (2023). *Semiconductors in the EU: State of play, future trends and vulnerabilities of the semiconductor supply chain*. JRC Technical Report, JRC133850.

				participant in the western EDA ecosystem.
Semiconductor Manufacturing Equipment	~24–26 % of global equipment market (2023) 27.9 % in Capital equipment (2023) as reported by IDC	24.2% ([109])	Identified as a strategic chokepoint due to concentration of suppliers and long lead times. EU leadership (ASML) gives strategic leverage globally, but dependency on certain US and Japanese (e.g. Tokyo Electron) is also significant. Very limited market for EUV/advanced manufacturing equipment in Europe.	**Central to sustaining EU's comparative advantage** in advanced manufacturing.

([109]) Cerutti, Isabella & Nardo, Michela (2023). *Semiconductors in the EU: State of play, future trends and vulnerabilities of the semiconductor supply chain*. JRC Technical Report, JRC133850.

Semiconductor manufacturing	For foundry services: 0.9% (2023 IDC) For ATP: ~3 % of global ATP capacity (2022; projected constant to 2032) IDC (2023) reports a negligible market share) For IDMs: 10.1% (2023 IDC)	64% ([110])	Foundry: Moderate. new fabs help stabilise share; leading-edge gap persists ATPs: Lack of data transparency and extensive offshoring to Asia create major blind spots. This vulnerability was clearly exposed during the COVID-19 pandemic, when lockdown-related shutdowns of ATP facilities in Asia disrupted global supply and caused cascading shortages across downstream industries. Also, no real-time monitoring of back-end capacity or stockpiles. IDMs: Moderate. strong in automotive/power; weak in logic & memory	An integrated manufacturing chain, spanning front-end fabs, IDMs and advanced back-end (ATP), is **the single critical enabler of Europe's autonomy, resilience and competitiveness** in semiconductors.
Downstream Integration	No consolidated figure; ~34% share in global automotive semiconductors; ~60 % in SIM/ID chips	~70%*	EU downstream actors lack supply chain visibility and incentives for proactive management, although some end-customers have already begun diversifying their supplier base and geographic footprint as part of their own risk-mitigation strategies. However, these diversification efforts remain uneven	**Key to turning chip production into competitive industrial systems** (automotive, robotics, energy).

([110]) Cerutti, Isabella & Nardo, Michela (2023). *Semiconductors in the EU: State of play, future trends and vulnerabilities of the semiconductor supply chain*. JRC Technical Report, JRC133850.

			across sectors and are not yet integrated into a coordinated EU-wide resilience framework.	
End-Use Applications	~34 % global share in automotive semiconductors; 64 % of EU semiconductor demand in embedded industries (vs 22 % global)	*Demand side, not considered in this analysis of semiconductor supply dependencies*	Explicitly mentioned as excluded from current Chips Act crisis-response mechanisms. Largest economic and societal exposure to chip shortages. The EU has very limited presence in consumer electronics, particularly smartphones, which are the principal drivers of demand for leading-edge logic. This limits Europe's influence over supply allocation and reinforces dependence on third-country manufacturing ecosystems.	Incorporating end-users into resilience governance is vital for long-term preparedness and industrial continuity.

*There is no direct indicator for downstream integration dependency, as trade data in the semiconductor value-chain study stop at the chip level.

1.3.5. Modelling the BAU scenario

The dynamic baseline modelling builds directly on the quantitative and qualitative figures presented in the previous table, which summarises the European Union's current position across each segment of the semiconductor global value chain. These baseline indicators covering market share, import dependency, and resilience profile serve as the starting point for projecting the EU's relative performance to 2035 (with a check in point in 2028). Each value represents the best available estimate for 2021–2023, derived from Joint Research Centre dependency ratios, BCG–SIA and McKinsey capacity assessments, and complementary evidence from IFRI, DGE, and Eurostat.

In addition to these structural indicators, the modelling draws on IDC's 2023–2030 forecast series on revenue, which captures verified investment pipelines, corporate announcements, and regional growth expectations. The dataset reflects both global market recovery after the 2022 downturn and strong European capital formation driven by public subsidies and private investment in new fabs and equipment capacity.

To inform the long-run BAU trajectory, it is important to note that growth patterns in semiconductor devices largely determine the evolution of the entire value chain, since device demand drives equipment orders, EDA tool requirements, materials usage, and foundry utilisation. This relationship underpins the approach taken for post-2030 modelling.

Table 8. Compound Annual Growth Rates (CAGR) by Value Chain Segment, 2023–2030. *Source: IDC 2030 study reporting.*

Segment	IDC projection in 2030 (EUR Billion)	Projected CAGR 2023 - 2030	Projected European share of global market in 2030
Intellectual Property (IP)	-	-	-
Electronic Design Automation (EDA)	3.247	7,7 %	17,9%
Capital equipment	62.785	9,9 %	33,5%
Foundry services	1.007	3,0 %	0,5%
OSAT	-		-
Semiconductor devices	85.073	7,7 %	9,6%
Materials	14.319	5,1 %	18,7%
Total	166.432	8.3%	11.6%

To extend the BAU projection to 2035, we are applying a rate consistent with long-term global semiconductor trends observed in the literature. WSTS publishes only short- to medium-term forecasts, but a range of industry sources provide useful evidence for long-term semiconductor market growth. According to the WSTS Spring 2025 forecast, the global semiconductor market is expected to rebound strongly, expanding by +15.4 % in 2025 to USD 728 billion, followed by +9.9 % growth in 2026 to USD 800 billion. Looking further ahead, several independent analyses converge around a mid-single-digit long-term Compound Annual Growth Rate (CAGR). RootsAnalysis projects a 5.08 % CAGR from 2024 to 2035 for the global semiconductor market. Alvarez & Marsal, using WSTS historical data, assume a 5–6 % CAGR

to support their projection that the industry will reach USD 1 trillion by the mid-2030s. Similarly, the Futurum Group states that the semiconductor industry has stabilised around a 6 % long-term growth rate, which they adopt as the benchmark for their forecasts. Taken together, these sources justify the use of a 5–6 % compound annual growth rate (CAGR) as an industry consensus long-term assumption for modelling global semiconductor market expansion. Given these structural conditions, Europe's semiconductor value chain revenues are assumed to grow in line with but below global averages.

In addition, the modelling distinguishes between value-chain segments according to their exposure to global AI-driven growth. Semiconductor devices shape demand for upstream activities and therefore drive overall value-chain dynamics. However, only certain upstream segments in Europe are positioned to benefit from AI-related revenue expansion. In particular, EDA and capital equipment suppliers, including ASML, are tightly linked to global leading-edge logic and AI accelerator demand, and their revenues can therefore be assumed to follow the global long-run CAGR (5-6%). In contrast, materials, devices, and foundry services in the EU remain tied to mature-node production as well as automotive and industrial applications, justifying a more conservative 3-4 % CAGR over 2030–2035.

Table 9. Assumptions for the revenue growth model. *Source: Compiled by the authors*.

Parameter	Global market	Europe (BAU)	Comment
2030–2035 CAGR	5–6 %	Two rates applied: 5–6 % for EDA and equipment; 3–4 % for materials, devices, and foundry (3.5% taken as a central estimate)	Adjusted for limited exposure to AI-driven growth and mature product mix
Growth driver	AI logic, HBM, accelerators	Automotive, power, industrial semiconductors	ASP divergence
Relative global share	Concentration in Asia and US	Stable at 11–12 % ([111])	No structural capacity shift expected
Key risks	AI-cycle volatility, trade barriers, CAPEX constraints	Energy prices, project delays, limited AI participation	Structural, not cyclical

The BAU projection therefore applies differentiated growth assumptions across value-chain segments, with EDA and equipment following a 5–6 % CAGR and materials, devices and foundry following a 3–4 % CAGR. To illustrate these differentiated growth paths, the 2030 IDC values for the relevant segments (Table 2) are projected forward to 2035:

- **EDA (EUR 3.247 bn, 2030)**
  - 5 % CAGR → **EUR 4.14 bn in 2035**
  - 6 % CAGR → **EUR 4.33 bn in 2035**

([111]) Europe's recent revenue share has shown short-term volatility due to downturns in automotive and industrial semiconductors, although its medium-term structural share typically remains within the 10–12 % range.

• Capital equipment (EUR 62.785 bn, 2030)
– 5 % CAGR → **EUR 80.2 bn in 2035**
– 6 % CAGR → **EUR 83.9 bn in 2035**

Subtotal for EDA + equipment in 2035:
EUR 84.3–88.2 bn

• Devices (EUR 85.073 bn, 2030), as also discussed in section 13.1.1, and included here for the sake of completeness
– 3 % CAGR → **EUR 98.7 bn**
– 4 % CAGR → **EUR 103.5 bn**

• Materials (EUR 14.319 bn, 2030)
– 3 % CAGR → **EUR 16.6 bn**
– 4 % CAGR → **EUR 17.4 bn**

• Foundry (EUR 1.007 bn, 2030)
– 3 % CAGR → **EUR 1.17 bn**
– 4 % CAGR → **EUR 1.22 bn**

Subtotal for materials + devices + foundry in 2035:
EUR 116.5–122.1 bn

Combined EU27 semiconductor value chain projection for 2035:
• Low case: 84.3 + 116.5 ≈ **EUR 200.8 bn**
• High case: 88.2 + 122.1 ≈ **EUR 210.3 bn**
• Central estimate ≈ EUR 205 bn

Under the revised BAU assumption, which now reflects the distinct growth trajectories of AI-exposed (EDA, equipment) and mature-node (materials, devices, foundry[112]) activities, the EU27 semiconductor value chain increases from EUR 166.4 billion in 2030 to approximately EUR 201–210 billion in 2035. The central estimate of EUR 205 billion reflects the uplift from globally exposed equipment and EDA segments. Over the full 2023–2035 period, the EU27 semiconductor value chain is therefore projected to grow from EUR 95.9 billion to around EUR 205 billion. This corresponds to a cumulative increase of roughly 114 % and an average annual growth rate of around 6.4 %, with most of the expansion occurring before 2030, which is consistent with the assumptions in the BAU scenario described above.

From this baseline, the modelling assesses how changes in capacity, demand, and policy conditions influence Europe's competitiveness and vulnerability over time. This approach captures both quantitative trends, such as shifts in market share or dependency, and qualitative changes in resilience.

The forward-looking assessment is structured around three key drivers: capacity evolution, demand dynamics, and policy and geo-economic conditions. Together, these drivers determine

[112] Foundry here refers to foundry activities by EU headquartered companies, which exclusively manufacture mature node semiconductors.

how Europe's market share, import dependency, and resilience are likely to develop under the business-as-usual scenario and under alternative policy scenarios.

Capacity evolution

- **Effect on market share**: New fabrication plants, wafer facilities, or equipment production increase the EU's contribution to global output. Additional European capacity therefore lifts market share relative to global totals.
- **Effect on import dependency**: Higher domestic output reduces the need for imports. Delays, cost overruns, or slow uptake of First-of-a-Kind facilities, as noted by the European Court of Auditors (2025), limit these gains.
- **Effect on resilience**: More domestic capacity increases redundancy and reduces supply chain length, improving resilience in front-end manufacturing and materials.

Policy and geo-economic conditions

- **Regulatory shocks:** Export controls, sanctions, or other restrictions reduce access to parts of the global supply chain and raise import dependency in affected segments.
- **Critical-material constraints:** Shortages of inputs such as gallium, germanium, or neon limit potential production growth. Diversification measures or strategic reserves help ease these constraints. The EU also remains exposed to export restrictions on critical materials such as gallium and germanium, where China dominates global processing and has already introduced targeted export controls. Diversification measures and the development of strategic reserves are intended to mitigate these risks, although their impact is expected to remain gradual over the baseline period.
- **Supplier concentration:** High global concentration in foundries and back-end service providers increases systemic risks and lowers resilience.
- **Environmental disruptions**: More frequent floods, storms, and droughts can interrupt global semiconductor production and logistics, as seen in Taiwan and Japan. These events increase volatility in import availability and may heighten dependency in the short term. Strengthening monitoring, stockpiling, and diversification helps mitigate these risks.
- **Positive policy levers:** Investments supported by the Chips Joint Undertaking, IPCEIs, and State-aid schemes can accelerate technology diffusion and expand domestic capacity. These measures can improve market share and resilience while gradually lowering import dependency.

Overview of Business-as-Usual (BAU) scenario

The Business-as-Usual (BAU) modelling indicates that Europe's position in the global semiconductor value chain remains broadly stable, but increasingly constrained by demand as consumption grows faster than domestic production through to 2035. Installed wafer-fabrication capacity in Europe is projected to reach around 1.39 million wafers per month (300 mm equivalent) by 2030, an increase of approximately 31 percent compared with 2023, with a **3.9% annual growth rate**. Applying assumed organic growth of 2% to 4% per year from 2030 onwards to reflect incremental brownfield expansion and future, currently unannounced projects, **overall capacity is projected to reach between 1.54 and 1.69 million wafers per month by 2035**. Given that global capacity is expected to expand at 3% to 5% per year, Europe's share of global wafer capacity therefore remains relatively stable at around 8%.

However, capacity stability contrasts with an expansion in European chip demand, especially from the automotive and industrial sectors. The World Semiconductor Trade Statistics (WSTS) projects a 75% increase in semiconductor shipments to Europe between 2017 and 2027, while the European semiconductor market which is valued at around EUR 50 billion in 2023 continues to grow ([113]). The automotive segment alone represents approximately 37% of semiconductors shipped to Europe, expanding from EUR 13.05 billion in 2023 to EUR 17.38 billion by 2026, an 8.2 percent CAGR ([114]). This is driven by rising semiconductor intensity per vehicle, particularly in electric and connected models that integrate up to 3,000 chips per unit, compared with 1,000–1,500 in conventional vehicles. Parallel growth in the industrial and communication sectors with shipments of analogue, logic, and sensor components up by 30–40% since 2020 further amplifies domestic consumption ([115]).

Although Europe has expanded its semiconductor manufacturing capacity since the COVID-19 shortages, in the long term this growth remains insufficient to keep pace with projected increases in semiconductor consumption. As a result, apparent consumption continues to outstrip domestic output, and import dependence remains high. Only limited improvements are visible in the upstream segments, where diversification efforts modestly reduce reliance on non-EU inputs.

Europe retains a strong position in lithography through ASML, which helps sustain a stable share of roughly 25% in this specific subsegment of semiconductor manufacturing equipment. However, this strength does not extend across the full equipment landscape.

By contrast, front-end manufacturing shows limited change: new fabs in Ireland, France, and Germany help stabilise Europe's position, but dependency remains close to 50% and market share around 9%. Here, very high dependency remains when it comes to advanced logic and memory. The most significant vulnerabilities persist in assembly, test, and packaging, where dependency exceeds 60%, and in downstream integration, where reliance on external suppliers for around 70% of system assembly continues.

Under the Business-as-Usual trajectory, the resilience of Europe's semiconductor value chain improves only marginally and unevenly across segments. Incremental capacity additions and limited diversification reduce exposure in a few upstream areas, particularly chemicals, and wafer substrates, but systemic vulnerabilities persist in the front-end and back-end stages where Europe remains structurally import-dependent. Resilience gains are further offset by external factors, including high global concentration in foundries and packaging services and the rising incidence of environmental disruptions, such as floods, storms, and droughts. These events have already disrupted semiconductor production in regions such as Taiwan and Japan and increase volatility in supply availability. As a result, the overall resilience profile stabilises rather than strengthens, with systemic exposure largely unchanged.

Table 10. Assumed direction for EU market share, import dependency and resilience under BAU scenario.

([113]) European Commission, Joint Research Centre. (2025). *EU's strengths and weaknesses in the global semiconductor sector (JRC141323)*. Publications Office of the European Union. https://data.europa.eu/doi/10.2760/6302476
([114]) Compound Annual Growth Rate.
([115]) European Commission, Joint Research Centre. (2025). *EU's strengths and weaknesses in the global semiconductor sector (JRC141323)*. Publications Office of the European Union. https://data.europa.eu/doi/10.2760/6302476

IDC Segment	EU Market Share (2023 → 2030 → 2035)	Import Dependency (2023 → 2030 → 2035)	Resilience Profile	Baseline summary
Intellectual Property (IP)	2023: <1 % 2030: <1 % 2035: stable	Not applicable	Low (→)	EU has limited IP footprint; ecosystem remains fragmented; dependency on US IP persists.
Electronic Design Automation (EDA)	2023: 21 % 2030: 18 % 2035: stable	Not applicable	Low → Moderate (↑)	Slight gains from EU design-ecosystem initiatives; strong reliance on US EDA vendors remains.
Capital Equipment	2023: 28 % 2030: 34 % 2035: slow growth	2023: ~50 % 2030: stable 2035: stable	High (→)	Strong leadership from ASML; dependence on US/Japanese process equipment persists.
Foundry Services	2023: 1 % 2030: 1 % 2035: stable	2023: 24 % 2030: stable 2035: stable	Moderate (↑)	EU remains dependent on overseas leading-edge foundries.
OSAT	2023: <1 % 2030: <1 % 2035: stable	2023: ~64 % 2030: stable 2035: slow decline	Low → Moderate (↑)	Limited reshoring for automotive and SiC; Asia maintains dominance.
IDMs and fabless	2023: 10 % 2030: 10 % 2035: stable	2023: ~50 % 2030: stable 2035: stable	Moderate (→)	Mature-node strength supports stability; limited exposure to AI logic caps growth. Very high dependency when it comes to advanced logic and memory that in the dependency figure is masked by significant capacity targeting automotive and industrial automation end users.
Materials	2023: 17 % 2030: 19 % 2035: slow growth	2023: ~29–47 % 2030: slow decline 2035: slow decline	Moderate → Moderately high (↑)	Critical Raw Materials Act reduces dependency; risks persist for Chinese-controlled gallium/germanium supply.
End-Use Applications	2023: Automotive represents more than 37% of semiconductor	*Not applicable (demand-side)*	Moderate but uneven (→)	EU demand grows in automotive and industrial sectors; supply reliance remains high.

	shipments to Europe 2030: slow decline 2035: slow decline			

Justification for the assumptions above:

The baseline and forward-looking indicators presented above are derived from a triangulation of official statistics, Joint Research Centre (JRC) analysis, industry forecasts, and academic and policy literature. Each segment of the semiconductor global value chain (GVC) draws on a combination of quantitative trade data, capacity benchmarks, and qualitative assessments of resilience and dependency.

For the Intellectual Property (IP) segment, the 2023 baseline reflects Europe's marginal global footprint (below 1 %), consistent with IDC reporting (2023) as well as McKinsey (2024) **([116])** and IFRI (2024) **([117])**, which highlight the structural dominance of US IP licensors. Since IP does not map onto trade flows, no import dependency metric is reported, and resilience is assessed as remaining low and stable over the baseline period

For Electronic Design Automation (EDA), Europe's 2023 market share (around 21 %) follows IDC's reporting but is projected to decline modestly toward 2030. Dependency cannot be measured through trade statistics, yet qualitative evidence from **BCG–SIA (2024) ([118])** and **Interface (2024) ([119])** suggests that Europe remains heavily reliant on US EDA vendors.

For **semiconductor manufacturing equipment**, the baseline EU market share **of 28 % in 2023, rising toward 34 % in 2030 is captured by IDC, BCG (2021), and McKinsey (2024) ([120])**. These sources identify Europe's enduring leadership in lithography (ASML) and metrology, balanced by continuing reliance on non-EU suppliers for other critical equipment categories, including etching, deposition, and ion implantation tools from the US, as well as mask exposure equipment and EUV light sources from Japan. While the lithography segment is expected to remain a structural strength for Europe, the broader equipment landscape continues to exhibit significant dependencies on US and Japanese technologies.

For foundry services, Europe's market share remains small (around 1 %), consistent with IDC and BCG–SIA (2024) data**([121])**. The dependency rate (~24 %) reflects Europe's continued need for advanced-node and leading-edge wafer capacity located mainly in Taiwan, South Korea,

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([116]) McKinsey & Company. (2024). *McKinsey on semiconductors: Creating value, pursuing innovation, and optimizing operations* (No. 9, March 2024). McKinsey & Company.
([117]) Ebrahimi, A. (2024). *Groundbreaking chip sovereignty: Europe's strategic push in the semiconductor race.* Ifri Memos, Institut français des relations internationales (IFRI). ISBN 979-10-373-0874-0.
([118]) BCG & Semiconductor Industry Association (2024). *Emerging Resilience in the Semiconductor Supply Chain.* Boston Consulting Group and Semiconductor Industry Association, May 2024.
([119]) Kleinhans, J.-P. (2024), *The missing strategy in Europe's chip ambitions: Member States must drive the next steps*, Interface, July 2024.
([120]) McKinsey & Company. (2024). *McKinsey on semiconductors: Creating value, pursuing innovation, and optimizing operations* (No. 9, March 2024). McKinsey & Company.
([121]) **BCG & Semiconductor Industry Association (2024).** *Emerging Resilience in the Semiconductor Supply Chain.* Boston Consulting Group and Semiconductor Industry Association, May 2024.

and the US. New European fabs stabilise capacity but do not materially change global share or structural dependence.

For **assembly, test, and packaging (ATP)**, the baseline dependency of around 64% is derived from the same JRC (2023) ([122]) "chips" category after disaggregation. IDC reporting shows that that **Europe's market share remains negligible (<1 %)**, while McKinsey (2024) ([123]) estimates that 85–90 percent of global packaging value is located in Asia. IFRI (2024) ([124]) and SIA (2024) ([125]) note limited reshoring of ATP for automotive and SiC devices, suggesting marginal gains in European share to 5–6 percent by 2035. Nonetheless, McKinsey (2025) ([126]) emphasises that Europe's back-end gap will remain its most persistent vulnerability.

For semiconductor vendors (including fabless), the baseline market share (~10 %) is drawn from IDC's semiconductor device estimates, while the import dependency figure (~50 %) derives from the **JRC (2023) ([127])** "chips" dependency measure, adjusted to isolate front-end manufacturing. These values align with **BCG–SIA (2024) ([128])** findings that Europe holds only 9–10 % of global wafer capacity. Resilience is assessed as moderate, supported by Europe's strong position in mature nodes but limited by minimal participation in leading-edge logic.

For materials (including gases, chemicals, and wafer substrates), Europe's baseline market share (17 % in 2023, rising to 19 % in 2030) follows IDC segmentation, with import dependency values (29–47 %) derived from **JRC (2023) ([129])** estimates for chemicals, precursors, and wafers. Dependency is projected to decline slowly due to CRMA-driven diversification and expanded SiC and GaN substrate production, although structural reliance on Chinese-controlled gallium and germanium continues to constrain resilience.

The **downstream integration** segment (system assembly and electronic manufacturing services) is characterised by high import dependency of around 70% in 2023. This figure is based on Eurostat COMEXT trade statistics, BCG–SIA (2024) ([130]) global supply chain analysis, and DGE (2024) ([131]). Minor reductions in dependency are consistent with McKinsey

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([122]) Cerutti, Isabella & Nardo, Michela (2023). *Semiconductors in the EU: State of play, future trends and vulnerabilities of the semiconductor supply chain*. JRC Technical Report, JRC133850.
([123]) McKinsey & Company. (2024). *McKinsey on semiconductors: Creating value, pursuing innovation, and optimizing operations* (No. 9, March 2024). McKinsey & Company.
([124]) Ebrahimi, A. (2024). *Groundbreaking chip sovereignty: Europe's strategic push in the semiconductor race.* Ifri Memos, Institut français des relations internationales (IFRI). ISBN 979-10-373-0874-0.
([125]) **BCG & Semiconductor Industry Association (2024).** *Emerging Resilience in the Semiconductor Supply Chain.* Boston Consulting Group and Semiconductor Industry Association, May 2024.
([126]) **McKinsey & Company (2025).** *Semiconductors have a big opportunity but barriers to scale remain.* February 2025.
([127]) Cerutti, Isabella & Nardo, Michela (2023). *Semiconductors in the EU: State of play, future trends and vulnerabilities of the semiconductor supply chain*. JRC Technical Report, JRC133850.
([128]) **BCG & Semiconductor Industry Association (2024).** *Emerging Resilience in the Semiconductor Supply Chain.* Boston Consulting Group and Semiconductor Industry Association, May 2024.
([129]) Cerutti, Isabella & Nardo, Michela (2023). *Semiconductors in the EU: State of play, future trends and vulnerabilities of the semiconductor supply chain*. JRC Technical Report, JRC133850. Publications Office of the European Union. ISBN 978-92-68-06549-5 (online). DOI: 10.2760/038299.
([130]) **BCG & Semiconductor Industry Association (2024).** *Emerging Resilience in the Semiconductor Supply Chain.* Boston Consulting Group and Semiconductor Industry Association, May 2024.
([131]) Direction Générale des Entreprises (DGE) (2024), *Les semi-conducteurs: un marché mondialisé et une dépendance européenne*, *Les Thémas de la DGE*, n° 27, Ministère de l'Économie, des Finances et de la Souveraineté industrielle et numérique, January 2024.

(2025) ([132]) projections of near-shoring in industrial automation and IFRI (2024) ([133]) evidence of increased localisation in defence electronics and power systems.

Finally, **end-use applications** rely on WSTS (2024–2025) market data showing that semiconductor shipments to Europe amounted to about EUR 50 billion in 2023, with the automotive sector alone accounting for more than 37% of the semiconductors shipped to the region ([134]). The WSTS Spring 2025 forecast, together with DGE (2024) ([135]) and IFRI (2024) ([136]), indicates that European semiconductor demand will continue expanding at 5–6% annually, with the automotive segment growing particularly fast at roughly 8.2% CAGR between 2023 and 2026. McKinsey (2025) ([137]) and SIA (2024) ([138]) imply that demand in embedded sectors will continue to rise faster than Europe's domestic production capacity, reinforcing persistent import dependence.

1.4. The cost (price) competitiveness of the EU industry

In line with the Better Regulation Guidelines and the Better Regulation Toolbox (notably Tool #24 on Competition and Tool #21 on Competitiveness), the analysis distinguishes between two interrelated but distinct perspectives: intra-EU competition and extra-EU competitiveness. Here we focus on extra-EU competitiveness.

The extra-EU competitiveness perspective focuses on the cost and price competitiveness of EU semiconductor production in relation to global competitors. To assess Europe's cost and price competitiveness in the global semiconductor industry, the analysis focuses on the **relative cost of production** in the EU compared with global benchmarks (Asian countries and U.S.), and on the **key cost drivers** that shape this gap.

1.4.1. Establishing a starting point for BAU scenario

Semiconductor manufacturing in the EU faces a **structurally higher cost base** than in leading East Asian hubs, with total fab production costs around 40–50% higher than in Taiwan, South Korea and China. ([139]) Capital expenditure (CapEx) is the largest cost component, and capital efficiency in Europe is lower: producing a given manufacturing facility requires significantly more investment than in Taiwan, partly because fabs tend to be smaller on average and project lead times longer. Energy prices for industrial users are a major obstacle to investment, with electricity and gas costs well above US and Asian levels. Labour costs are also high when compared to other major regions: unit labour costs in EU fabs exceed those of major competitors, and estimates suggest that fab labour in Europe can be two to three times more expensive than in East Asia, alongside specific bottlenecks in skilled construction trades and

([132])**McKinsey & Company (2025).** *Semiconductors have a big opportunity but barriers to scale remain.* February 2025.
([133])Ebrahimi, A. (2024). *Groundbreaking chip sovereignty: Europe's strategic push in the semiconductor race.* Ifri Memos, Institut français des relations internationales (IFRI). ISBN 979-10-373-0874-0.
([134]) World Semiconductor Trade Statistics (WSTS) (2025), *Spring 2025 forecast summary and market data*, WSTS, Inc., May 2025
([135]) Direction Générale des Entreprises (DGE) (2024), *Les semi-conducteurs: un marché mondialisé et une dépendance européenne*, Ministère de l'Économie, des Finances et de la Souveraineté industrielle et numérique, January 2024.
([136]) Ebrahimi, A. (2024). *Groundbreaking chip sovereignty: Europe's strategic push in the semiconductor race.* Ifri Memos, Institut français des relations internationales (IFRI). ISBN 979-10-373-0874-0.
([137]) **McKinsey & Company (2025).** *Semiconductors have a big opportunity but barriers to scale remain.* February 2025.
([138])Boston Consulting Group (BCG) and Semiconductor Industry Association (SIA) (2024), *Attracting chips investment: Industry recommendations for policymakers*, August 2024.
([139])Decision Etudes & Conseil and YOLE Group, *Competitiveness of the EU semiconductor manufacturing industry*, Nov. 2025.

some technical roles. At the same time, the semiconductor industry is highly R&D-intensive globally, investing around 22% of revenues in R&D and 26% in capital expenditure. Finally, the EU is heavily reliant on imports of many specialty materials, gases and chemicals, which, despite a strong domestic supplier base in some segments, exposes the European semiconductor ecosystem to supply disruptions and price volatility.

The newly available evidence([140]) confirms and strengthens these patterns. Recent benchmarking of fab-level cost structures shows that total semiconductor production costs in the EU remain structurally above those of all major competitors: EU = 100 (baseline), US = 84, Japan = 84, China = 61, Taiwan = 53, and South Korea = 50. This implies that, on average, EU fabs operate at a 16% cost premium relative to the US and at a 40–50 % premium relative to leading Asian hubs.

Two additional structural factors further widen the EU cost base ([141]):

- First, the cost of capital is considerably higher in the EU than in competing regions. The weighted average cost of capital (WACC) for semiconductor manufacturers operating in the EU is 8.3 %, exceeding that of the US (7.3 %), Japan (8.2 %), China (6.1 %), Taiwan (4.8 %), and South Korea (4.4 %). Higher equity risk premia in Europe, lower market capitalisation of EU-based semiconductor firms, and high exposure to cyclical automotive markets contribute to elevated financing costs.
- Second, unit labour costs in EU manufacturing fabs (0.38 in PPP terms) remain noticeably higher than in the US (0.35) and significantly above levels in China (0.15), Taiwan (0.12), Japan (0.16), and South Korea (0.11). Crucially, this gap is not driven by nominal wages but by lower labour productivity in EU fabs combined with considerably higher employers' social contributions, which in several EU Member States are among the highest in the OECD.

In the table below we outline the available evidence from the literature on the key cost components and possible benchmark figures in comparison to EU's global competitors such as USA, China and Taiwan.

Table 11. Key cost drivers in the Chips industry. *Source: compiled by the authors.*

Driver	Description	Knowledge base from the literature and additional details
Capital intensity and scale	High construction and equipment costs per wafer capacity. Smaller average fab size ([142]) and higher	Constructing a new, state-of-the-art facility is expensive, with location-specific construction and equipment costs being significant drivers of investment decisions ([143]).

([140])Decision Etudes & Conseil and YOLE Group, *Competitiveness of the EU semiconductor manufacturing industry*, Nov. 2025.
([141])Decision Etudes & Conseil and YOLE Group, *Competitiveness of the EU semiconductor manufacturing industry*, Nov. 2025.
([142]) The reference to "smaller average fab size" is based on evidence that Europe's semiconductor ecosystem is dominated by mid-scale fabs focused on mature-node, automotive, power, and analog manufacturing, rather than the large leading-edge megafabs typical of Asia and the US, which achieve significantly greater economies of scale. Evidence drawn from JRC, IFRI, Interface, and industry reports (McKinsey, BCG, SIA) supports this structural distinction.
([143])**Semiconductor Industry Association (SIA)** and **Boston Consulting Group (BCG)**, *Attracting Chips Investment: Industry Recommendations for Policymakers*, August 2024.

	compliance costs inflate EU unit costs.	Wafer fabrication, or front-end manufacturing, accounts for 64% of the industry's capital expenditure ([144]). A state-of-the-art semiconductor fab can require roughly USD 5 billion for mature node fabs to USD 20 billion for advanced logic and memory fabs in capital expenditure, including land, building, and equipment ([145]). Evidence by Decision & Yole ([146]) shows that this effect is compounded in the EU by higher financing costs: semiconductor firms operating in Europe face an average WACC of 8.3 %, substantially higher than in Korea (4.4 %), Taiwan (4.8 %), or China (6.1 %). The industry and its supply chain depend on high utilisation (typically more than 75%) for favourable economics, subsidies, and lower capital utilisation could lead to further boom and bust cycles ([147]). Large-scale operations can significantly reduce costs at fabs ([148]).
Energy costs	Electricity and gas prices for large industrial consumers; Europe's exposure to volatile energy markets increases operational expenditure per wafer.	Energy prices in Europe are two to three times higher than in the US ([149]). Subsidies for utilities can also differ, with Mainland China offering up to 70% and Taiwan 30% ([150]). Some regions, like Germany, may offer caps on energy costs as part of subsidy packages for new fabs ([151]). The updated 2025 data show that wholesale gas prices in the EU are around 2.8 times higher than in the US, directly translating into industrial electricity

([144])Boston Consulting Group (2021), *Strengthening the Global Semiconductor Supply Chain: A report by BCG and the Semiconductor Industry Association (SIA).*
([145])Boston Consulting Group (2021), *Strengthening the Global Semiconductor Supply Chain: A report by BCG and the Semiconductor Industry Association (SIA).*
([146])Decision Etudes & Conseil and YOLE Group, *Competitiveness of the EU semiconductor manufacturing industry*, Nov.2025
([147])**McKinsey & Company (2025).** *Semiconductors have a big opportunity but barriers to scale remain.* February 2025.
([148])McKinsey & Company (2021), *McKinsey on Semiconductors: Creating value, pursuing innovation, and optimising operations.*
([149])DECISION Études & Conseil. (2025). *European consumption of mainstream chips from third countries: Draft final report* (Contract No. EC-CNECT/2024/LVP/0074). European Commission, Directorate-General for Communications Networks, Content and Technology (DG CNECT).
([150])DECISION Études & Conseil. (2025). *European consumption of mainstream chips from third countries*
([151]) **Boston Consulting Group (BCG) & Semiconductor Industry Association (SIA).** (May 2024). *Emerging Resilience in the Semiconductor Supply Chain.*

		prices that are 137 % above US levels because of Europe's marginal pricing system ([152]).
Labour and productivity	Labour costs and productivity in semiconductor manufacturing and equipment operation.	Labour costs are a major factor in construction cost differences. Labour costs in Europe can be two to three times more expensive than in Asia ([153]). Furthermore, labour productivity in major US fabs (Intel, Texas Instruments, GlobalFoundries) is roughly twice the level observed in leading EU fabs (Infineon, STMicroelectronics, Bosch), resulting in higher unit labour costs despite comparable nominal wages. Moreover, EU employers' social contributions, often double those in the US, further elevate total labour costs ([154]). Maintenance costs, heavily influenced by labour rates and overtime, can be up to 50% higher in the US and 30% higher in Europe compared to East Asia ([155]). The increased demand for skilled craft workers means projects often use less experienced workforces, exacerbating productivity issues and extending project timelines ([156]). The industry faces a massive talent gap for engineers, estimated at over 100,000 each in the US and Europe, and upward of 200,000 in Asia–Pacific (excluding China). This talent challenge extends across the entire semiconductor value chain, including equipment design and manufacturing ([157]).
Research and Development (R&D) and design costs	Continuous innovation in chip design, materials, and manufacturing processes requires sustained high R&D	Designing a new state-of-the-art system-on-chip (SoC) for a flagship smartphone can exceed USD 1 billion ([158]), ([159]). For a 5nm chip, design costs, including validation and IP qualification, are about USD 540 million,

([152]) Decision Etudes & Conseil and YOLE Group, *Competitiveness of the EU semiconductor manufacturing industry*, Nov.2025
([153]) **McKinsey & Company (2025).** *Semiconductors have a big opportunity but barriers to scale remain.* February 2025.
([154]) Decision Etudes & Conseil and YOLE Group, *Competitiveness of the EU semiconductor manufacturing industry*, Nov.2025
([155]) DECISION Études & Conseil. (2025). *European consumption of mainstream chips from third countries*
([156]) **McKinsey & Company (2025).** *Semiconductors have a big opportunity but barriers to scale remain.* February 2025.
([157]) McKinsey & Company (2021), *McKinsey on Semiconductors: Creating value, pursuing innovation, and optimising operations.*
([158]) Boston Consulting Group (2021), *Strengthening the Global Semiconductor Supply Chain: A report by BCG and the Semiconductor Industry Association (SIA).*
([159]) Cerutti, Isabella & Nardo, Michela (2023). *Semiconductors in the EU: State of play, future trends and vulnerabilities of the semiconductor supply chain*. JRC Technical Report, JRC133850.

	spending. Advanced-node development drive significant fixed costs, while limited EU design scale raises per-project expenditure.	significantly higher than the USD 175 million for a 10 nm chip or USD 300 million for a seven nm chip ([160]). The semiconductor industry has a high level of intensity in R&D, accounting for 22% of annual final chip revenues ([161]). Design activities account for 65% of the total industry R&D ([162]).
Materials and inputs	Speciality gases, wafers, and chemicals' import dependency adds cost and risk premiums.	Specialty gases, chemicals, metals, and other materials are identified as a top cost item in the semiconductor industry ([163]). Many essential raw materials, such as gallium, germanium, copper, and tungsten, are concentrated in a few locations globally. This concentration increases the dependence of intermediary chemical producers in these specific locations, some of which are geopolitically sensitive. This characteristic makes the supply chain vulnerable to disruptions or necessitates sourcing more expensive alternatives. It may also potentially lead to higher costs if trade restrictions are imposed ([164]). Since companies often import many materials, border costs such as tariffs, fees, customs clearance, and regulatory approvals are decisive factors in cost assessments ([165]).

Overall, we see that **capital intensity and scale** remain the dominant driver: building and equipping a state-of-the-art fab can require between **USD 4 billion and USD 20 billion ([166])**, with **wafer fabrication alone accounting for around 64 % of total capital expenditure**. Smaller average fab sizes and higher compliance costs in Europe inflate per-wafer unit costs compared with Asia, where large-scale operations achieve substantial economies of scale.

([160]) McKinsey & Company (2021), *McKinsey on Semiconductors: Creating value, pursuing innovation, and optimising operations.*
([161]) Boston Consulting Group (2021), *Strengthening the Global Semiconductor Supply Chain: A report by BCG and the Semiconductor Industry Association (SIA).*
([162]) Cerutti, Isabella & Nardo, Michela (2023). *Semiconductors in the EU: State of play, future trends and vulnerabilities of the semiconductor supply chain*. JRC Technical Report, JRC133850.
([163]) Boston Consulting Group (BCG) and Semiconductor Industry Association (SIA) (2024), *Attracting chips investment: Industry recommendations for policymakers*, August 2024.
([164]) **McKinsey & Company (2025).** *Semiconductors have a big opportunity but barriers to scale remain*. February 2025.
([165]) Boston Consulting Group (BCG) and Semiconductor Industry Association (SIA) (2024), *Attracting chips investment: Industry recommendations for policymakers*, August 2024.
([166]) Building on BSC figure, converted to EUR from USD.

When all major components (capital, labour, energy, land) are combined, EU fabs remain 16% more expensive than US fabs and up to 50% more expensive than leading Asian fabs ([167]).

1.4.2. Modelling the BAU scenario

Building on the state of play overview above we provide a logical inference on how EU

Information anchors

Global investment and cost structure: Industry plans roughly USD 1 trillion of new fabs by 2030 ([168]), but structural cost gaps remain due to site productivity, logistics, and cluster effects. Europe faces higher construction and operating costs and slower ramp-ups compared with leading Asian sites. Build-and-commission timelines for EU based fabs are around 34 months, compared to 19 months in Taiwan. ([169])

Node mix and ecosystem gaps: Europe's strengths are in automotive, power, analogue and sensors, with limited leading-edge logic. There are clear gaps in back-end, advanced packaging and substrates, which increasingly determine system-level performance and cost.

Talent constraints: Skills shortages in engineering and skilled trades are a binding constraint in Europe as well as the US and Asia, affecting time-to-build and OPEX.

Materials and inputs: The EU remains dependent on imported specialty gases, chemicals and critical raw materials with concentrated global supply, adding price and disruption risk premia.

Capital intensity and fab scale

- **Developments expected under BAU:** A number of EU greenfield and brownfield projects announced since 2023 complete construction and begin ramping. Local supplier bases deepen marginally, and experience curves reduce overruns. However, **average EU fabs remain smaller ([170]) than Asian mega-fabs** and less embedded in very large, turnkey industrial parks.
- **Rationale:** Persistent **barriers to scale** in Europe and North America include higher construction costs and logistics frictions; the **European Court of Auditors (ECA)** underlines that public support levels and timelines fall short of transforming EU market share quickly ([171]). In addition, Europe faces structurally higher financing costs: the weighted average cost of capital (WACC) for semiconductor manufacturers is 8.3% in the EU, compared with 7.3 % in the US, 6.1 % in China, 4.8 % in Taiwan, and 4.4% in

([167]) Decision Etudes & Conseil and YOLE Group, *Competitiveness of the EU semiconductor manufacturing industry*, Nov.2025
([168]) **McKinsey & Company (2025).** *Semiconductors have a big opportunity but barriers to scale remain.* February 2025.
([169]) IDC "Semiconductors Market Data by Feature Size, Sector, and Region" Report
([170]) The reference to "smaller average fab size" is based on evidence that Europe's semiconductor ecosystem is dominated by mid-scale fabs focused on mature-node, automotive, power, and analog manufacturing, rather than the large leading-edge megafabs typical of Asia and the US, which achieve significantly greater economies of scale. Evidence drawn from JRC, IFRI, Interface, and industry reports (McKinsey, BCG, SIA) supports this structural distinction.
([171]) European Court of Auditors. (2025). *Special Report 12/2025 – The EU's strategy for microchips: Reasonable progress in its implementation, but the Chips Act is very unlikely to be sufficient to reach the overly ambitious Digital Decade target.*

South Korea ([172]). These higher financing costs make large-scale investments more expensive to execute in Europe relative to leading competitors.

- **Implication for costs:** According to the comparative fab cost index by Decision & Yole ([173]), Europe remains the highest-cost location among the major semiconductor manufacturing regions: EU = 100, US = 84, Japan = 84, China = 61, Taiwan = 53, Korea = 50. This evidence suggests that, even if some cost efficiencies materialise as EU sites mature, a significant structural cost gap remains between the EU and leading Asian ecosystems under a business-as-usual trajectory.

Operating expenditure (energy, labour, compliance)

- **Developments expected under BAU:** Energy markets stabilise relative to the 2022–2023 spike, with more long-term **power purchase agreements (PPAs)**, **and on-site renewables**. Labour productivity improves gradually through automation and learning, but **wage levels and compliance costs** in Europe remain structurally high. EU skills programmes, increased automation, and migration relieve the **worst shortages**, but global competition keeps talent **tight and expensive**. Construction and ramp-up timelines also remain longer in Europe, with typical build-and-commission periods of about 34 months compared with roughly 19 months in Taiwan, reinforcing cost and time-to-market disadvantages.
- **Rationale:** The ECA suggests **no near-term step-change** in competitiveness drivers from current policies ([174]); McKinsey points to recurring OPEX headwinds in Europe and North America ([175]). Europe faces structurally higher energy prices: the report shows that EU wholesale gas prices are around 2.8 times those in the US, which contributes to industrial electricity prices that are 137 % higher in the EU compared with the US. Labour cost pressures also persist with unit labour costs in EU semiconductor manufacturing (0.38) remaining above those in the US (0.35) and significantly above levels in Korea (0.11), Taiwan (0.12), China (0.15), and Japan (0.16), largely due to lower productivity and higher employers' social contributions in the EU ([176]).
- **Implication for costs:** Europe remains a structurally higher-cost operating environment compared with major competitors. The report identifies energy and labour costs as two of the main contributors to the EU's higher fab cost index (EU = 100 vs 84 in the US) ([177]). Under BAU, some efficiency gains may occur, but the evidence suggests that Europe's operating-cost disadvantage will persist.

Advanced packaging and substrates

- **Developments expected under BAU:** Europe pilots some **advanced-packaging lines** and niche OSAT activity, with new investments such as the planned SiliconBox

([172]) Decision Etudes & Conseil and YOLE Group, *Competitiveness of the EU semiconductor manufacturing industry*, Nov.2025
([173]) Decision Etudes & Conseil and YOLE Group, *Competitiveness of the EU semiconductor manufacturing industry*, Nov.2025
([174]) European Court of Auditors. (2025). *Special Report 12/2025 – The EU's strategy for microchips: Reasonable progress in its implementation, but the Chips Act is very unlikely to be sufficient to reach the overly ambitious Digital Decade target.*
([175]) **McKinsey & Company (2025).** *Semiconductors have a big opportunity but barriers to scale remain.* February 2025.
([176]) Decision Etudes & Conseil and YOLE Group, *Competitiveness of the EU semiconductor manufacturing industry*, Nov.2025
([177]) Decision Etudes & Conseil and YOLE Group, *Competitiveness of the EU semiconductor manufacturing industry*, Nov.2025

advanced-packaging facility in Novara strengthening capabilities in specialised advanced packaging activities. However, **volume capacity remains concentrated in Asia**, which increasingly shapes system performance, cost and time-to-market.

- **Rationale:** The JRC (2025) ([178]) shows Europe's strategic dependency on the US and Asia for advanced packaging and IC substrates. IFRI (2024) ([179]) similarly highlights structural gaps in Europe's back-end capabilities. While Member State support has begun to include back-end initiatives such as Silicon Box in Italy and the (now-cancelled) Intel packaging project in Poland, the bulk of announced investments have been focused on front-end fabrication. Overall, the evidence indicates that Europe's structural gap in advanced packaging is likely to persist under BAU.
- **Implication for costs:** While firms offshore back-end processing because private production costs are lower in Asia, Europe's reliance on overseas packaging introduces additional logistics, coordination, and lead-time costs at the system level. As the Nexperia case illustrates, export restrictions imposed on back-end sites can have serious repercussions for European industry. These do not outweigh Asia's cost advantages for individual firms but nonetheless reduce Europe's ability to optimise time-to-market and design–manufacturing integration compared with a fully localised supply chain. *(Logical chain grounded in cited ecosystem gaps.)*

Materials, chemicals and gases

- **Developments expected under BAU:** Incremental **supplier diversification and recycling** reduce some risk premia, but EU remains **import-dependent** for many critical inputs with geopolitically concentrated supply. Continued investment in semiconductor manufacturing capacity is expected to encourage material suppliers to expand their presence.
- **Implication for costs:** continued exposure to **price volatility and border-compliance costs**, adding a thin but persistent premium to EU unit costs. *(Qualitative inference.)*

Key uncertainties

- **Energy price path**: faster convergence would narrow OPEX more quickly; renewed volatility would widen it. EU wholesale gas prices are currently 2.8 times higher than in the US and EU industrial electricity prices remain 137% higher ([180]). These structural differences imply that even moderate volatility could significantly affect the EU cost base because energy is a major driver of fab operating expenditure.
- **Talent inflows**: stronger migration and training outcomes could shorten ramp times and reduce labour premia by the early 2030s. The EU still benefits from 1.1 million STEM graduates per year, more than the US (0.9 million), but growth in STEM output since 2015 has been only 11%, compared with 32% in the US and a near doubling in China. This slower growth increases uncertainty regarding the EU's long-term talent advantage ([181]).

([178]) Bonnet, P., Ciani, A., Molnar, J., & Nardo, M. (2025). *EU's strengths and weaknesses in the global semiconductor sector* (JRC141323, EUR 40253). Luxembourg: Publications Office of the European Union. https://doi.org/10.2760/6302476

([179]) Ebrahimi, A. (2024). *Groundbreaking chip sovereignty: Europe's strategic push in the semiconductor race.* Ifri Memos, Institut français des relations internationales (IFRI). ISBN 979-10-373-0874-0.

([180])Decision Etudes & Conseil and YOLE Group, *Competitiveness of the EU semiconductor manufacturing industry*, Nov.2025

([181])Decision Etudes & Conseil and YOLE Group, *Competitiveness of the EU semiconductor manufacturing industry*, Nov.2025

- **Global subsidies race**: escalation in the US or Asia could further widen gaps if EU support remains static. Japan, China, and the US have all announced larger semiconductor support packages than the EU Chips Act, in some cases several times higher ([182]), which increases uncertainty about Europe's relative attractiveness for future capital-intensive projects.

1.5. Public budget effects

1.5.1. Establishing a starting point for BAU scenario

Public support for Europe's semiconductor ecosystem is already substantial, combining EU-level instruments, national state-aid schemes, and regional investment incentives.

To date, total announced public funding commitments under the EU Chips Act and related initiatives amount to approximately €32 billion, including both EU and national (without accounting for the IPCEI on Microelectronics and Communication Technologies).

At the EU level, the Chips Act also provides an indicative public envelope of additional EUR 11 billion over 2021-2030, financed mainly through:

- Horizon Europe and Digital Europe programmes for R&D and pilot-line development (Pillar I);
- First-of-a-Kind (FoaK) industrial-deployment support (Pillar II);
- Coordination, monitoring, and crisis-response measures (Pillar III).

At the national level, Member States have pledged the bulk of financial support through the IPCEI on Microelectronics and Communication Technologies and bespoke subsidy schemes. Germany, France, Italy, Ireland, and Austria together account for more than 80% of total national semiconductor funding.

In terms of fiscal revenues, the semiconductor sector remains modest but rising: it accounts for less than **0.3 % of EU GDP (≈ EUR 44 billion in gross value added)** and generates around **EUR 7.5 billion annually in tax receipts**, ([183]) ([184]) mainly through corporate taxation, labour contributions, and indirect taxes on high-value manufacturing ([185]). The sector's potential for multiplier effects is high, yet most fiscal returns are geographically concentrated in host regions.

Table 12. Starting parameters. *Source: Compiled by authors.*

Variable	Description	Value	Source
EU-27 GDP (2023)	Nominal GDP baseline	€14.6 trillion	Eurostat (AMECO)

([182])Decision Etudes & Conseil and YOLE Group, *Competitiveness of the EU semiconductor manufacturing industry*, Nov.2025

([183]) The effective fiscal yield (τ) used in this model represents the average share of gross value added accruing to public finances through corporate, labour, and indirect taxation. Based on OECD (2024) and JRC (2025) fiscal incidence data, and calibrated using semiconductor sector margins (Deloitte 2021; McKinsey 2025), τ is set at 16 % for 2023–2029 and 17 % for 2030–2035. This corresponds to approximately 9 % of GVA from payroll and social contributions, 4–5 % from corporate income tax, and 2–3 % from indirect levies.

([184]) Here the' semiconductor sector' refers to semiconductor manufacturers and not the broader semiconductor value chain.

([185]) Bonnet, P., Ciani, A., Molnar, J., & Nardo, M. (2025). *EU's strengths and weaknesses in the global semiconductor sector* (EUR 40253 EN). Luxembourg: Publications Office of the European Union. https://doi.org/10.2760/6302476

Semiconductor sector GVA	0.3 % of GDP GVA=14,600×0.003=€43.8 billion.	≈ €44 billion	JRC (2025) ([186])
Total public commitments (EU + MS)	Chips Act + IPCEI ME2 + national subsidies	€32 billion (2023–2030)	European Court of Auditors (2025), *Special Report 12/2025*
Effective fiscal yield (corporate, labour, indirect)	Average share of value added captured as fiscal revenue EUR 44 billion x 17% ≈ EUR 7.7 billion	16–17 %	JRC (2025) ([187]); OECD Tax Revenue Database ([188])
Sectoral output growth (BAU)	Compound annual growth rate of semiconductor GVA	6.9%	From the market size estimations
Discount rate	Real rate for long-term public investment appraisals	3 %	European Commission, Better Regulation Tool #61

1.5.2. Modelling the BAU scenario

Developments expected under BAU

Under a Business-As-Usual trajectory, the fiscal landscape of the semiconductor industry remains stable, with public-sector expenditure patterns following current commitments and limited expansion beyond projects already announced.

- **Public expenditure**. EU and national support continues through 2030 as existing fab and pilot-line projects are implemented. Expenditure peaks between 2026 and 2029, during the construction and ramp-up phase, and declines thereafter as facilities move to operational self-financing. No significant new EU-level budgetary envelopes are foreseen after 2030.
- **Public revenues**. As fabs reach full operation, corporate-tax revenues and social contributions rise gradually. Most fiscal gains accrue in Germany, France, Ireland, and Austria, where large-scale projects are located.
- **Net budgetary balance**. The overall fiscal balance of the Chips Act and related measures remains negative over most of the 2020s, reflecting the long gestation period of semiconductor investments. Only in the 2030s do cumulative public receipts begin to approach prior outlays, assuming stable global demand and high-capacity utilisation.

Rationale and evidence base

The persistence of the current fiscal pattern is explained by structural and institutional factors:

1. **Capital intensity and sunk costs**. Semiconductor fabrication and equipment production are among the most capital-intensive industrial activities. Once established,

([186]) Bonnet, P., Ciani, A., Molnar, J., & Nardo, M. (2025). *EU's strengths and weaknesses in the global semiconductor sector* (EUR 40253 EN). Luxembourg: Publications Office of the European Union. https://doi.org/10.2760/6302476
([187]) Bonnet, P., Ciani, A., Molnar, J., & Nardo, M. (2025). *EU's strengths and weaknesses in the global semiconductor sector* (EUR 40253 EN). Luxembourg: Publications Office of the European Union. https://doi.org/10.2760/6302476
([188]) *OECD Tax Revenue Statistics: Comparative Tables and Tax Revenue Database (Edition 2024).* Paris: OECD Publishing. Available at https://stats.oecd.org/Index.aspx?DataSetCode=REV

these facilities create long-term lock-in and relocating them is economically prohibitive ([189])

2. **Fiscal-return dynamics**. Empirical modelling by Deloitte (2021) ([190]) suggests semiconductor multipliers of 1.2–1.5, meaning that for every euro of public investment, between EUR 1.20 and EUR 1.50 of additional economic output is generated. However, the realisation of these multipliers depends on sustained utilisation rates and global market stability.

Implications

Short-term (2025–2030)

- High fiscal outflows linked to construction subsidies and infrastructure provision.
- Limited immediate return in tax revenue due to investment write-offs and accelerated depreciation allowances.
- National budgets face concentration risks where large individual projects dominate expenditure ([191]).

Medium-term (2030–2035)

- Operational fabs generate steady corporate-tax inflows and social contributions.
- Spillover effects (supplier VAT, construction, and services) strengthen local fiscal bases around centres of activity, where large scale front-end facilities reach maturity. Other clusters are more focused on R&D, design, and equipment, which yield smaller direct fiscal flows in the short to medium term.
- EU-level expenditure declines as pilot lines and competence centres move into self-sustaining models.

Long-term (post-2035 trend)

- Fiscal breakeven is achievable if facilities remain globally competitive and avoid obsolescence.
- Potential positive net position through continued exports and technology spillovers.
- Risk remains of fiscal asymmetry between Member States, as larger economies capture most revenue while smaller ones shoulder coordination or cohesion costs without direct returns.
- High energy and water use in concentrated clusters may necessitate additional public investment in utilities and grid capacity, partly offsetting fiscal gains.
- Continued labour-market imbalances could require supplementary training budgets to address skills shortages, exerting additional fiscal pressure.

([189]) **McKinsey & Company. (2025).** *Semiconductors have a big opportunity, but barriers to scale remain.* New York: McKinsey Global Institute.
([190]) Deloitte. (2021). *Measuring semiconductors' economic impact: How many jobs does the semiconductor industry create?* Deloitte Insights, September 2021.
([191]) European Court of Auditors. (2025). *Special Report 12/2025 – The EU's strategy for microchips: Reasonable progress in its implementation, but the Chips Act is very unlikely to be sufficient to reach the overly ambitious Digital Decade target.*

2. MODELLING SOCIAL IMPACTS

2.1. Jobs in the EU semiconductor industry

2.1.1. Establishing a starting point for BAU scenario

The semiconductor industry in Europe supports a substantial and growing labour force, concentrated in high-skill and high-value-added activities. In 2023, the European Chips Skills Academy estimated the **EU semiconductor workforce at approximately 382 000 jobs** across the full value chain, including around **263 000 in core design and production**. The top 25 employers account for roughly 40 % of this employment base ([192]).

Employment is concentrated in a few regional clusters such as Saxony, Crolles-Grenoble, Eindhoven-Veldhoven, and Dresden, where manufacturing, equipment supply, and research organisations co-locate. These clusters benefit from strong productivity but face tight local labour markets.

Europe's chip workforce is highly skilled. Deloitte (2021) ([193]) shows that semiconductor manufacturing employment is concentrated in engineers, technicians, and specialised trades, with wages more than double the private-sector average due to the high skill intensity and continuous-operation environment. ECSA (2024) ([194]) and McKinsey (2024) ([195]) confirm that Europe's semiconductor workforce is dominated by technical and engineering profiles requiring advanced qualifications, with wage premia and strong compliance and safety requirements consistent with global benchmarks. According to Deloitte (2021) ([196]), semiconductor workers earn on average more than twice the private-sector wage and roughly 50% more than the manufacturing average in the US, reflecting the sector's high skill intensity and 24/7 operations. Although direct EU data is scarce, similar occupational structures suggest a substantial **wage premium in Europe as well, conservatively estimated at around 40–50 % above the manufacturing average**.

The quality of jobs is correspondingly high, with permanent contracts prevailing and considerable investment in training and safety. **Indirect and induced employment multipliers are significant**: U.S. evidence shows that each semiconductor job supports roughly 5–6 additional jobs in the wider economy (a total multiplier of about 6.7), according to Deloitte (2021) ([197]) based on SIA/Oxford Economics modelling ([198]). Given Europe's dense supplier ecosystem, particularly in equipment and materials, the EU's multiplier effects are likely substantial, though not yet formally quantified.

The demand for skills already exceeds supply. McKinsey (2024) ([199]) estimates a shortfall of over 100 000 engineers in Europe, similar in magnitude to the U.S. gap. Online vacancy data

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([192]) European Chips Skills Academy (ECSA). (2024). *European semiconductor skills strategy 2024.* Luxembourg: Publications Office of the EU.
([193]) **Deloitte.** (2021). *Measuring semiconductors' economic impact.* Deloitte Insights.
([194])European Chips Skills Academy (ECSA). (2024). *European semiconductor skills strategy 2024.* Luxembourg: Publications Office of the EU.
([195]) McKinsey & Company. (2024). *McKinsey on semiconductors: Creating value, pursuing innovation, and optimizing operations* (No. 9, March 2024). McKinsey & Company.
([196]) **Deloitte.** (2021). *Measuring semiconductors' economic impact.* Deloitte Insights.
([197]) **Deloitte.** (2021). *Measuring semiconductors' economic impact.* Deloitte Insights.
([198]) https://www.semiconductors.org/chipping-in-sia-jobs-report/
([199]) McKinsey & Company. (2024). *McKinsey on semiconductors: Creating value, pursuing innovation, and optimizing operations* (No. 9, March 2024). McKinsey & Company.

show that postings for semiconductor technical roles in the EU grew at over 75 % CAGR between 2018 and 2022, a clear signal of unmet demand ([200]). SEMI Europe (2024) ([201]) similarly estimates that approximately 350 000 additional workers would be required by 2030 to meet the Chips Act objectives which is well above the current expansion pipeline. The Joint Research Centre (JRC, 2025) ([202]) lists skills shortages alongside fragmented markets and complex regulation as the main competitiveness constraints of the EU semiconductor ecosystem.

This demand projection assumes that only the announced increase in manufacturing capacity will take place over the course of this decade, and that no further significant investments in manufacturing capacity are made, except for organic expansions of current facilities.

Since job creation is proportional to the investment level, a further increase in public and private investment would result in a commensurate increase in high-quality and high-added value jobs, with the positive spill overs that this would have both from a social and an economic productivity perspective. This factor has not been quantitatively assessed in this social impacts model.

2.1.2. Modelling the BAU scenario

Developments expected under BAU

Under a business-as-usual trajectory, the EU semiconductor labour market expands gradually but remains constrained by structural skills shortages and uneven regional capacity. Between 2025 and 2030, the new fabs and expansions already under construction: **Intel Ireland, STMicroelectronics–GlobalFoundries Crolles, ESMC Dresden, Infineon Dresden, GlobalFoundries Dresden expansion,** and the **Catania SiC Campus**. They generate direct and indirect job growth as they ramp from construction to production. By 2030, the bulk of these facilities are expected to reach steady operation, with employment transitioning from construction trades to production technicians, maintenance engineers, and process specialists.

Beyond 2030, employment growth moderates as automation deepens and fabs reach maturity. Job creation increasingly depends on the localisation of **advanced packaging, compound-semiconductor production (SiC/GaN),** and **equipment manufacturing**, where Europe holds competitive strengths.

Nevertheless, under BAU, the **skills constraint** remains binding: the pool of engineers and technicians grows too slowly to meet rising demand, even with national training and mobility programmes. ECSA (2024) ([203]) projects that, under current policies, the EU semiconductor sector will add around 156 000 new jobs by 2030 (≈ 5 % CAGR) and experience about 271,000 cumulative openings when retirements and replacement needs are included. However, graduate inflows are projected to grow by only ≈ 1 % per year, implying a widening shortfall of around 16 800 unfilled technical roles by 2030. Unless the pace of education and reskilling accelerates

([200]) McKinsey & Company. (2024). *McKinsey on semiconductors: Creating value, pursuing innovation, and optimizing operations* (No. 9, March 2024). McKinsey & Company.
([201]) SEMI Europe. (2024). *Advocacy White Paper 2024.* Brussels: SEMI Europe.
([202]) European Commission, Joint Research Centre (JRC). (2025). *EU's strengths and weaknesses in the global semiconductor sector (JRC141323).* Luxembourg: Publications Office of the EU.
([203]) European Chips Skills Academy (ECSA). (2024). *European semiconductor skills strategy 2024.* Luxembourg: Publications Office of the EU.

markedly, the projected headcount increases in announced projects will not translate one-to-one into realised employment.

Rationale and evidence base

- **Industrial context:** McKinsey (2024) ([204]) projects about **USD 1 trillion in global fab investments by 2030**, implying **intense competition for qualified talent**. Europe captures a modest share of these projects, insufficient to transform its labour dynamics rapidly.
- **Policy context:** The Chips Act provides support for competence centres, skills initiatives, pilot lines and first-industrial deployment, but these initiatives are only now being implemented. It is therefore too early to assess their full impact on the talent gap, although current evidence suggests that substantial shortages will persist in the near term. The **European Court of Auditors (2025) ([205])** observes that current public support levels and timelines "fall short of transforming EU market share quickly".
- **Skills evidence:** ECSA (2024) ([206]) and SEMI Europe (2024) ([207]) highlight that the largest shortages will occur in **technicians, process engineers, and software/automation specialists**, reflecting the shift toward **smart manufacturing, advanced materials**, and **digital design integration**.
- **Geographical concentration:** Existing clusters (Dresden, Grenoble, Eindhoven, Catania, Southern Austria) attract investment and provide higher hiring efficiency, but new greenfield sites face slower ramp-up due to limited local talent pools which is highlighted in McKinsey's (2024) ([208]) analysis.

Implications for employment and skills

- **Job creation:** The EU semiconductor workforce is expected to continue expanding through 2030 as ongoing investments reach full capacity. By 2035, employment growth slows but remains positive, driven by ecosystem expansion in equipment, materials, and specialised manufacturing. However, realised employment depends on mitigating the skills bottleneck.
- **Job quality:** Semiconductor jobs remain among the most stable and best-paid in manufacturing. High skill intensity and safety standards support good working conditions and strong career progression prospects.
- **Skills demand:** The composition of employment shifts toward **process automation, embedded software, AI/ML-assisted design,** and **compound-materials engineering**. Without significant training acceleration, the EU risks persistent reliance on third-country experts and cross-border mobility.

([204]) McKinsey & Company. (2024). *McKinsey on semiconductors: Creating value, pursuing innovation, and optimizing operations* (No. 9, March 2024). McKinsey & Company.
([205]) European Court of Auditors. (2025). *Special Report 12/2025 – The EU's strategy for microchips: Reasonable progress in its implementation, but the Chips Act is very unlikely to be sufficient to reach the overly ambitious Digital Decade target.* Luxembourg: Publications Office of the European Union.
([206]) European Chips Skills Academy (ECSA). (2024). *European semiconductor skills strategy 2024.* Luxembourg: Publications Office of the EU.
([207]) SEMI Europe. (2024). *Advocacy White Paper 2024.* Brussels: SEMI Europe.
([208]) McKinsey & Company. (2024). *McKinsey on semiconductors: Creating value, pursuing innovation, and optimizing operations* (No. 9, March 2024). McKinsey & Company.

- **Systemic risk:** Labour shortages may become a structural drag on the effectiveness of Chips Act investments, limiting capacity utilisation and slowing Europe's technology-leadership ambitions.

2.2. SME/start-up ecosystem in the EU semiconductor industry

2.2.1. Establishing a starting point for BAU scenario

Small and Medium-sized Enterprises (SMEs) in the EU semiconductor industry face specific conditions and challenges. Historically, information on smaller players has been limited, providing only a partial picture of their involvement compared to larger companies ([209]).

One significant weakness in the EU semiconductor industry is the need for stronger cooperation between large companies and innovative SMEs, as SMEs currently struggle to gain attention ([210]). This is particularly evident in the design of advanced processors, despite the EU having a thriving ecosystem of startups in this area ([211]). Large firms also tend to have more diversified expenditure on inputs across geographical areas than SMEs ([212]).

To address these challenges, the Chips Act includes initiatives aimed at supporting SMEs and startups. These include a design platform designed to lower barriers to entry for chip design. Additionally, the Chips Fund offers various equity and debt solutions for SMEs and startups. Competence Centres are also being established in member states to facilitate access to the virtual design platform and pilot lines. The opening of these pilot lines is intended to provide SMEs and startups with easier and faster access to foundry services for both novel and older technologies.

SME and start-up role in the value chain: Europe's semiconductor ecosystem, in terms of number of companies, is dominated by small and medium-sized enterprises, which account for roughly 69% of all firms across the value chain.

The EU hosts a large number of small and mid-sized champions in equipment, specialty materials, sensors and MEMS, power electronics, and optoelectronics, where innovation and domain expertise matter more than scale. However, it has far fewer successful scale-ups in fabless design and virtually no globally competitive EDA providers beyond Siemens EDA (the result of the acquisition of US-based Mentor Graphics by Siemens AG in 2017). This structural pattern mirrors Europe's technological strengths in optoelectronics, MEMS, and power semiconductors, but also its relative weakness in advanced logic design and digital system-on-chip innovation, where large U.S. and Asian firms dominate ([213]).

Access to finance and scale-up pathways: Persistent late-stage funding gaps constrain EU chip start-ups and fabless SMEs from moving beyond prototypes to growth manufacturing. Although policy instruments such as the Chips Fund and InvestEU exist on paper, Interface

([209]) Rosati, N., Bonnet, P., Ciani, A., Duch Brown, N., Miguez, S., & Zaurino, E. (2023). *The EC consultation on the semiconductors' value chain* (JRC133892, EUR 31585 EN).
([210]) DECISION Études & Conseil. (2024). *Economic analysis of the EU and global chips ecosystem.* European Commission, Directorate-General for Communications Networks, Content and Technology (DG CNECT).
([211]) DECISION Études & Conseil. (2024). *Economic analysis of the EU and global chips ecosystem.* European Commission, Directorate-General for Communications Networks, Content and Technology (DG CNECT).
([212]) Rosati, N., Bonnet, P., Ciani, A., Duch Brown, N., Miguez, S., & Zaurino, E. (2023). *The EC consultation on the semiconductors' value chain* (JRC133892, EUR 31585 EN).
([213]) Survey data collected by DG CNECT from Member States for Chips Act Pillar III mapping and elaborated by the JRC.

(2024) ([214]), IFRI (2024) ([215]), and JRC (2025) ([216]) note that investment capacity and deal flow remain limited compared with U.S. and Asian ecosystems. McKinsey (2024) ([217]) similarly highlights Europe's structural deficit in late-stage venture capital and corporate investment.

Access to shared infrastructure and tools: The Chips Act introduced a Design Platform (DP), a network of competence centres, pilot lines, and a Chips Fund precisely to lower barriers for SMEs and start-ups. These measures are designed to ease access to EDA/IP, multi-project wafers (MPWs), and expert support, and to blend equity/debt for young firms. Implementation is underway but still maturing; practical access and throughput for SMEs varies by Member State.

Administrative burden and access to support: Implementation of the Chips Act spans several overlapping instruments: the Chips Joint Undertaking, the Chips Fund, the Design Platform, national state-aid schemes under Pillar II and IPCEI ME2, as well as Horizon Europe and InvestEU windows. Each of them has a separate application, eligibility, and reporting requirements. For smaller firms, this multi-layered structure results in high fixed compliance costs and lengthy approval timelines. The **ECA (2025) ([218])** and Interface (2024) ([219]) note that the absence of a single-entry point and duplication between EU and national levels increase transaction costs, while IFRI (2024) ([220]) and JRC (2025) ([221]) highlight uneven administrative capacity across Member States, especially in State aid management. SMEs active in cross-border or pilot projects are particularly affected, as differing national procedures often require multiple notifications and audits. Large firms can absorb these costs through dedicated compliance resources, but smaller companies frequently withdraw or forgo participation. As a result, SMEs face slower access to support and lower participation rates in major semiconductor programmes.

2.2.2. Modelling the BAU scenario

2.2.2.1 Access to finance and scale-up

- **Developments expected under BAU:** Gradual improvement in seed and Series A availability is expected via the Chips Fund, the Design Platform, and InvestEU windows. However, little progress is anticipated at late-stage growth and expansion rounds, as these financing gaps stem from broader structural weaknesses in the EU capital market. These issues go beyond the scope of sector-specific instruments and

([214]) Kleinhans, J.-P. (2024), *The missing strategy in Europe's chip ambitions: Member States must drive the next steps*, Interface, July 2024.
([215]) Ebrahimi, A. (2024). *Groundbreaking chip sovereignty: Europe's strategic push in the semiconductor race.* Ifri Memos, Institut français des relations internationales (IFRI). ISBN 979-10-373-0874-0.
([216]) Bonnet, P., Ciani, A., Molnar, J., & Nardo, M. (2025). *EU's strengths and weaknesses in the global semiconductor sector* (JRC141323, EUR 40253). Luxembourg: Publications Office of the European Union. https://doi.org/10.2760/6302476
([217]) McKinsey & Company (2021), *McKinsey on Semiconductors: Creating value, pursuing innovation, and optimising operations.*
([218]) European Court of Auditors. (2025). *Special Report 12/2025 – The EU's strategy for microchips: Reasonable progress in its implementation, but the Chips Act is very unlikely to be sufficient to reach the overly ambitious Digital Decade target.* Luxembourg: Publications Office of the European Union.
([219]) Kleinhans, J.-P. (2024), *The missing strategy in Europe's chip ambitions: Member States must drive the next steps*, Interface, July 2024.
([220]) Ebrahimi, A. (2024). *Groundbreaking chip sovereignty: Europe's strategic push in the semiconductor race.* Ifri Memos, Institut français des relations internationales (IFRI). ISBN 979-10-373-0874-0.
([221]) Bonnet, P., Ciani, A., Molnar, J., & Nardo, M. (2025). *EU's strengths and weaknesses in the global semiconductor sector* (JRC141323, EUR 40253). Luxembourg: Publications Office of the European Union. https://doi.org/10.2760/6302476

cannot be resolved without deeper systemic reforms such as a functioning Capital Markets Union**.**

- **Rationale:** Interface (2024) ([222]) notes that while the Chips Act's instruments such as pilot lines, the competence centres and the Chips Fund formally exist, their strategic follow-through and implementation capacity remain limited. Member States differ markedly in how they execute and resource these instruments, creating uneven access for start-ups and SMEs. As a result, the transition from prototype development to commercial manufacturing remains constrained, and the pipeline from pilot to product is only partially functional under current conditions.
- **Implications for SMEs:** By 2028, many SMEs gain first access to the Chips Act's Design Platform and competence centres, improving their ability to design and prototype new chips. However, access to large-scale follow-on financing for industrialisation and scaling remain scarce, leaving promising fabless firms unable to design at leading edge nodes or move from prototype runs to market-ready production. Some relocate intellectual property or exit early to attract non-EU investment. The critical transition between Technology Readiness Levels 6 and 8 (the "valley of death") therefore remains a high-risk stage under BAU conditions, and this challenge is unlikely to be fully resolved even under alternative scenarios. The underlying barriers are structural – notably the shortage of late-stage capital, limited domestic demand-pull, and Europe's fragmented financing landscape – and extend beyond what sectoral instruments such as the Chips Act can realistically address.

2.2.2.2 Access to infrastructure and tools (DP, competence centres, pilot lines)

- **Developments expected under BAU:** Access to shared design and prototyping infrastructure improves gradually as the Virtual Design Platform, competence centres, and pilot lines reach maturity. SMEs benefit from expanded multi-project wafer services and more predictable conditions for EDA tools, alongside financial support, which lower entry barriers and accelerate prototyping. Bottlenecks, however, persist in securing affordable access to design tools, navigating heterogeneous access conditions across Member States, and obtaining timely technical assistance, reflecting broader coordination and capacity challenges rather than specific technical constraints**.**
- **Rationale:** Pillar I of the Chips Act was designed to also ease SME entry into semiconductor innovation, but practical capacity and coordination are still catching up, as noted by Interface (2024) ([223]) and the ECA (2025) ([224]).
- **Implications for SMEs:** Entry costs for first-time tape-outs and lab prototyping decline, improving time-to-prototype and customer validation. Yet cross-country disparities persist, and scaling beyond prototype remains constrained by dependence on non-EU foundries and OSATs.

Overall, by 2035, it is expected that the Design Platform, competence centres, and pilot lines will have expanded and become accessible, lowering entry barriers and improving prototyping speed for SMEs. Some regional clusters strengthen around Europe's established niches in

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([222])Kleinhans, J.-P. (2024), *The missing strategy in Europe's chip ambitions: Member States must drive the next steps*, Interface, July 2024.
([223]) Kleinhans, J.-P. (2024), *The missing strategy in Europe's chip ambitions: Member States must drive the next steps*, Interface, July 2024.
([224]) European Court of Auditors. (2025). *Special Report 12/2025 – The EU's strategy for microchips: Reasonable progress in its implementation, but the Chips Act is very unlikely to be sufficient to reach the overly ambitious Digital Decade target.*

equipment, materials, and power electronics. Yet core structural constraints persist and the late-stage financing gap remains wide.

2.3. R&D&I leadership in the EU semiconductor industry

Competitive advantage can be achieved through cost (and hence price) or the innovation, sophistication and quality of chips. As discussed in Section 1.3 of this annex, the EU holds a strong market position in the design and manufacture of analogue chips, radio-frequency (RF) components, sensors and MEMS, power semiconductors, microcontrollers, and silicon photonics ([225]), ([226]). European suppliers are global leaders in embedded systems serving strategic industrial sectors such as automotive, robotics, energy, healthcare, aerospace, defence, and telecommunications infrastructures ([227]), ([228]), ([229]). European firms such as STMicroelectronics, Infineon, Robert Bosch, and NXP are recognised global leaders in power electronics and sensors, particularly for heavy industrial and automotive uses ([230]), ([231]).

The EU is also home to world-class research and innovation centres, including IMEC in Belgium, CEA-Leti in France, and Fraunhofer in Germany, which have contributed to major technological breakthroughs in microelectronics ([232]), ([233]), ([234]).

Within the supply chain, the EU possesses a clear competitive advantage in manufacturing equipment, led by ASML in the Netherlands, the world's sole provider of extreme ultraviolet (EUV) lithography tools and with an 88% market share in the broader lithography market in 2022 ([235]), ([236]). Germany's Siemens also plays a critical role in electronic design software ([237]).

However, despite these strengths, the EU remains absent from the technological frontier of semiconductor innovation. It plays only a minor role in global chip design, accounting for about 9% of the global market ([238]), and lacks production capacity for the leading edge and advanced nodes (below 16 nm) ([239]), which are overwhelmingly concentrated in Taiwan and South Korea,

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([225]) DECISION Études & Conseil. (2024). *Economic analysis of the EU and global chips ecosystem.* European Commission, Directorate-General for Communications Networks, Content and Technology (DG CNECT).
([226]) Cerutti, I., Nardo, M., et al. (2024). *Applying the SCAN methodology to the Semiconductor Supply Chain.* JRC Technical Report, JRC141323. Publications Office of the European Union
([227]) European Semiconductor Industry Association. (2025). *Position paper on EU Chips Act 2*. Brussels: ESIA.
([228]) DECISION Études & Conseil. (2024). *Economic analysis of the EU and global chips ecosystem.* European Commission, Directorate-General for Communications Networks, Content and Technology (DG CNECT).
([229]) Cerutti, I., Nardo, M., et al. (2024). *Applying the SCAN methodology to the Semiconductor Supply Chain.* JRC Technical Report, JRC141323. Publications Office of the European Union
([230]) Ebrahimi, A. (2024). *Groundbreaking chip sovereignty: Europe's strategic push in the semiconductor race.* Ifri Memos, Institut français des relations internationales (IFRI). ISBN 979-10-373-0874-0.
([231]) Cerutti, Isabella & Nardo, Michela (2023). *Semiconductors in the EU: State of play, future trends and vulnerabilities of the semiconductor supply chain*. JRC Technical Report, JRC133850.
([232]) DECISION Études & Conseil. (2024). *Economic analysis of the EU and global chips ecosystem.* European Commission, Directorate-General for Communications Networks, Content and Technology (DG CNECT).
([233]) Cerutti, Isabella & Nardo, Michela (2023). *Semiconductors in the EU: State of play, future trends and vulnerabilities of the semiconductor supply chain*. JRC Technical Report, JRC133850.
([234]) Cerutti, I., Nardo, M., et al. (2024). *Applying the SCAN methodology to the Semiconductor Supply Chain.* JRC Technical Report, JRC141323. Publications Office of the European Union
([235]) DECISION Études & Conseil. (2024). *Economic analysis of the EU and global chips ecosystem.* European Commission, Directorate-General for Communications Networks, Content and Technology (DG CNECT).
([236]) Ebrahimi, A. (2024). *Groundbreaking chip sovereignty: Europe's strategic push in the semiconductor race.* Ifri Memos, Institut français des relations internationales (IFRI). ISBN 979-10-373-0874-0.
([237]) Ebrahimi, A. (2024). *Groundbreaking chip sovereignty: Europe's strategic push in the semiconductor race.* Ifri Memos, Institut français des relations internationales (IFRI). ISBN 979-10-373-0874-0.
([238]) Ebrahimi, A. (2024). *Groundbreaking chip sovereignty: Europe's strategic push in the semiconductor race.* Ifri Memos, Institut français des relations internationales (IFRI). ISBN 979-10-373-0874-0.
([239]) IDC. (2025). Semiconductors D3: Second interim study report (Version 3.0). Prepared for the European Commission.

with a smaller share in the US ([240]), ([241]). Most EU production focuses on mature nodes (40 nm and above), serving industrial and automotive demand rather than leading-edge computing applications ([242]). Europe also lacks large-scale pure-play foundries and depends on other regions for advanced-node manufacturing ([243]). In addition, Europe's strong public research base does not consistently translate into industrial leadership. Although organisations such as IMEC, CEA-Leti and Fraunhofer develop world-class technologies, commercialisation channels and scaling partnerships remain limited and many innovations pioneered in European pilot lines are industrialised in non-EU foundries. While the EU benefits from a growing base of innovative fabless startups, collaboration between large incumbents and smaller firms remains limited ([244]). Finally, structural barriers, including fragmented markets, and complex regulatory environments, further constrain the translation of research into competitive industrial capacity. As a result, the EU's semiconductor ecosystem shows high technological sophistication but does not convert its research excellence into global leadership in advanced chip design and manufacturing ([245]),([246]).

2.3.1. Establishing a starting point for BAU scenario

Quantitative indicators of R&D and innovation effort

The EU semiconductor ecosystem demonstrates high R&D intensity but remains structurally constrained in scale, market penetration, advanced-node chip design and high-volume manufacturing, despite strong European leadership in process research and enabling technologies such as EUV lithography. The table below summarises the key indicators that define the 2023 starting point, benchmarked against major global competitors.

Table 13. Starting point for R&D and innovation BAU. *Source: Compiled by the authors.*

Indicator	Indicative EU figure (2023)	Benchmark comparison	Reference and justification
Effectiveness of technology transfer	Low to moderate; a significant	Higher conversion	JRC (2025) ([247]) highlights fragmentation between research and

([240]) Ebrahimi, A. (2024). *Groundbreaking chip sovereignty: Europe's strategic push in the semiconductor race.* Ifri Memos, Institut français des relations internationales (IFRI). ISBN 979-10-373-0874-0.
([241]) DECISION Études & Conseil. (2024). *Economic analysis of the EU and global chips ecosystem.* European Commission, Directorate-General for Communications Networks, Content and Technology (DG CNECT).
([242]) DECISION Études & Conseil. (2024). *Economic analysis of the EU and global chips ecosystem.* European Commission, Directorate-General for Communications Networks, Content and Technology (DG CNECT).
([243]) DECISION Études & Conseil. (2024). *Economic analysis of the EU and global chips ecosystem.* European Commission, Directorate-General for Communications Networks, Content and Technology (DG CNECT).
([244]) DECISION Études & Conseil. (2024). *Economic analysis of the EU and global chips ecosystem.* European Commission, Directorate-General for Communications Networks, Content and Technology (DG CNECT).
([245]) Cerutti, Isabella & Nardo, Michela (2023). *Semiconductors in the EU: State of play, future trends and vulnerabilities of the semiconductor supply chain*. JRC Technical Report, JRC133850.
([246]) Bonnet, P., Ciani, A., Molnar, J., & Nardo, M. (2025). *EU's strengths and weaknesses in the global semiconductor sector* (JRC141323, EUR 40253). Luxembourg: Publications Office of the European Union. https://doi.org/10.2760/6302476
([247]) European Commission, Joint Research Centre (JRC). (2025). *EU's strengths and weaknesses in the global semiconductor sector (JRC141323).* Luxembourg: Publications Office of the European Union.

(lab-to-fab conversion of research outputs)	proportion of pilot-line technologies are industrialised outside the EU	rates in the US, Taiwan, and South Korea	manufacturing; ECA (2025) (**[248]**) notes that technology developed in EU pilot lines is frequently scaled abroad; IFRI (2024) (**[249]**) and BCG & SIA (2024) (**[250]**) underline the absence of large-scale EU foundries capable of absorbing advanced research.
R&D intensity (R&D expenditure as % of semiconductor revenue)	≈ 22 % (± 2 pp)	Global average ~22 % (U.S. 23 %; Asia 21 %)	**McKinsey & Company (2025) (**[251]**)**: "Semiconductor industry averages about 22 % of revenue in R&D." **Deloitte (2021) (**[252]**)**: "Typically reinvest 20–25 % of revenue in R&D." **Company reports**: ASML 15 %, Infineon 14 %, ST 13 %, NXP 16 %. Adjusted upward for Europe's strong public-research component gives ≈ 22 %.
Share of global semiconductor R&D spending	≈ 9–10 % (± 2 pp)	U.S. ≈ 50 %; Asia ≈ 35 %	**McKinsey (2024) (**[253]**)**: Europe's revenue share ≈ 10 % of global industry → assumed proportional R&D share. JRC (2025) **(**[254]**)** reports EU accounts for roughly 10% of semiconductor value-added. Given that semiconductor R&D intensity is relatively constant worldwide (around 20–25 % of revenue; McKinsey 2025; Deloitte 2021), it is reasonable to assume that regional R&D spending scales proportionally with regional industry revenue. Accordingly, Europe's approximate 10% share of global semiconductor revenue implies a

([248]) European Court of Auditors. (2025). *Special Report 12/2025 – The EU's strategy for microchips: Reasonable progress in its implementation, but the Chips Act is very unlikely to be sufficient to reach the overly ambitious Digital Decade target.*
([249]) Ebrahimi, A. (2024). *Groundbreaking chip sovereignty: Europe's strategic push in the semiconductor race.* Ifri Memos, Institut français des relations internationales (IFRI). ISBN 979-10-373-0874-0.
([250]) **Boston Consulting Group (BCG) & Semiconductor Industry Association (SIA).** (May 2024). *Emerging Resilience in the Semiconductor Supply Chain.*
([251]) **McKinsey & Company (2025).** *Semiconductors have a big opportunity but barriers to scale remain.* February 2025.
([252]) **Deloitte.** (2021). *Measuring semiconductors' economic impact.* Deloitte Insights.
([253]) McKinsey & Company. (2024). *McKinsey on Semiconductors: Creating value, pursuing innovation, and optimizing operations.* McKinsey & Company.
([254]) European Commission, Joint Research Centre (JRC). (2025). *EU's strengths and weaknesses in the global semiconductor sector (JRC141323).* Luxembourg: Publications Office of the European Union.

			similar order of magnitude for its share of global R&D expenditure (≈ 9–10 %).
Share of global chip-design market	≈ 9 %	`U.S. ≈ 60 %; China ≈ 16 %; Taiwan ≈ 8 %	**JRC (2025) ([255])**: EU ≈ 9 % of global chip-design revenue (including European IDMs). **BCG & SIA (2024) ([256])**: "The US retains > 60 % of global chip-design."
Share of global advanced-node patents (< 16 nm)	< 5 %	Dominated by U.S., Taiwan, Korea	JRC (2025), IFRI (2024), and BCG–SIA (2024) show that the EU has limited domestic production capacity at <16 nm except for the Intel manufacturing in Leixlip, Ireland. Advanced-node process innovation is concentrated in Taiwan (TSMC), South Korea (Samsung) and the US (Intel and leading U.S. design–EDA ecosystems), though IMEC and CEA-Leti are innovating a lot for manufacturing below 2nm and FD-SOI below 7nm. Outside of the patents hold by RTOs, European patenting strength lies in equipment, materials, lithography and photonics rather than advanced CMOS logic. Given the strong correlation between leading-edge manufacturing and process-technology patenting, Europe's share of <16 nm patents is therefore inferred to be very small, typically estimated at below 5 %.
Top 10 EDA/design-tool vendors headquartered in EU	1 (Siemens EDA)	3 in U.S.	**IFRI (2024) ([257])**: lists Siemens EDA as Europe's sole global-tier EDA provider.
Public R&D funding for microelectronics (EU + MS)	≈ EUR 3–4 billion annually	U.S./Asia ≈ EUR 7–15 billion	**ECA (2025) ([258])**: notes Chips Act public component "covers a small fraction" of global subsidies; combined EU-level and national

([255]) European Commission, Joint Research Centre (JRC). (2025). *EU's strengths and weaknesses in the global semiconductor sector (JRC141323).* Luxembourg: Publications Office of the European Union.
([256]) **Boston Consulting Group (BCG) & Semiconductor Industry Association (SIA).** (May 2024). *Emerging Resilience in the Semiconductor Supply Chain.*
([257]) Ebrahimi, A. (2024). *Groundbreaking chip sovereignty: Europe's strategic push in the semiconductor race.* Ifri Memos, Institut français des relations internationales (IFRI). ISBN 979-10-373-0874-0.
([258]) European Court of Auditors. (2025). *Special Report 12/2025 – The EU's strategy for microchips: Reasonable progress in its implementation, but the Chips Act is very unlikely to be sufficient to reach the overly ambitious Digital Decade target.*

			programmes ≈ EUR 43 billion over 2021–2030, this translates to an annual average of roughly EUR 4 billion per year.

2.3.2. Modelling the BAU scenario

In the BAU model, we explicitly assume that Europe's strong research base does not translate proportionally into industrial capacity, due to persistent lab-to-fab bottlenecks, limited domestic absorption capacity, and structural fragmentation. As a result, R&D inputs increase, but technology-transfer outcomes remain modest, in line with the evidence from JRC (2025) **([259])**, ECA (2025) **([260])**, IFRI (2024) **([261])**, and BCG–SIA (2024) **([262])**.

Technology transfer and industrial scaling (lab-to-fab)

- **Developments expected under BAU**: Under the business-as-usual scenario, Europe's pilot lines continue to generate high-quality scientific outputs in advanced logic, power electronics, compound semiconductors, photonics, and materials engineering. However, the rate of industrial uptake remains limited. Most European IDMs operate at mature nodes and demonstrate only partial incentives to integrate new process modules that require costly requalification. The EU's limited presence in advanced-node manufacturing further restricts opportunities for domestic scaling. Consequently, although pilot lines strengthen Europe's technological capabilities, a significant share of innovations is expected to be commercialised in non-EU foundries where larger design ecosystems and high-volume manufacturing platforms are available.
- **Rationale**: Evidence from the JRC (2025) ([263]), IFRI (2024) ([264]), and BCG–SIA (2024) ([265]) shows that the EU's innovation pipeline is weakened by structural fragmentation between research organisations, early-stage firms, and large industrial players. The ECA (2025) ([266]) stresses that technologies developed within EU-funded pilot lines are often industrialised abroad, underscoring limited domestic absorption capacity. In contrast, the US, Taiwan, and South Korea benefit from dense co-development ecosystems in which research institutes, EDA suppliers, design houses, and advanced foundries jointly validate and scale innovations. Without a comparable industrial base, Europe's capability to transform research excellence into competitive market positions remains constrained.
- **Implication for competitiveness**: Under BAU, Europe's research institutions consolidate their position as global leaders in semiconductor science, but the Union

([259]) European Commission, Joint Research Centre (JRC). (2025). *EU's strengths and weaknesses in the global semiconductor sector (JRC141323).* Luxembourg: Publications Office of the European Union.
([260]) European Court of Auditors. (2025). *Special Report 12/2025 – The EU's strategy for microchips: Reasonable progress in its implementation, but the Chips Act is very unlikely to be sufficient to reach the overly ambitious Digital Decade target.*
([261]) Ebrahimi, A. (2024). *Groundbreaking chip sovereignty: Europe's strategic push in the semiconductor race.* Ifri Memos, Institut français des relations internationales (IFRI). ISBN 979-10-373-0874-0.
([262]) **Boston Consulting Group (BCG) & Semiconductor Industry Association (SIA).** (May 2024). *Emerging Resilience in the Semiconductor Supply Chain.*
([263]) European Commission, Joint Research Centre (JRC). (2025). *EU's strengths and weaknesses in the global semiconductor sector (JRC141323).* Luxembourg: Publications Office of the European Union.
([264]) Ebrahimi, A. (2024). *Groundbreaking chip sovereignty: Europe's strategic push in the semiconductor race.* Ifri Memos, Institut français des relations internationales (IFRI). ISBN 979-10-373-0874-0.
([265]) Boston Consulting Group (BCG) & Semiconductor Industry Association (SIA). (May 2024). *Emerging Resilience in the Semiconductor Supply Chain.*
([266]) European Court of Auditors. (2025). *Special Report 12/2025 – The EU's strategy for microchips: Reasonable progress in its implementation, but the Chips Act is very unlikely to be sufficient to reach the overly ambitious Digital Decade target.*

makes only modest progress in commercialising these advances domestically. Weak lab-to-fab scaling reduces the economic return on public R&D investment, slows the emergence of European design champions, and allows competing regions to capture value added from technologies that originate in Europe. As a result, Europe's innovation strengths translate into incremental rather than structural competitiveness gains in high-growth semiconductor segments.

R&D intensity (R&D as % of semiconductor revenue)

- **Developments expected under BAU:** The European semiconductor ecosystem maintains a structurally high R&D intensity. Newly built fabs in Ireland, France, Germany, and Italy reinforce the applied-research interface between equipment suppliers, materials firms, and integrated device manufacturers. Pilot lines increase Europe's leadership in the development of process technology. However, these additions mainly broaden production rather than altering the R&D-to-revenue ratio, which remains close to the global average.
- **Rationale:** McKinsey (2025) ([267]) and Deloitte (2021) ([268]) find that R&D intensity in semiconductors is remarkably uniform worldwide at about one-fifth of revenue. Company data for ASML, Infineon, STMicroelectronics, and NXP confirm that European firms already operate within this band. Neither new subsidies nor new fabs are expected to change this structural parameter.
- **Implication for competitiveness:** The EU sustains a world-class research effort and strong public-private science base, but high R&D intensity alone does not guarantee technological leadership. Without greater design scale or faster commercialisation, high R&D effort continues to yield incremental rather than transformational advantages.

Share of global semiconductor R&D spending

- **Developments expected under BAU:** Absolute R&D spending in Europe rises as new fabs and pilot lines come online, yet the EU's global share changes little. Growth elsewhere, particularly in Asia and the US, keeps relative positions broadly stable through 2035. European technology developed in the pilot lines is industrialised elsewhere.
- **Rationale:** Global R&D intensity remains constant, meaning regional spending scales with output. Europe's announced fabs expand capacity but not enough to alter the global distribution. The ECA (2025) ([269]) and JRC (2025) ([270]) both note that current investment levels are modest compared with the subsidy waves in Asia and North America.
- **Implication for competitiveness:** Europe strengthens its applied-research network and process-engineering skills, but its overall share of global semiconductor R&D remains modest. Without a wider industrial base, Europe's innovation influence grows only gradually.

([267]) **McKinsey & Company (2025).** *Semiconductors have a big opportunity but barriers to scale remain.* February 2025.
([268]) **Deloitte.** (2021). *Measuring semiconductors' economic impact.* Deloitte Insights.
([269]) European Court of Auditors. (2025). *Special Report 12/2025 – The EU's strategy for microchips: Reasonable progress in its implementation, but the Chips Act is very unlikely to be sufficient to reach the overly ambitious Digital Decade target.*
([270]) European Commission, Joint Research Centre (JRC). (2025). *EU's strengths and weaknesses in the global semiconductor sector (JRC141323).* Luxembourg: Publications Office of the European Union.

Share of global chip-design market

- **Developments expected under BAU:** The EU's design activity grows within its established strengths such as embedded systems, automotive, industrial control, and RF/power electronics. New FD-SOI and automotive-logic fabs stimulate local design collaboration but this does not alter Europe's marginal position in the global fabless design market, which remains dominated by U.S. and Asian firms.
- **Rationale:** The JRC (2025) ([271]) reports that Europe accounts for around 9 % of global design revenues when including design carried out within IDMs and embedded-system suppliers, while the BCG & SIA (2024) ([272]) estimate that the US retains more than 60 %. However, Europe's share of the global **fabless semiconductor market**, the segment that defines global competitiveness in advanced chip design, is **below 1 %**, according to IFRI (2024) and BCG–SIA (2024). This reflects both the limited scale of Europe's fabless sector and persistent dependence on non-EU EDA tools and manufacturing ecosystems.
- **Implication for competitiveness:** Incremental design growth reinforces Europe's role in high-reliability and industrial segments but Europe's position in globally competitive fabless design remains largely unchanged. Limited EDA autonomy, scale constraints, and shallow late-stage venture capital restrict the emergence of European design champions capable of competing in leading-edge markets.

Share of global advanced-node patents

- **Developments expected under BAU:** Most leading-edge process patents continue to originate outside the EU. New facilities hosting advanced-node production (e.g. Intel Ireland and ESMC Dresden) operate with process IP developed abroad. European patenting remains concentrated in enabling technologies, notably EUV lithography, advanced metrology, power devices, SiC/GaN, and photonics. These fields are at the cutting edge of semiconductor innovation, but they do not substitute for the scale and design ecosystems required for advanced-node CMOS process development.
- **Rationale:** Bruegel (2025) ([273]) shows that the EU accounts for only a small fraction of radical innovation patents ([274]), while McKinsey (2025) ([275])and JRC (2025) ([276]) confirm that Europe's innovation strength lies upstream in equipment and materials rather than node development.
- **Implication for competitiveness:** The EU maintains technological leadership in production equipment and materials science, but it does not close the frontier gap in logic and memory process innovation. Its comparative advantage remains in enabling rather than defining the leading edge.

([271]) European Commission, Joint Research Centre (JRC). (2025). *EU's strengths and weaknesses in the global semiconductor sector (JRC141323).* Luxembourg: Publications Office of the European Union.
([272]) **Boston Consulting Group (BCG) & Semiconductor Industry Association (SIA).** (May 2024). *Emerging Resilience in the Semiconductor Supply Chain.*
([273]) Bruegel. (2025). *Europe's technological divide: Radical novelties, diffusion, and the global race for frontier innovation* (Working Paper 07/2025). Brussels: Bruegel. https://www.bruegel.org/sites/default/files/2025-07/WP%2007%202025.pdf
([274]) Patent families representing entirely new combinations of technology codes in the global patent system. In semiconductors, these identify frontier breakthroughs in materials, device structures, and manufacturing processes. Between 2019 and 2023, the EU produced only 804 such patents, compared with 3 203 in the US and 2 892 in China.
([275]) **McKinsey & Company (2025).** *Semiconductors have a big opportunity but barriers to scale remain.* February 2025.
([276]) European Commission, Joint Research Centre (JRC). (2025). *EU's strengths and weaknesses in the global semiconductor sector (JRC141323).* Luxembourg: Publications Office of the European Union.

Public R&D funding for microelectronics (EU + Member States)

- **Developments expected under BAU:** Public support through the Chips Act, IPCEI ME2, and national programmes remains broadly stable at around the current annual level. Funding streams shift towards construction phases of the new fabs but remain modest compared with U.S. and Asian subsidy envelopes.
- **Rationale:** ECA (2025) ([277]) calculates combined EU and Member-State commitments at about EUR 11 billion over 2021–2030 and describes this as "a small fraction" of global support. The JRC (2025) ([278]) confirms that Asian and U.S. programmes are considerably larger in scale and faster in implementation.
- **Implication for competitiveness:** Existing funding is sufficient to maintain Europe's strong research institutions and pilot lines but not to transform its position in global innovation hierarchies. Without a significant increase in scale or focus on design and back-end innovation, structural gaps persist.

3. REGIONAL AND TERRITORIAL EFFECTS

3.1. Establishing a starting point for BAU scenario

The European semiconductor landscape is **polycentric but highly uneven**. A handful of core clusters such as **Leuven-Eindhoven (Belgium – the Netherlands), the Dresden area / Saxony (Germany), the Munich area (Germany), the Grenoble area (France), Ireland, the axis Graz-Villach (Austria), and the axis Milano-Turino (Italy)** account for the majority of industrial output, R&D investment, and employment. Other regions contribute mainly through packaging, materials, or design services ([279]).

The six core clusters, that collectively cover less than **8 % of the EU population**, account for the vast majority of semiconductor value creation. Data from **McKinsey (2025) ([280])** indicate that approximately **80 % of wafer-fabrication capacity** and **over 70 % of semiconductor-related R&D personnel** are concentrated in these areas, confirming Europe's exceptionally high locational concentration relative to other advanced industries.

The **Joint Research Centre ([281])** similarly identifies this pattern as one of *geographical lock-in*, where existing clusters continue to attract incremental investment due to cumulative advantages in know-how, infrastructure, and established industrial ecosystems. These regions have become self-reinforcing "centres of gravity" within the European semiconductor landscape, benefiting disproportionately from new fab announcements under the Chips Act and IPCEI ME2.

([277]) European Court of Auditors. (2025). *Special Report 12/2025 – The EU's strategy for microchips: Reasonable progress in its implementation, but the Chips Act is very unlikely to be sufficient to reach the overly ambitious Digital Decade target.*
([278]) European Commission, Joint Research Centre (JRC). (2025). *EU's strengths and weaknesses in the global semiconductor sector (JRC141323).* Luxembourg: Publications Office of the European Union.
([279]) DECISION Études & Conseil (2024), *Mapping of the European Semiconductor Industry and Value Chain: Company Distribution, Regional Clusters and Investment Dynamics*, study prepared for DG CONNECT, European Commission, Brussels.
([280]) McKinsey & Company (2025), *Semiconductors Have a Big Opportunity, but Barriers to Scale Remain*, McKinsey Global Institute, April 2025.
([281]) European Commission, Joint Research Centre (2025), *EU's Strengths and Weaknesses in the Global Semiconductor Sector*, Publications Office of the European Union, Luxembourg, doi:10.2760/6302476.

JRC (2025) ([282]) explains that more than **85 % of EU semiconductor exports** originate in just five Member States (Germany, France, the Netherlands, Ireland, and Austria), underscoring the strong asymmetry between core and peripheral regions. **McKinsey (2024) ([283])** also notes that semiconductor ecosystems exhibit strong *path-dependence*: once established, clusters maintain durable competitive advantages through cumulative knowledge spillovers and sunk infrastructure costs, making it extremely difficult for new regions to catch up without major coordinated interventions.

The European semiconductor system thus exhibits certain regional specialisations

- Regions with broad semiconductor activity (Dresden, Grenoble, Eindhoven–Leuven, Munich, Ireland, Milano-Turino, and Graz–Vienna) host IDMs, equipment suppliers, and major R&D institutes.
- Regions with focused technological specialisations (Catania, Regensburg, Villach, Brno, and Wrocław) concentrate on areas including power electronics, metrology, and automotive applications.
- Regions with strong support and complementary activities (Portugal, Hungary, parts of Eastern and Southern Europe) primarily host assembly, testing, or material-processing activities which are more labour intensive.

This division reflects both market forces and policy design: state-aid frameworks and investment incentives have largely supported existing industrial bases where returns are highest, rather than diffusing activity geographically. The **ECA (2025) ([284])** confirms that national co-financing under the Chips Act and IPCEI schemes has been predominantly channelled toward incumbent centres, given their readiness and project scale.

Economic and policy implications

The current degree of concentration delivers clear **efficiency gains** through agglomeration, but it raises **territorial cohesion concerns**:

- **Positive effects:**
  - Deepened regional specialisation and productivity gains from clustering.
  - Enhanced innovation networks between firms, research institutes, and universities.
  - Economies of scale in infrastructure, logistics, and skilled-labour attraction.
- **Negative effects:**
  - Persistent **geographic inequality** between innovation-intensive regions and the rest of the EU.
  - **Barriers to entry** for emerging regions lacking pre-existing semiconductor capacity or infrastructure.
  - **Skill and wage polarisation**, as talent and investment concentrate further in core clusters.

([282]) Bonnet, P., Ciani, A., Molnar, J., & Nardo, M. (2025). *EU's strengths and weaknesses in the global semiconductor sector* (EUR 40253 EN). Luxembourg: Publications Office of the European Union. https://doi.org/10.2760/6302476
([283]) McKinsey & Company. (2024). *McKinsey on semiconductors: Creating value, pursuing innovation, and optimizing operations.* New York: McKinsey Global Institute.
([284]) European Court of Auditors. (2025). *Special report 12/2025: The EU's strategy for microchips – Reasonable progress in its implementation, but the Chips Act is very unlikely to be sufficient to reach the overly ambitious Digital Decade target.*

3.2. Modelling the BAU scenario

Under a **Business-as-usual (BAU)** trajectory, Europe's semiconductor geography remains **highly concentrated and path-dependent**. The major industrial and research hubs established before 2025 continue to attract the vast majority of investments, talent, and public support. While new fabs and R&D facilities expand capacity within existing clusters, there is limited diffusion of semiconductor activity to peripheral regions. This results in gradual strengthening of existing agglomerations rather than a structural shift in the European territorial landscape.

Developments expected under BAU

Continuation of core-cluster dominance. Between 2025 and 2035, announced semiconductor investments, including **Intel Ireland, STMicroelectronics–GlobalFoundries Crolles**, **ESMC Dresden**, **Infineon Dresden and Villach**, and **Catania SiC Campus**, consolidate existing regional ecosystems rather than create new ones. By 2035, approximately **80 % of EU semiconductor employment and value added** remains concentrated in the same six core clusters.

Peripheral or emerging regions (e.g. Poland, Czech Republic, Hungary, Portugal, southern Italy) experience moderate growth through supplier linkages, logistics, and equipment sub-contracting but remain secondary players. This spatial concentration mirrors the industrial geography of other global semiconductor ecosystems, such as the U.S. *'Silicon Triangle'* (linking California, Arizona, and Texas) and the East Asian manufacturing corridor connecting Taiwan, Japan, and South Korea ([285])[,] [286].

Limited emergence of new hubs. Despite EU policy efforts to enhance territorial cohesion, most **new greenfield fabs and pilot lines** locate near existing ecosystems to exploit established infrastructure, supplier proximity, and skilled labour pools. New entrants in Central and Eastern Europe mainly target packaging, assembly, or materials production rather than high-value design or advanced-node manufacturing. **JRC (2025) ([287])** projects that under current policies, fewer than **20 % of new semiconductor investments** by 2035 will occur outside the existing top-tier regions.

Cross-border consolidation and functional integration. Core regions become increasingly interconnected across borders, forming a **North-Central European semiconductor corridor** linking the Netherlands, Belgium, Germany, France, and Austria. Industrial interdependencies, e.g. between ASML (Netherlands) and imec (Belgium) strengthen vertical integration within this corridor. This cross-border clustering reinforces Europe's strengths in equipment, materials, and power devices but further marginalises outer regions.

Regional spillovers and supplier linkages. Peripheral regions benefit from indirect employment and supply chain effects during fab construction and through service provision.

([285]) McKinsey & Company. (2025). *Semiconductors have a big opportunity, but barriers to scale remain.* New York: McKinsey Global Institute.
([286]) Boston Consulting Group (BCG) & Semiconductor Industry Association (SIA). (2024). *Emerging resilience in the semiconductor supply chain.* May 2024. Boston: Boston Consulting Group and Semiconductor Industry Association.
([287]) Bonnet, P., Ciani, A., Molnar, J., & Nardo, M. (2025). *EU's strengths and weaknesses in the global semiconductor sector* (EUR 40253 EN). Luxembourg: Publications Office of the European Union. https://doi.org/10.2760/6302476

Supplier multipliers estimated by **Deloitte (2021) ([288])** and **McKinsey (2024) ([289])** suggest that each direct semiconductor job supports 5–6 indirect jobs, mainly in construction, utilities, and logistics. However, these spillovers remain largely **localised near established hubs**; broader diffusion toward less developed regions is minimal without additional policy intervention.

Rationale and evidence base

The persistence of concentration under BAU reflects several reinforcing factors:

1. **Infrastructure and sunk capital:** Semiconductor fabs and equipment clusters are among the most capital-intensive industrial assets, creating long-term lock-in effects once located. **McKinsey (2025) ([290])** explains that global semiconductor investments show strong path-dependence due to the high irreversibility of capital expenditure and skill accumulation.
2. **Talent availability:** The **European Chips Skills Academy ([291])** and **JRC (2025) ([292])** highlight persistent labour shortages, with engineering and technician gaps particularly acute outside existing hubs. Firms therefore concentrate expansion where talent pools and training infrastructure already exist. Although Competence Centres are being established in all Member States to broaden access to design support, specialised training, and prototyping services, their impact under BAU is expected to improve participation rather than materially shift the location of large-scale industrial investments.
3. **Network and innovation effects:** Co-location of R&D, suppliers, and production drives economies of scope. **BCG (2024) ([293])** notes that advanced-packaging and materials innovation depend on physical proximity between design centres and fabs, favouring the established clusters.
4. **Policy structure:** State-aid rules and IPCEI frameworks incentivise large-scale projects requiring national co-financing. ECA (2025) ([294]) reports that this has channelled most support to high-capacity incumbents in Germany, France, Ireland, and the Netherlands, limiting the potential for geographical diversification. While Competence Centres provide nationwide support services, they do not alter the underlying factors shaping the siting of major manufacturing projects under BAU.

Implications

Regional concentration and productivity. Under BAU, the **top six NUTS-2 regions** slowly increase their combined share of semiconductor-related value added, driven by cumulative investment and productivity gains. Agglomeration effects enhance efficiency and innovation

([288]) Deloitte. (2021). *Measuring semiconductors' economic impact: How many jobs does the semiconductor industry create?* Deloitte Insights, September 2021.
([289]) McKinsey & Company. (2024). *McKinsey on semiconductors: Creating value, pursuing innovation, and optimizing operations.* New York: McKinsey Global Institute.
([290]) McKinsey & Company. (2025). *Semiconductors have a big opportunity, but barriers to scale remain.* New York: McKinsey Global Institute.
([291]) European Chips Skills Academy. (2024). ECSA Skills Strategy 2024 (rev 20052025). https://chipsacademy.eu/wp-content/uploads/2025/05/ECSA-Skills-Strategy-2024-rev-20052025.pdf
([292]) Bonnet, P., Ciani, A., Molnar, J., & Nardo, M. (2025). *EU's strengths and weaknesses in the global semiconductor sector* (EUR 40253 EN). Luxembourg: Publications Office of the European Union. https://doi.org/10.2760/6302476
([293]) Boston Consulting Group. (2024). *Advanced packaging is reshaping the chip industry.* Boston: Boston Consulting Group, February 2024.
([294]) European Court of Auditors. (2025). *Special Report 12/2025 – The EU's strategy for microchips: Reasonable progress in its implementation, but the Chips Act is very unlikely to be sufficient to reach the overly ambitious Digital Decade target.*

capacity but create **structural divergence** between high-performing clusters and lagging regions.

Labour markets and skills. Regional labour-market effects mirror the overall pattern of agglomeration. Core regions face **tight labour markets** and wage pressures, while peripheral regions experience limited job creation. Cross-border mobility of engineers remains insufficient to offset regional imbalances, as **McKinsey (2024) ([295])** and **ECSA (2024) ([296])** report.

Environmental and infrastructure pressures. High-capacity clusters such as Dresden, Crolles–Grenoble, and Dublin experience growing strain on local **energy and water systems**, reinforcing regional environmental pressures identified in section 3.3. In contrast, potential sites with available capacity in peripheral regions remain underutilised.

Overall, under BAU conditions, the **regional geography of Europe's semiconductor industry remains largely unchanged through 2035**.

- Existing high-tech clusters consolidate their dominance, benefiting from cumulative investment, infrastructure, and skills ecosystems.
- Cross-border integration between Benelux, Germany, France, and Austria forms a competitive "semiconductor corridor", but without significant geographic expansion.
- Peripheral Member States gain limited spillovers, primarily through supply chain participation and service contracts, without achieving substantial localisation of high-value activities.
- Territorial cohesion objectives therefore remain only partially fulfilled, as structural imbalances persist between innovation-intensive core regions and industrial peripheries.

4. MODELLING ENVIRONMENTAL IMPACTS

4.1. Environmental impacts

4.1.1. Establishing a starting point for BAU scenario

When addressing sustainability in semiconductor manufacturing, attention often alternates between climate-related and broader environmental considerations. Climate concerns primarily pertain to greenhouse gas (GHG) emissions, including those from high global warming potential (GWP) gases and the energy consumption associated with raw materials mining and processing as well as chemicals refinement and wafer fabrication. These factors are commonly monitored using the Greenhouse Gas (GHG) Protocol, a widely adopted and standardised global framework.

Regarding the climate impact of chip production in Europe, scope 1 (mainly fluorinated gases) and scope 2 (mainly energy consumption) emissions are dominating the sectors carbon footprint (see below). ([297]) Scope 3 covers emissions across the entire value chain, both upstream and downstream. Semiconductor manufacturers generally do not report the climate footprint of their

([295]) McKinsey & Company. (2024). *McKinsey on semiconductors: Creating value, pursuing innovation, and optimizing operations.* New York: McKinsey Global Institute.
([296]) European Chips Skills Academy. (2024). ECSA Skills Strategy 2024 (rev 20052025). https://chipsacademy.eu/wp-content/uploads/2025/05/ECSA-Skills-Strategy-2024-rev-20052025.pdf
([297]) Interface (2024). Chip Production's Ecological Footprint: Mapping Climate and Environmental Impact. https://www.interface-eu.org/publications/chip-productions-ecological-footprint

products, as these are classified as *intermediate goods*. This lack of disclosure, combined with limited research on the ecological footprint during end-product operation, makes it challenging to obtain reliable and granular data on overall environmental impacts. ([298]) It is nevertheless important to note that the ecological impact during the operational phase of end-products varies substantially depending on their final application. Battery-powered devices such as tablets and smartphones exhibit higher emissions during manufacturing, whereas data centres - characterised by intensive energy use - generate significant emissions during operation. This issue is particularly pronounced in GPU-based data centres used for artificial intelligence (AI), where extreme thermal stress leads to accelerated hardware degradation. As a result, GPUs often need to be replaced every two to four years, a phenomenon known as *chip aging*.

Environmental considerations, by contrast, encompass aspects such as water consumption, the ecological impacts of raw material extraction, risks of chemical contamination to ecosystems and human health via forever chemicals (such as PFAS), and the challenges of waste management arising from chip production and electronic device end-of-life processes. In addition, greenfield investments are requiring massive land to host the large-scale clean-room infrastructure. ([299])

Scope 1 emissions (direct emissions) and PFAS

The environmental impacts of semiconductor production in the EU are regulated, inter alia, by Regulation (EU) No 2024/573 on fluorinated greenhouse gases (F-gases). F-gases are human-made chemicals that are very strong greenhouse gases (GHG), often several thousand times stronger than carbon dioxide (CO_2). Under the F-gas Regulation, the semiconductor industry sector is covered by a prohibition to intentionally emit F-gases as well as requirements to take technically and economically feasible measures to minimise unintentional ("leakage") of these gases. These rules have been reinforced recently with the new 2024 update of the Regulation.

While the production of semiconductors uses some of the F-gases with the highest global warming potential (e.g. trifluoromethane (HFC-23), perfuorocarbons (PFCs), nitrogen trifluoride (NF_3), sulphur hexafluoride (SF_6) etc.), the quantities are still modest amounting currently to about a few percent of total current F-gas emissions in the EU. ([300])

Generally, the EU semiconductor industry is taking stricter measures during its manufacturing processes to prevent emitting F-gases compared to other world regions. The sector is claiming to have made substantial investments to implement reduction practices at operations across Europe. The European Semiconductor Industry Association (ESIA) estimated in 2021 that the industry had achieved a 42% absolute emission reduction of PFCs between 2010 and 2020. ([301]) If looked at from a global perspective, an increased and significant production of

([298]) Interface (2024). Chip Production's Ecological Footprint: Mapping Climate and Environmental Impact. https://www.interface-eu.org/publications/chip-productions-ecological-footprint

([299]) Interface (2024). Chip Production's Ecological Footprint: Mapping Climate and Environmental Impact. https://www.interface-eu.org/publications/chip-productions-ecological-footprint

([300]) See Impact Assessment to: *Regulation (EU) No 517/2014 of the European Parliament and of the Council of 16 April 2014 on fluorinated greenhouse gases and repealing Regulation (EC) No 842/2006 Text with EEA relevance:* https://ec.europa.eu/clima/document/download/9013881e-8d5d-429e-9112-c908f127c833_en?filename=f-gases_impact_assessment_en.pdf

([301]) https://www.electronicspecifier.com/industries/alternative-energy/european-fluorinated-greenhouse-gas-emissions-cut-by-42

semiconductors in the EU while minimising where possible emissions, is likely to save emissions from F-gases at global scale.

While past efforts have reduced emissions by substituting longer-chain per-and polyfluoroalkyl substances (PFAS) with short-chain alternatives, further reductions necessitate entirely new compounds, presenting a complex challenge. Switching to alternative chemicals involves balancing global warming potential (GWP) and atmospheric persistence, often leading to trade-offs. For instance, while CHF_3 has a higher GWP than CF_4, CF_4 stays longer in the atmosphere.

Despite the urgency, transitioning away from harmful compounds will require time, with challenges varying across processes. Solutions for cleaning processes may emerge within 5–10 years, while alternatives for dry etching could take more than 15 years. Generally, implementation of non-PFAS alternatives is expected to take 15 to more than 20 years. This transition incurs substantial research and transition costs, underscoring the need for a long-term commitment to sustainability. Certain of these forever chemicals used in semiconductor manufacturing are included in the proposed ban on PFAS under the REACH regulation. ([302])

Scope 2 emissions (indirect emissions)

Electricity represents the largest share of energy consumption in semiconductor manufacturing and is the primary source of GHG emissions in chip production. The amount of electricity used varies significantly depending on factors such as chip type, manufacturing process complexity, and lithography technology. More advanced processes, such as extreme ultraviolet (EUV) lithography, consume substantially more energy. For instance, 5 nm logic manufacturing processes require roughly three times as much electricity as 32 nm processes. This illustrates that it is not possible to provide a general estimate of energy consumption per wafer without specifying the manufacturing process, technology type, and node. ([303])

Very broadly speaking estimates suggest that large, advanced wafer fabrication facilities can draw more than 100 MW of continuous power - comparable to the electricity demand of a small city. From a global perspective, total energy consumption in semiconductor manufacturing increased by approximately 125% between 2015 and 2023. This growth is driven not only by the increasing complexity of manufacturing processes and equipment but also by the substantial expansion of global production capacity and increased operation of abatement equipment. ([304])

There are two distinct methods for scope 2 accounting. A location-based method reflects the average emissions intensity of grids on which energy consumption occurs (using mostly grid-average emission factor data). ([305]) A market-based method reflects emissions from electricity that companies have purposefully chosen (or their lack of choice). ([306]) In the estimations below, both scope 2 accounting methods will be presented.

([302]) https://www.interface-eu.org/publications/chip-productions-ecological-footprint
([303]) https://www.interface-eu.org/publications/semiconductor-emission-explorer
([304]) https://www.interface-eu.org/publications/semiconductor-emission-explorer
([305]) Scope 2 Guidance.pdf
([306]) Scope 2 Guidance.pdf

4.1.2. Environmental impact assessment for BAU scenario

Reported total emissions from EU chip production in 2021 amounted to be between 10.67 Mio tCO2e and 13.67 Mio tCO2e. ([307]) Assuming, no major changes in total emissions by 2024, this matches our own calculations for scope 1 and 2 emissions in Europe. Assuming that Europe's current yearly manufacturing capacity of wafers is around 12.84 Mio, scope 1 emissions are estimated to reach between 821 760 ([308]) – 1 027 000 ([309]) tCO2e, with scope 2 (location-based) being around 4 173 000 ([290]) – 5 392 800 ([308]) tCO2e. Our analysis lacks the reporting on scope 3 emissions due to missing standardisation. However, as the average share of scope 3 emissions among the 20 largest chip manufacturers was 65% in 2021 ([310]), and assuming scope 3 emissions did not change significantly over the last 3 years, the total emissions from EU chip manufacturing in 2024 are indeed estimated to be between 10.67 Mio tCO2e and 13.67 Mio tCO2e. Using imec.netzero model ([311]), total scope 3 emissions are estimated to be around 3 466 800 tCO2e.

Estimated EU's total scope 1 and 2 emissions (location and market-based) were calculated based on scope 1 and 2 emissions reported for the Global Foundries (GF) fab in Dresden in 2023 assuming maximum yearly wafer capacity of 950 000. ([312]) Data from Global Foundries fab in Dresden were purposefully chosen to reflect as much as possible the European reality. Among available disclosures, only GlobalFoundries provided **both site-level emissions data and corresponding wafer capacity**, which enabled transparent calculation of emissions intensity and supports a defensible proxy for European fab operations.

Additionally, imec.netzero multi-parametric Life-Cycle Assessment model that calculates the environmental footprint for the fabrication of integrated circuits in a high-volume semiconductor fab was also used and the data achieved are consistent with our own calculations. ([313]) One of the major additional benefits of the imec.netzero model is the inclusion of scope 3 emissions.

To estimate total EU emissions for scope 1 and 2, first emissions per wafer were calculated for the **Global Foundries fab in Dresden.**

Maximum yearly wafer capacity /wpy	950 000 ([314])
Scope 1 emissions / tCO2e	60 831 ([315])
Scope 2 emissions (location-based) / tCO2e	308 337 ([316])

([307]) https://www.interface-eu.org/publications/chip-productions-ecological-footprint
([308])Own calculations
([309])Die Setup - imec.netzero; technologies: N28 (Logic Mobile SoC, 300 mm), Germany - average ; 10 mm die size X and die size Y: yield 85%; IPCC Tier 2C with combustion abatement model
([310]) https://www.interface-eu.org/publications/chip-productions-ecological-footprint
([311]) Die Setup - imec.netzero; technologies: N28 (Logic Mobile SoC, 300 mm), Germany - average ; 10 mm die size X and die size Y: yield 85%; IPCC Tier 2C with combustion abatement model
([312]) 2023 data are taken into account as from 1st January 2024, a cogeneration plant at the Dresden site came under the operational control of GF and the emissions from the plant are being reported as scope 1 emissions. Before 1st January 2024 they were categorised as scope 2 emissions.
([313]) Die Setup - imec.netzero; technologies: N28 (Logic Mobile SoC, 300 mm), Germany - average ; 10 mm die size X and die size Y: yield 85%; IPCC Tier 2C with combustion abatement model
([314]) Dresden: Facts, figures, data | GlobalFoundries
([315]) CDP_-GlobalFoundries-Inc.-09-10-2024-CORPORATE_public_version.pdf
([316]) CDP_-GlobalFoundries-Inc.-09-10-2024-CORPORATE_public_version.pdf

Scope 2 emissions (market-based) / tCO2e	273 995 ([317])
Scope 1 emissions / tCO2e/wafer	≈ 0.064
Scope 2(location-based) emissions / tCO2e/wafer	≈ 0.325
Scope 2 (market-based) emissions / tCO2e/wafer	≈ 0.288
Total current capacity /wpy	≈ 12.84 Mio
Estimated total scope 1 emissions / tCO2e	≈ 821 760
Estimated total current scope 2 (location-based) emissions / tCO2e	≈ 4 173 000
Estimated total current scope 2 (market-based) emissions / tCO2e	≈ 3 697 920

Data achieved from imec.netzero model for N28 (Logic Mobile SoC, 300 mm) are presented in the Table below. ([318])

Scope 1 emissions / tCO2e/wafer	0.08 ([317])
Estimated total scope 1 emissions / tCO2e	1 027 000
Scope 2 emissions / tCO2e/wafer	0.42 ([317])
Estimated total current scope 2 (location-based) emissions / tCO2e	5 392 800
Scope 3 emissions / tCO2e/wafer	0.27 ([317])
Estimated total current scope 3 emissions / tCO2e	3 466 800

However, because Europe accounts for only a small share of global semiconductor manufacturing capacity compared with its Asian counterparts, its associated emissions remain well below those of high-emitting sectors.

Water

A large semiconductor fabrication plant (fab) uses up to 38 million litres per day, equivalent to the daily water consumption of around 300,000 people in Germany. ([319]) Water is primarily used for ultrapure water (UPW) production, a complex process that involves multi-stage treatments, such as reverse osmosis and ultrafiltration, with water reuse and recycling being common on-site practices. ([320])

([317]) CDP_-GlobalFoundries-Inc.-09-10-2024-CORPORATE_public_version.pdf
([318]) Die Setup - imec.netzero; technologies: N28 (Logic Mobile SoC, 300 mm), Germany - average ; 10 mm die size X and die size Y: yield 85%; IPCC Tier 2C with combustion abatement model
([319]) Interface (2024). Chip Production's Ecological Footprint: Mapping Climate and Environmental Impact. https://www.interface-eu.org/publications/chip-productions-ecological-footprint
([320]) IMEC. (2022). *Sustainable Semiconductor Manufacturing: A Path Forward.* IMEC Research Report.

Semiconductor manufacturing in Europe reflects the global characteristics of the industry: it is among the most resource- and energy-intensive industrial activities per unit of value added. The deployment of advanced wafer fabrication processes in Europe would likely result in a substantial increase in emissions. However, European fabs benefit from a comparatively low-carbon electricity mix: the average grid emission intensity is roughly one-third that of major East Asian manufacturing regions. ([321]) Despite this advantage, electricity use remains the single largest contributor to lifecycle emissions, accounting for approximately 60–70% of total CO_2-equivalent emissions in front-end manufacturing. ([322])([323])([324])

Overall, semiconductor manufacturing is extremely water intensive. Current water withdrawal per wafer in Europe is estimated to be about 10.75 m^3 ([325]) (some reports give even higher values of 15 m^3 per 12-inch wafer ([326]), which accounts for around 138 Mio m^3 water used per year during semiconductor manufacturing, assuming 12.8 Mio wafer capacity in the EU.

Waste

Apart from GHG emissions and various volatile organic compounds that are released into the atmosphere, front-end manufacturing generates chemical waste, solid waste, wastewater, slurries and abrasives and packaging waste. In the last eight years, the amount of waste generated in the semiconductor industry has nearly doubled. ([327])

Regarding the environmental impact, it is important to differentiate between general or non-hazardous waste and hazardous waste. ([328]) For most semiconductor manufacturers, the ratio between hazardous and non-hazardous waste is 40%–60%. ([329]) Unused or spent chemicals, such as those that can be categorised as PFAS, often contain waste acids, waste solvents, waste copper sulphate, heavy metals, etc., which end up in either chemical waste or wastewater. ([330]) If not treated properly, they pose a high risk to environmental and human health. The same applies to waste slurries, which consist of solid and potentially abrasive and hazardous particles suspended in water from chemical mechanical polishing (CMP) processes. ([331])

Front-end manufacturers have put in place waste classification and separation, as well as safe treatment practices to comply with regulations and increase the share of recyclable waste. Within the last decade, most manufacturers have achieved high external recycling rates and very low rates of disposal to landfill. A low share of hazardous waste needs to be treated by specially authorised companies. On average, around 70% of all hazardous and non-hazardous

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([321]) International Energy Agency (IEA). (2023). *Energy Efficiency in Industry: Semiconductor Manufacturing Focus.* Paris: IEA.
([322]) European Commission, Joint Research Centre (JRC). (2025). *EU's strengths and weaknesses in the global semiconductor sector (JRC141323).* Luxembourg: Publications Office of the European Union.
([323]) McKinsey & Company. (2025). *Semiconductors have a big opportunity—but barriers to scale remain.* McKinsey Global Institute.
([324]) IMEC. (2022). *Sustainable Semiconductor Manufacturing: A Path Forward.* IMEC Research Report.
([325]) Calculations based on total water withdrawals by Global Foundries in 2023 (CDP_-GlobalFoundries-Inc.-09-10-2024-CORPORATE_public_version.pdf) assuming total wafer shipments of 2.2 Mio wpy
[326] Water-Europe-Socio-Economic-Study-1.pdf
([327]) Ian King (2022): Chipmakers' $52 Billion US Bonanza Imperils Environmental Gains. Bloomberg.
([328]) Waste | NXP Semiconductors
([329]) Interface (2024). Chip Production's Ecological Footprint: Mapping Climate and Environmental Impact. Chip Production's Ecological Footprint: Mapping Climate and Environmental Impact
([330]) Waste | NXP Semiconductors
([331]) Waste | NXP Semiconductors

wastes can be recycled for reuse in other industries. ([332]) It is much more difficult to recycle waste to be reused within the front-end manufacturing process itself. The share of preparation for reuse in a fab varies significantly and is mostly applied to chemical reuse from hazardous waste. A recent example is the invention of neon gas recycling technology, which can reduce emissions in the production and usage of neon gas, as well as in waste treatment. ([333]) Additionally, waste is burnt with recovery for energy; only 1%–5% of waste is sent to landfill. ([334])

4.1.3. Modelling for different scenarios

Developments expected under BAU to 2035

Energy consumption: Under BAU, the total energy demand of Europe's semiconductor industry increases substantially as announced fabs in Germany, France, Ireland, and Italy become operational. Despite continued grid decarbonisation and growing uptake of power purchase agreements (PPAs) and on-site renewables, absolute electricity use more than doubles by 2035. Energy intensity per wafer will most likely grow due to the transition to more advanced lithography equipment, growing overall complexity in manufacturing processes and increased use of abatement equipment.

Water use and waste treatment: Water stress becomes an increasing constraint on site selection, particularly in regions with limited freshwater availability such as Saxony and southern France. ([335]) Most new fabs incorporate water-recycling systems targeting 75–85 % reuse, yet total consumption still rises with industry expansion and growing complexity of manufacturing processes. ([336])([337]) Chemical-waste treatment and ultrapure-water systems continue to account for roughly 20–30 % of fab operating expenditure related to utilities. ([338])([339])

With the estimated 20.28 Mio wpy produced in Europe in 2035, the water withdrawal will reach 218 Mio m^3.

Land use and spatial footprint: Land requirements expand through new industrial parks and fab extensions, but EU planning and permitting rules constrain excessive sprawl. ([340]) Environmental impact assessments (EIAs) and biodiversity-offset obligations remain stringent,

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([332]) Interface (2024). Chip Production's Ecological Footprint: Mapping Climate and Environmental Impact. Chip Production's Ecological Footprint: Mapping Climate and Environmental Impact
([333]) https://www.gasworld.com/story/industrys-first-neon-gas-recycling-technology-announced-by-sk-hynix-temc/2136766.article/
([334]) Ibid Interface (2024). Chip Production's Ecological Footprint: Mapping Climate and Environmental Impact. Chip Production's Ecological Footprint: Mapping Climate and Environmental Impact
([335]) European Commission, Joint Research Centre (JRC). (2025). *EU's strengths and weaknesses in the global semiconductor sector (JRC141323).* Luxembourg: Publications Office of the European Union.
([336]) SEMI. (2023). *Sustainability in the Semiconductor Manufacturing Supply Chain.* SEMI Global Update.
([337]) McKinsey & Company. (2025). *Semiconductors have a big opportunity—but barriers to scale remain.* McKinsey Global Institute.
([338]) IMEC. (2022). *Sustainable Semiconductor Manufacturing: A Path Forward.* IMEC Research Report.
([339]) SEMI. (2023). *Sustainability in the Semiconductor Manufacturing Supply Chain.* SEMI Global Update.
([340]) European Court of Auditors. (2025). *Special Report 12/2025 – The EU's strategy for microchips: Reasonable progress in its implementation, but the Chips Act is very unlikely to be sufficient to reach the overly ambitious Digital Decade target.*

while approval timelines continue to be long due to the environmental sensitivity of large-scale semiconductor sites. ([341])

Emissions:

Under BAU, EU front-end manufacturing capacity grows, from 1.07 million wpm in 2023 to around 1.48 million wpm by 2030 and 1.56–1.82 million wpm by 2035, maintaining a stable 8–9% of global capacity share. Taking the average of this range, under BAU the EU's front-end manufacturing capacity in 2035 will reach 1.69 Mio wpm, which is 20.28 Mio wpy (as estimated in Annex 4, Section 1.2). Therefore, based on the scope 1 and 2 emissions reported for the Global Foundries (GF) fab in Dresden in 2023, and extrapolating to European wafer production capacity, the total Europe's scope 1 and 2 emissions from front-end manufacturing in 2035 can be estimated.

Estimated average capacity in 2035 / wpy	≈ 20.28 Mio
Estimated total scope 1 emissions in 2035 under BAU / tCO2e	≈ 1 297 920
Estimated total scope 2 (location-based) emissions in 2035 under BAU / tCO2e	≈ 6 591 000
Estimated total scope 2 (market-based) emissions in 2035 under BAU / tCO2e	≈ 5 840 640
Estimated total scope 1 emissions in 2035 under BAU using imec.netzero model ([342]) / tCO2e	1 622 400
Estimated total scope 2 emissions in 2035 under BAU using imec.netzero model ([343]) / tCO2e	8 517 600
Estimated total scope 3 emissions in 2035 under BAU using imec.netzero model ([344]) / tCO2e	5 475 600

Emissions from fluorinated gases (e.g. perfluorocarbons [PFCs], SF_6) decline slightly owing to substitution and abatement technologies, supported by international efforts under the Kyoto-Protocol gases framework. ([345]) Nevertheless, indirect emissions from electricity consumption dominate the sector's carbon balance until full grid decarbonisation is achieved. ([346])([347]) By

([341]) European Commission, Joint Research Centre (JRC). (2025). *EU's strengths and weaknesses in the global semiconductor sector (JRC141323).* Luxembourg: Publications Office of the European Union.
([342]) Die Setup - imec.netzero; technologies: N28 (Logic Mobile SoC, 300 mm), Germany - average ; 10 mm die size X and die size Y: yield 85%; IPCC Tier 2C with combustion abatement model
([343]) Die Setup - imec.netzero; technologies: N28 (Logic Mobile SoC, 300 mm), Germany - average ; 10 mm die size X and die size Y: yield 85%; IPCC Tier 2C with combustion abatement model
([344]) Die Setup - imec.netzero; technologies: N28 (Logic Mobile SoC, 300 mm), Germany - average ; 10 mm die size X and die size Y: yield 85%; IPCC Tier 2C with combustion abatement model
([345]) IMEC. (2022). *Sustainable Semiconductor Manufacturing: A Path Forward.* IMEC Research Report.
([346]) McKinsey (2025). *Semiconductors have a big opportunity—but barriers to scale remain.* McKinsey Global Institute.
([347]) International Energy Agency (IEA). (2023). *Energy Efficiency in Industry: Semiconductor Manufacturing Focus.* Paris: IEA.

2035, Europe's fab-related emissions intensity is expected to fall by roughly 20–25 %, but total emissions still rise in line with overall capacity growth. ([348])([349])

Rationale

Environmental performance improves gradually under BAU thanks to incremental technology gains, stricter EU environmental standards, and a cleaner electricity mix. ([350])([351]) European fabs benefit from ongoing grid decarbonisation, adoption of power purchase agreements (PPAs), and diffusion of energy- and water-efficiency technologies such as heat recovery and closed-loop recycling. ([352])([353])

However, structural factors such as high capital intensity, dependence on specialty chemicals, and the 24/7 operational nature of fabs limit the scope for deep decarbonisation without major technological or process breakthroughs. ([354])([355])([356])

Implications

Under BAU conditions, Europe's semiconductor expansion increases the industry's absolute environmental footprint despite moderate efficiency gains. ([357])([358]) SMEs in supply chain segments particularly in materials, chemicals, and component processing face higher compliance costs as environmental reporting and permitting become more stringent under EU legislation such as the Industrial Emissions Directive and CSRD, while large fabs are better positioned to absorb these through scale and dedicated compliance teams. ([359])([360]) Water and energy efficiency technologies, including closed-loop recycling, waste-heat recovery, and renewable PPAs, become standard features of new facilities by the early 2030s, ([361])([362]) but their diffusion across smaller suppliers remains uneven. In comparison to other manufacturing regions internationally, Europe has positioned itself as the frontier manufacturing hub when it comes to more sustainable solutions not only due to the availability of renewable energy but also due to its excellent research and development strengths in the supplier markets (equipment & chemicals) as well as in chip production.

([348]) European Commission, Joint Research Centre (JRC). (2025). *EU's strengths and weaknesses in the global semiconductor sector (JRC141323).* Luxembourg: Publications Office of the European Union.
([349]) McKinsey (2025). *Semiconductors have a big opportunity—but barriers to scale remain.* McKinsey Global Institute.
([350]) European Commission, Joint Research Centre (JRC). (2025). *EU's strengths and weaknesses in the global semiconductor sector (JRC141323).* Luxembourg: Publications Office of the European Union.
([351]) International Energy Agency (IEA). (2023). *Energy Efficiency in Industry: Semiconductor Manufacturing Focus.* Paris: IEA.
([352]) IMEC. (2022). *Sustainable Semiconductor Manufacturing: A Path Forward.* IMEC Research Report.
([353]) McKinsey (2025). *Semiconductors have a big opportunity—but barriers to scale remain.* McKinsey Global Institute.
([354]) IMEC. (2022). *Sustainable Semiconductor Manufacturing: A Path Forward.* IMEC Research Report.
([355]) McKinsey (2025). *Semiconductors have a big opportunity—but barriers to scale remain.* McKinsey Global Institute.
([356]) Boston Consulting Group (BCG). (2024). *Advanced packaging is reshaping the chip industry.* BCG Report.
([357]) European Commission, Joint Research Centre (JRC). (2025). *EU's strengths and weaknesses in the global semiconductor sector (JRC141323).* Luxembourg: Publications Office of the European Union.
([358]) McKinsey (2025). *Semiconductors have a big opportunity—but barriers to scale remain.* McKinsey Global Institute.
([359]) European Court of Auditors. (2025). *Special Report 12/2025 – The EU's strategy for microchips: Reasonable progress in its implementation, but the Chips Act is very unlikely to be sufficient to reach the overly ambitious Digital Decade target.*
([360]) Ebrahimi, A. (2024). *Groundbreaking chip sovereignty: Europe's strategic push in the semiconductor race.* Ifri Memos, Institut français des relations internationales (IFRI). ISBN 979-10-373-0874-0.
([361]) IMEC. (2022). *Sustainable Semiconductor Manufacturing: A Path Forward.* IMEC Research Report.
([362]) SEMI. (2023). *Sustainability in the Semiconductor Manufacturing Supply Chain.* SEMI Global Update.

4.1.4. Developments expected under Policy Option 1

It was assumed that, under Policy Option 1 (PO1), more favourable policy frameworks would lead to a growth rate of 4% from 2030 onwards. This would lead to the capacity of 20.3 Mio wafer per year, which in turn would account to between 1.3 – 1.6 MtCO2 in scope 1 emissions and 6.6 – 8.526 MtCO2 in scope 2 emissions (location-based). Estimated EU's total scope 1 and 2 emissions (location-based) of PO1 were calculated based on scope 1 and 2 emissions reported for the Global Foundries (GF) fab in Dresden in 2023 and imec.netzero model. ([363])([364])

4.1.5. Developments expected under Policy Option 2

Under Policy Option 2, two scenarios were envisaged:

1. Scenario 1 - in which new investments broadly replicate the current European wafer mix and technology profile;
2. Scenario 2 - in which part of the investment is redirected towards a cutting-edge logic fab, with the remainder following the current European mix.

The estimation of additional scope 1 and 2 emissions resulting from future investments for scenario 1 was based on emissions from Global Foundries fab in Dresden in 2023 and taking into consideration the expansion of the current European wafer mix as presented in Annex 4, section 1.2.

Scenario 1:

Total estimated capacity in 2035 in scenario 1/wpy	≈ 22.0 Mio
Estimated total scope 1 emissions in 2035 in scenario 1/ tCO2e	≈ 1 409 859
Estimated total scope 2 (location-based) emissions in 2035 in scenario 1 / tCO2e	≈ 7 146 221
Estimated total scope 2 (market-based) emissions in 2035 in scenario 1 / tCO2e	≈ 6 350 288
Total estimated water withdrawal per year in 2035 in scenario 1/ Mio m^3	≈ 236.5
Estimated total scope 1 emissions in 2035 in scenario 1 using imec.netzero model ([365]) / tCO2e	1 761 426
Estimated total scope 2 emissions in 2035 in scenario 1 using imec.netzero model ([366]) / tCO2e	9 247 486

([363]) CDP_-GlobalFoundries-Inc.-09-10-2024-CORPORATE_public_version.pdf
([364]) Die Setup - imec.netzero; technologies: N28 (Logic Mobile SoC, 300 mm), Germany - average ; 10 mm die size X and die size Y: yield 85%; IPCC Tier 2C with combustion abatement model
([365]) Die Setup - imec.netzero; technologies: N28 (Logic Mobile SoC, 300 mm), Germany - average ; 10 mm die size X and die size Y: yield 85%; IPCC Tier 2C with combustion abatement model
([366]) Die Setup - imec.netzero; technologies: N28 (Logic Mobile SoC, 300 mm), Germany - average ; 10 mm die size X and die size Y: yield 85%; IPCC Tier 2C with combustion abatement model

Estimated total scope 3 emissions in 2035 in scenario 1 using imec.netzero model ([367]) / tCO2e	5 944 813

In scenario 1, the total water withdrawal would increase to 236.5 Mio m^3 per year, which is around 8.5% increase in water withdrawal compared to the baseline scenario.

The estimation of additional scope 1 and 2 emissions resulting from future investments for scenario 2 was based on emissions from Global Foundries fab in Dresden in 2023 and as well as scope 1 and 2 emissions of TSMC fabs Japan, also taking into consideration the expansion of mainstream manufacturing capacities and **assuming emergence of leading-edge manufacturing** as presented in Annex 4, Section 1.1 and 1.2.

Scenario 2:

Total estimated capacity in 2035 of mainstream manufacturing in scenario 2 / wpy	≈ 20.4 Mio
Estimated total scope 1 emissions in 2035 of mainstream manufacturing in scenario 2/ tCO2e per year	≈ 1 303 394
Estimated total scope 2 (location-based) emissions in 2035 of mainstream manufacturing in scenario 2/ tCO2e per year	≈ 6 606 576
Estimated total scope 2 (market-based) emissions in 2035 of mainstream manufacturing in scenario 2/ tCO2e per year	≈ 5 870 747
Total estimated water withdrawal per year in 2035 of mainstream manufacturing in scenario 2/ Mio m^3 per year	≈ 222.5
Estimated total scope 1 in 2035 of mainstream manufacturing in scenario 2 using imec.netzero model ([368]) / tCO2e	1 628 412
Estimated total scope 2 emissions in 2035 of mainstream manufacturing in scenario 2 using imec.netzero model ([369]) / tCO2e	8 549 164
Estimated total scope 3 emissions in 2035 of mainstream manufacturing in scenario 2 using imec.netzero model ([370]) / tCO2e	5 495 891

([367]) Die Setup - imec.netzero; technologies: N28 (Logic Mobile SoC, 300 mm), Germany - average ; 10 mm die size X and die size Y: yield 85%; IPCC Tier 2C with combustion abatement model
([368]) Die Setup - imec.netzero; technologies: N28 (Logic Mobile SoC, 300 mm), Germany - average ; 10 mm die size X and die size Y: yield 85%; IPCC Tier 2C with combustion abatement model
([369]) Die Setup - imec.netzero; technologies: N28 (Logic Mobile SoC, 300 mm), Germany - average ; 10 mm die size X and die size Y: yield 85%; IPCC Tier 2C with combustion abatement model
([370]) Die Setup - imec.netzero; technologies: N28 (Logic Mobile SoC, 300 mm), Germany - average ; 10 mm die size X and die size Y: yield 85%; IPCC Tier 2C with combustion abatement model

The data to calculate the environmental impact of one leading-edge fab in Europe were based on the emissions reported by TSMC in 2024 and taking into consideration that TSMC's wafer manufacturing capacity in 2024 was 12.9 Mio. ([371]) Using TSMC as a proxy for leading-edge fab emissions in Europe can be justified on technical and operational grounds. Firstly, leading-edge fabs are dominated by process node physics and equipment sets (EUV lithography, advanced deposition/etch, ultra-pure water systems). TSMC operates the same class of tools and nodes expected in Europe, making its per-wafer and per-area intensities a defensible starting point. Secondly, TSMC represents a global efficiency frontier for high-volume advanced manufacturing. Using a best-practice operator avoids underestimating process-intrinsic loads and provides a conservative, performance-anchored baseline for scope 1 (process gases) and scope 2 (electricity demand before grid adjustment). While TSMC's portfolio and scale in Taiwan will differ from a new proposed European site, scale efficiencies mainly affect overhead energy (HVAC, utilities) rather than tool energy per wafer. Additionally, imec.netzero multi-parametric Life-Cycle Assessment model that calculates the environmental footprint for the fabrication of integrated circuits in a high-volume semiconductor fab was also used and the data achieved are consistent with our own calculations, confirming their credibility and relevance. ([372])

Maximum yearly wafer capacity /wpy	12.9 Mio
Scope 1 emissions / tCO2e per year	1 826 000
Scope 2 emissions (location-based) / tCO2e per year	12 674 921
Scope 2 emissions (market-based) / tCO2e per year	10 957 397
Scope 1 emissions / tCO2e/wafer	≈ 0.141550
Scope 2 (location-based) emissions / tCO2e/wafer	≈ 0.9824806
Scope 2 (market-based) emissions / tCO2e/wafer	≈ 0.8493798
Energy consumption / GWh/wafer	≈ 0.00213
Water withdrawal / m^3/wafer	≈ 9.98
Scope 1 emissions from imec.netzero model / tCO2e/wafer	0.15 ([373])
Scope 2 emissions from imec.netzero model / tCO2e/wafer	0.92 ([374])
Scope 3 emissions from imec.netzero model / tCO2e/wafer	0.48 ([375])

([371]) esg.tsmc.com/en-US/file/public/2024-TSMC-Sustainability-Report-e.pdf
([372]) Die Setup - imec.netzero; technologies: N2 (Logic Mobile SoC, 300 mm), Germany -average ; 10 mm die size X and die size Y: yield 85%; IPCC Tier 2C with combustion abatement model
([373]) Die Setup - imec.netzero; technologies: N2 (Logic Mobile SoC, 300 mm), Germany -average ; 10 mm die size X and die size Y: yield 85%; IPCC Tier 2C with combustion abatement model
([374]) Die Setup - imec.netzero; technologies: N2 (Logic Mobile SoC, 300 mm), Germany -average ; 10 mm die size X and die size Y: yield 85%; IPCC Tier 2C with combustion abatement model
([375]) Die Setup - imec.netzero; technologies: N2 (Logic Mobile SoC, 300 mm), Germany -average ; 10 mm die size X and die size Y: yield 85%; IPCC Tier 2C with combustion abatement model

As modelled in Annex 4, section 1.2, the estimated capacity of a leading-edge fab could reach 25 000 wpm so 300 000 wpy in 2035. Taking this into consideration, total scope 1 and 2 emissions could be calculated based on the TSMC data. ([376])

Total estimated capacity in 2035 of advanced manufacturing in scenario 2 / wpy	≈ 300 000
Estimated scope 1 emissions of one leading-edge fab in scenario 2/ tCO2e per year	≈ 42 465
Estimated scope 2 (location-based) of one leading-edge fab in scenario 2 / tCO2e per year	≈ 294 766
Estimated scope 2 (market-based) of one leading-edge fab in scenario 2 / tCO2e per year	≈ 254 814
Estimated energy consumption of a one leading-edge / GWh per year	≈ 639
Estimated water withdrawal of one leading-edge fab in scenario 2 / Mio m^3 per year	≈ 2.994
Estimated total scope 1 in 2035 one leading-edge fab in scenario 2 using imec.netzero model ([377]) / tCO2e	45 000
Estimated total scope 2 emissions in 2035 of one leading-edge fab in scenario 2 using imec.netzero model ([378]) / tCO2e	276 000
Estimated total scope 3 emissions in 2035 of one leading-edge fab in scenario 2 using imec.netzero model ([379]) / tCO2e	144 000

It should be noted that in Taiwan, the power system remains heavily dependent on fossil fuels—with more than 80 % of generation from gas and coal and an average carbon intensity above ~0.50 tCO_2 per MWh (≈ 500 gCO_2/kWh) in 2024/25 – reflecting limited low-carbon penetration in its grid mix. ([380]) In contrast, the Europe electricity system, particularly at the EU level, benefits from a far higher share of renewables and nuclear generation combined with aggressive decarbonization policies. As a result, the average carbon intensity of electricity generation in the EU in 2024 was around 0.21–0.24 tCO_2/kWh (≈ 210–240 gCO_2/kWh), less than half the global average and substantially below typical Taiwanese levels. ([381]) This structural difference means that, for identical electricity use, scope 2 emissions (location-based) calculated with European grid factors are often **~40% or more lower** than when Taiwan's grid mix is applied,

([376]) esg.tsmc.com/en-US/file/public/2024-TSMC-Sustainability-Report-e.pdf
([377]) Die Setup - imec.netzero; technologies: N2 (Logic Mobile SoC, 300 mm), Germany -average ; 10 mm die size X and die size Y: yield 85%; IPCC Tier 2C with combustion abatement model
([378]) Die Setup - imec.netzero; technologies: N2 (Logic Mobile SoC, 300 mm), Germany -average ; 10 mm die size X and die size Y: yield 85%; IPCC Tier 2C with combustion abatement model
([379]) Die Setup - imec.netzero; technologies: N2 (Logic Mobile SoC, 300 mm), Germany -average ; 10 mm die size X and die size Y: yield 85%; IPCC Tier 2C with combustion abatement model
([380]) Republic of China (Taiwan) Electricity Generation Mix 2025 | Low-Carbon Power Data
([381]) Global Electricity Review 2025 | Ember

a gap driven by Europe's greater penetration of low-carbon energy sources and ongoing decarbonization of its power sector.

Additionally, it is estimated that **emissions per wafer are expected to increase due to more complex manufacturing processes**. The analysis results indicate an average annual increase of 5.79% in emissions per wafer since 2013. ([382]) Assuming that the above analysis was conducted for the year 2025, and accounting for an average annual increase of 5.79% in emissions per wafer, the revised calculations are presented below:

Estimated scope 1 emissions in 2035 for a leading-edge fab in scenario 2 assuming 5.79% annual increase / tCO2e	≈ 74 555
Estimated scope 2 (location-based) of a leading-edge fab in scenario 2 assuming 5.79% annual increase / tCO2e	≈ 517 515
Estimated scope 2 (location-based) of a leading-edge fab in scenario 2 assuming 5.79% annual increase **adjusted for European electricity mix** / tCO2e	≈ 310 509
Estimated scope 2 (market-based) of a leading-edge fab in scenario 2 assuming 5.79% annual increase / tCO2e	≈ 447 372
Estimated total scope 1 emissions in 2035 of one leading-edge fab in scenario 2 using imec.netzero model ([383]) assuming 5.79% annual increase / tCO2e	79 005
Estimated total scope 2 emissions in 2035 of one leading-edge fab in scenario 2 using imec.netzero model ([384]) assuming 5.79% annual increase / tCO2e	484 568
Estimated scope 2 of a leading-edge fab in scenario 2 assuming 5.79% annual increase **adjusted for European electricity mix** using imec.netzero model ([385]) / tCO2e	290 740
Estimated total scope 3 emissions in 2035 of one leading-edge fab in scenario 2 using imec.netzero model ([386]) assuming 5.79% annual increase / tCO2e	252 818

([382]) Interface (2024). Chip Production's Ecological Footprint: Mapping Climate and Environmental Impact.Chip Production's Ecological Footprint: Mapping Climate and Environmental Impact
([383]) Die Setup - imec.netzero; technologies: N2 (Logic Mobile SoC, 300 mm), Germany -average ; 10 mm die size X and die size Y: yield 85%; IPCC Tier 2C with combustion abatement model
([384]) Die Setup - imec.netzero; technologies: N2 (Logic Mobile SoC, 300 mm), Germany -average ; 10 mm die size X and die size Y: yield 85%; IPCC Tier 2C with combustion abatement model
([385]) Die Setup - imec.netzero; technologies: N2 (Logic Mobile SoC, 300 mm), Germany -average ; 10 mm die size X and die size Y: yield 85%; IPCC Tier 2C with combustion abatement model
([386]) Die Setup - imec.netzero; technologies: N2 (Logic Mobile SoC, 300 mm), Germany -average ; 10 mm die size X and die size Y: yield 85%; IPCC Tier 2C with combustion abatement model

	Total scope 1 emissions in 2035 under Scenario 2 / tCO2e	Total scope 2 emissions (location-based) in 2035 under Scenario 2 / tCO2e	Total scope 3 emissions in 2035 under Scenario 2 / tCO2e
Mainstream nodes	1 303 394 - 1 628 412	6 606 576 - 8 549 164	5 495 891
Advanced nodes	74 555 – 79 005	290 740 – 310 509	252 818
Total	1 377 949 – 1 707 417	6 918 085 – 8 839 904	5 748 709

The estimated water consumption in scenario 2 under PO2 is around 222.3 Mio m^3 per year. This estimation is on the lower end as it based on water consumption of a TSMC fab in Taiwan, where there is a high water scarcity and therefore a stronger emphasis on water reuse and recycling (80% in Taiwan), while fabs in Europe typically have lower recycling rates (10%–14%). ([387]) This suggests that water consumption in Europe will be higher however the adoption of advanced water management technologies, including recycling and advanced treatment, can improve competitiveness, circularity and water efficiency in semiconductor production.

Furthermore, if scenario 2 of Policy Option 2 would take place, the increase in the use of materials would also happen. Leading-edge chips – especially those less than 10 nm – and advanced packaging (AP) require increasingly complex manufacturing methods, which increases the demand for the materials that enable these processes and create the finished products. As semiconductor technology progresses to use smaller nodes, the number of mask layers – used as part of the process that defines and fills conductive channels in the chip – for producing a single wafer increases disproportionally. For example, while a 65 nm process node wafer may require about 40 mask layers to complete, a leading-edge 5- or 3-nm process node requires up to 110 mask layers. ([388])

Beyond node size, AP is also increasing material consumption. Many AP technologies use interposers or base dies to connect multiple chips, require carrier wafers as part of the manufacturing process, or include an increasing number of interconnects (through-silicon via, for example). All these incremental process steps require more materials than mature technologies do.

The shift to using more mask layers and consuming additional materials as part of AP processes could increase Europe's total material consumption by as much as 65% and many of these materials may need to come from international markets. ([389])

Figure 21. Projected emissions under difference scenarios. *Source: prepared by the authors.*

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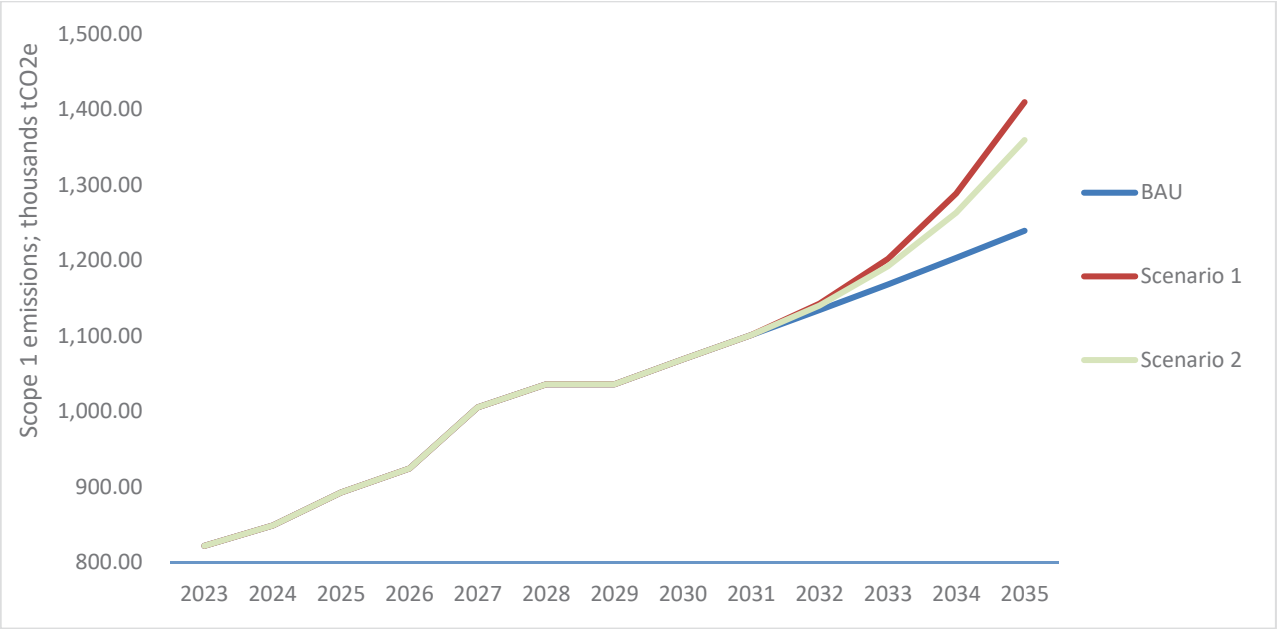
[387] Interface (2024). Chip Production's Ecological Footprint: Mapping Climate and Environmental Impact. Chip Production's Ecological Footprint: Mapping Climate and Environmental Impact

[388] Semiconductors have a big opportunity—but barriers to scale remain | McKinsey

[389] Semiconductors have a big opportunity—but barriers to scale remain | McKinsey



4.1.6. Costs of environmental impacts

From 2015 to 2025 the EU ETS carbon prices have been fluctuating a lot, ranging from very low prices, mostly below €10 / tCO_2 between 2015-2017, to €60–90 between 2022 -2023, before easing somewhat in 2024 – 2025 (€60 – €90 / tCO_2). Looking ahead, most outlooks point to a structurally tighter market with increasing scarcity of allowances, declining free allocation, and stricter caps, implying a renewed upward trend over the 2030s, with many analyst scenarios placing average EU ETS prices by 2035 well above today's levels - often in the range of roughly €190 – 300 per tonne of CO_2, depending on policy ambition, economic conditions, and technological progress. ([390])

Therefore, taking into consideration aggregated scope 1 and 2 emissions (location-based), environmental costs for each policy option in 2035 could be predicated in the ranges as follows:

- Baseline scenario BAU = €1.459 – €2.256 bln
- Policy Option 1 = €1.531 – €2.368 bln
- Policy Option 2, scenario 1 = €1.659 – €2.566 bln
- Policy Option 2, scenario 2 = €1.621 – €2.507 bln

The other possibility is to use the True Price method. This method developed the principles and methodology to monetise a wide set of social and environmental costs. ([391]) For environmental impacts, monetisation factor of €0.163 /kgCO2e was used describing restoration cost which expresses the abatement cost for achieving the policy targets of reducing GHG emissions to meet the 2-degree target as set in the Paris Agreement. ([348]) Using this factor, restoration cost for different policy options in 2035 can be estimated:

- Baseline scenario BAU = €1.226 bln

([390]) EU ETS Market Outlook 1H 2024: Prices Valley Before Rally | BloombergNEF
([391]) MONETISATION FACTORS FOR TRUE PRICING - True Price

- Policy Option 1 = €1.286 bln
- Policy Option 2, scenario 1 = €1.394 bln
- Policy Option 2, scenario 2 = €1.385 bln

5. COMPARATIVE ANALYSIS OF INVESTMENT, CAPACITY AND EMPLOYMENT OUTCOMES RELATED TO STRATEGIC PROJECTS

Modelling approach and baseline assumptions

The modelling relies on an empirical bottom-up calibration using first-of-a-kind (FOAK) semiconductor manufacturing projects supported to date in the EU. These projects constitute the only observable set of investments for which reasonably consistent information is available on:

- total investment volumes (public and private),
- planned wafer fabrication capacity, and
- announced direct employment at steady state.

The reference sample therefore reflects revealed investment behaviour under EU and Member State support schemes, rather than hypothetical or benchmarked fab configurations. This approach is consistent with the Better Regulation principle of grounding quantitative analysis in observed evidence where available, while acknowledging that the sample remains limited in size and heterogeneous in technological scope.

To ensure comparability across projects of different scale and technology profiles, the available FOAK data were normalised into intensity ratios, expressed as:

- wafer capacity per EUR billion of total investment; and
- direct employment per EUR billion of total investment.

Using the consolidated FOAK figures provided:

- total investment: EUR 31.23 billion;
- total planned new jobs: approximately 5,700; and
- total planned new wafer capacity: approximately 2.08 million wafers per year (around 173,000 wafers per month).

From these figures, the model derives average investment intensities that serve as proportional scaling parameters. These parameters implicitly capture the current European technology mix, capital intensity, and labour productivity embedded in recent supported projects.

The derived intensity ratios are then applied proportionally to the assumed EUR 40 billion investment envelope associated with strategic semiconductor projects, comprising public support and crowd-in private investment. The model assumes that:

- the full envelope translates into realised manufacturing investment;
- investment efficiency, in terms of capacity and employment per euro invested, remains constant relative to the FOAK reference sample; and
- no major structural break occurs in technology choice, production scale, or automation intensity relative to recent projects.

Under these assumptions, additional wafer capacity and employment are estimated by scaling up the FOAK-based ratios to the larger investment envelope. This proportional approach ensures internal consistency between observed projects and forward-looking estimates, while deliberately avoiding optimistic assumptions about learning effects or step-changes in productivity.

The modelling approach is intentionally conservative and subject to several limitations:

- FOAK projects may not yet reflect steady-state performance, as ramp-up periods and learning effects are ongoing.
- Publicly announced employment and capacity figures may change as projects progress.
- The sample does not include a fully operational leading-edge logic fab in Europe, limiting direct observability for advanced-node scenarios.

The modelling of Strategic Projects impacts relies on a total investment envelope of **EUR 40 billion**, comprising **EUR 15 billion in public support** (Competitiveness Fund, State aid, including Member State contributions) and **EUR 25 billion in private investment**. This envelope is assumed to be fully allocated to new manufacturing capacity and associated on-site activities.

Two scenarios are assessed:

- **scenario 1**, in which new investments broadly replicate the current European wafer mix and technology profile (i.e. mostly on mainstream chips); and
- **scenario 2**, in which part of the investment is redirected towards a cutting-edge logic fab, with the remainder following the current European mix.

Pessimistic scenario: continuation of the current European wafer mix

The pessimistic scenario assumes that new investments follow the **existing structure of semiconductor manufacturing in Europe**, characterised by a dominance of mature nodes and specialty technologies. The allocation of funding across technology segments is derived from **first-of-a-kind (FOAK) investments observed to date**, and the same proportional distribution is applied to the new EUR 40 billion envelope.

This scenario therefore reflects a continuation of current strengths, rather than a structural shift towards advanced logic manufacturing.

Employment and capacity impacts

Under this scenario, the model estimates:

- **Total new jobs**: **7,301**
- **Total new wafer capacity**: **2,660,263 wafers per year**, equivalent to
- **221,689 wafers per month**

Indirect employment

The evidence from the Intel Magdeburg case and the wider literature suggests that **no single indirect employment multiplier is universally appropriate** for semiconductor investments. Instead, the choice depends on the **purpose of the modelling** and the **degree of conservatism required**. **High-end estimates, such as the SIA multiplier of 6.7**, ([392]) reflect the full ecosystem effects observed in the US, where the multiplier captures a mature and highly localised semiconductor ecosystem, including upstream suppliers, specialised services, and downstream activities. There, semiconductor supply chains are deeper, labour mobility is higher, and a large share of upstream and downstream activities is domestic. Applying such a multiplier mechanically in an EU context risk **overestimating indirect and induced employment**, particularly in regions with tight labour markets and internationally fragmented

[392] The US semiconductor industry workforce and how federal incentives will increase domestic jobs – SIA, Oxford Economics - https://www.semiconductors.org/chipping-in-sia-jobs-report/

value chains. As such, the SIA figure is best used as an **upper-bound reference or sensitivity case**, rather than a central assumption.

For a **core or central modelling assumption** under the EU Chips Act, a **more conservative multiplier** is warranted. **Benchmarks such as the UNIDO ([393]) manufacturing multiplier (around 2.2 additional jobs per direct job)** provide a lower bound that is consistent with open economies and globalised supply chains, where a significant share of indirect effects is captured outside the host region through imports and international value chains, although not specific for the semiconductor industry. A pragmatic approach is therefore to use UNIDO multiplier as a proxy for a lower bound of potential indirect and induced jobs per direct job, reflecting partial but not full localisation of spillovers.

Therefore, under the pessimistic scenario, the level of indirect jobs created is assumed to be:

- Lower end (UNIDO multiplier): 7,301*2.2 = 16,061
- Upper end (downwards adjusted SIA multiplier): 7,301*5 = 36,503

These two benchmarks delimit a plausible range for indirect employment effects in the EU context.

Revenue impacts

To estimate revenues, the model applies a proportional approach based on the current relationship between **EU wafer capacity** and **device-level revenue**. Using an estimated total EU capacity of **1.07 million wafers per month** and reported EU semiconductor device revenue of **EUR 50.5 billion**, an average revenue per wafer is derived and applied to the incremental capacity.

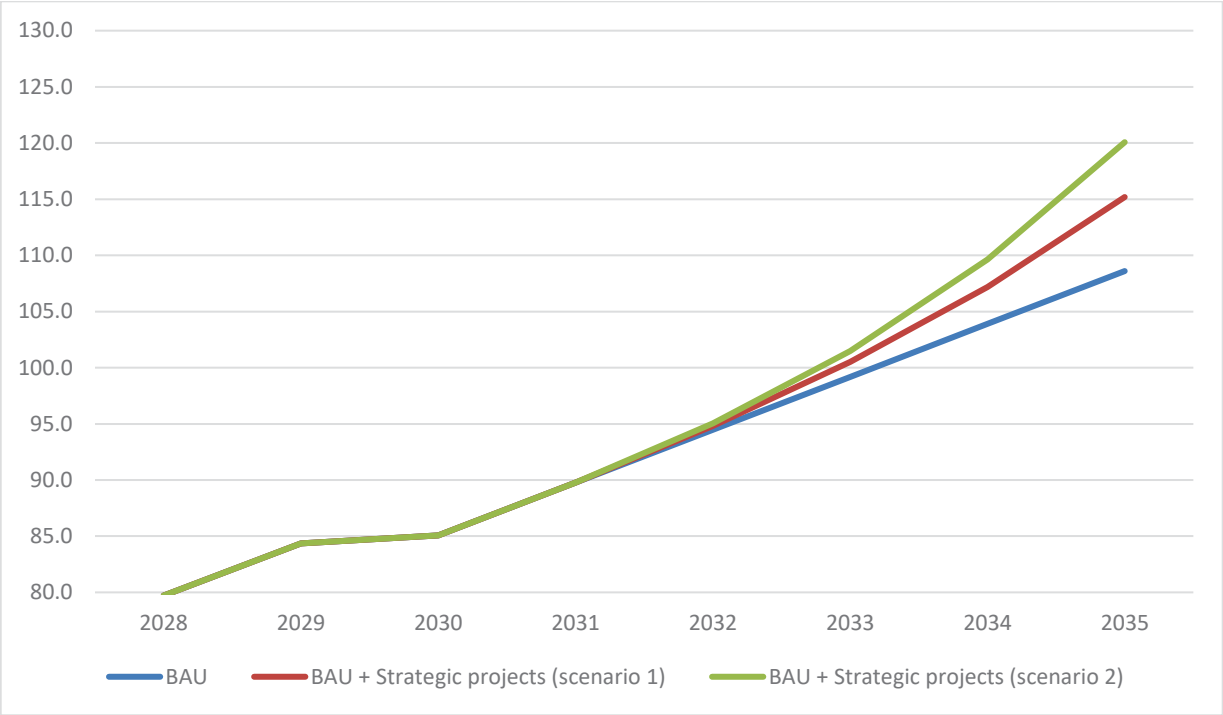
On this basis, the pessimistic scenario yields estimated additional annual revenue of approximately:

- **EUR 6.6 billion**

This outcome reflects the relatively low average selling prices associated with mature-node production, even at substantial volumes.

Figure 22. Projected revenues due to strategic projects. *Source: prepared by the authors.*

[393] The multiplier effect of industrial jobs – United Nation Industrial Development Organisation (UNIDO)



Optimistic scenario: assuming emergence of leading-edge manufacturing

The second scenario assumes a **more strategic allocation of investment**, in which:

- **EUR 25 billion** (indicative cost of a leading-edge fab) is dedicated to the construction of a **cutting-edge logic facility**, and
- the remaining **EUR 15 billion** is invested in line with the current European wafer mix, using the same assumptions as in the pessimistic scenario.

According to the Joint Research Centre, drawing on BCG analysis ([394]), a state-of-the-art semiconductor fab of standard capacity requires roughly USD 20 billion for advanced logic or memory production, including land, buildings and equipment. Another relevant reference is the Rapidus project in Japan, which targets 2-nanometre production and is reported to involve total investment of around USD 36 billion (approximately EUR 30 billion) ([395]), covering construction, equipment, and extensive process development. That figure reflects significant upfront R&D expenditure, notably through Rapidus' strategic collaboration via NanoIC pilot line hosted by imec ([396]). Given Europe's existing access to advanced research and pilot-line infrastructure through imec and related ecosystems, a lower all-in cost of EUR 25 billion for a comparable European fab is considered a reasonable assumption.

This scenario reflects a deliberate policy choice to use public support to **alter the technological composition** of EU semiconductor manufacturing, rather than only expanding existing segments.

Leading-edge fab assumptions:

([394]) Bonnet, P., Ciani, A., Molnar, J., & Nardo, M. (2025). *EU's strengths and weaknesses in the global semiconductor sector* (EUR 40253 EN). Luxembourg: Publications Office of the European Union. https://doi.org/10.2760/6302476
([395]) https://www.electronicsweekly.com/news/business/rapidus-picks-hokkaido-for-36bn-2nm-fab-2023-02/
([396]) https://www.imec-int.com/en/press/rapidus-japans-newly-founded-chip-manufacturer-joins-imecs-core-partner-program

The leading-edge component is modelled using conservative assumptions drawn from recent greenfield announcements:

- **Direct employment**: **2,000 jobs**, based on announced figures for comparable projects in the EU (e.g. ESMC).
- **Capacity**: **25,000 wafers per month**, consistent with public announcements for new advanced fabs (e.g. Rapidus[397]).
- **Average wafer revenue**: **EUR 30,000 per wafer**, reflecting industry estimates for advanced-node foundry pricing (e.g. TSMC[398])

These assumptions are indicative and reflect current industry benchmarks rather than firm contractual prices.

Combined impacts (leading-edge plus mature mix)

When combining the leading-edge investment with the remaining EUR 15 billion allocated to the current mix, the model estimates:

- **Total new direct jobs**: **4,738**
- **Total new indirect jobs: 10,423 – 23,690**
- **Total new wafer capacity**: **108,133 wafers per month**
- **Total additional annual revenue**: **EUR 11.5 billion**

Although total employment is lower than in the first scenario, this reflects the **higher capital intensity and automation** of leading-edge manufacturing rather than weaker economic performance.

Fiscal returns

We estimate the fiscal revenues generated once the new capacity is operational. Fiscal returns depend on the **additional value added** generated by ongoing production. To avoid overstating fiscal impacts by applying tax rates to turnover, the analysis converts additional semiconductor revenues into **additional gross value added (GVA)** using an empirically grounded value-added share.

Using OECD STAN data for EU Member States (ISIC Rev.4 **C26: manufacture of computer, electronic and optical products**) over 2020–2023, **the ratio of Value added to Output averages 34%.** This provides a transparent and robust benchmark for converting additional device revenues into additional value added. Accordingly, additional operational value added is estimated as:

Additional GVA = 0.34 × additional annual device revenue

This step ensures consistency with national accounts concepts and avoids double counting, as only the domestically generated component of revenue is treated as the relevant economic base for fiscal analysis.

([397])https://www.digitimes.com/news/a20250718PD228/rapidus-production-2nm-2027-chips.html#:~:text=Toward%20a%20commercial%20offering,Mayor%20Ryuichi%20Yokota%20of%20Chitose.
([398]) https://bits-chips.com/article/tsmc-to-raise-advanced-process-prices-by-up-to-10-percent/?utm

Based on the data provided in JRC (2025) ([399]) and OECD Tax Revenue Database ([400]) we know that an average share of value added captured as fiscal revenue is between 16% - 17% (assume 16.5% as a central point). This means that an annual fiscal return of:

- In pessimistic case: annual direct tax revenue would be around EUR 380 million;
- In optimistic case: annual direct tax revenue would be around EUR 662 million.

6. INNOVATION-ORIENTED PUBLIC PROCUREMENT AND FIRM INNOVATION OUTCOMES: EVIDENCE FROM THE LITERATURE

A growing empirical literature shows that public procurement can function as an effective **demand-side innovation instrument**, particularly when public buyers act as technologically sophisticated lead customers and require first-of-a-kind or non-off-the-shelf solutions. In such contexts, procurement influences firm behaviour not primarily through financial transfers, but by exposing suppliers to advanced technical requirements, intensive buyer–supplier interaction, and strong signalling effects towards downstream markets.

Evidence from procurement by large research infrastructures illustrates this mechanism clearly. Firm-level econometric analysis of CERN procurement shows that suppliers awarded CERN contracts experience a statistically significant increase in their likelihood of becoming innovators, with estimated effects in the order of around **10–20 percentage points** relative to otherwise comparable firms. The underlying channel operates through capability upgrading and learning-by-doing induced by demanding specifications, co-development processes, and reputational benefits associated with supplying a globally recognised scientific buyer. These effects are particularly salient for firms close to an innovation threshold, suggesting that innovation-oriented procurement can help firms cross barriers related to certification, technical validation, and market credibility ([401]).

Complementary large-sample evidence confirms that public procurement is associated with measurable innovation outcomes at firm level. Using Flash Eurobarometer data covering **28 EU Member States, Switzerland, and the US**, and a sample of **6,719 innovative firms** observed between **2011 and 2014**, econometric analysis combining cross-sectional regression with propensity score matching finds that participation in public procurement significantly increases the probability of innovation. Specifically, procurement participation raises the likelihood of introducing **product innovation by 10.6 percentage points in goods and 12.4 percentage points in services**, while supply-side R&D policy measures show no statistically significant effect on product innovation in either sector. For **process innovation**, procurement increases adoption probability by **6.3 percentage points**, while public R&D support raises the likelihood of process innovation by **7.2 percentage points**, indicating a degree of complementarity between demand-side and supply-side instruments for production upgrading ([402]).

([399]) Bonnet, P., Ciani, A., Molnar, J., & Nardo, M. (2025). *EU's strengths and weaknesses in the global semiconductor sector* (EUR 40253 EN). Luxembourg: Publications Office of the European Union. https://doi.org/10.2760/6302476

([400]) *OECD Tax Revenue Statistics: Comparative Tables and Tax Revenue Database (Edition 2024).* Paris: OECD Publishing. Available at https://stats.oecd.org/Index.aspx?DataSetCode=REV

([401]) Andrea Bastianin, Paolo Castelnovo, Lorenzo Zirulia, Overcoming the innovation threshold through innovative public procurement: evidence from CERN, *Industrial and Corporate Change*, Volume 34, Issue 5, October 2025, Pages 871–900, https://doi.org/10.1093/icc/dtaf004

([402]) Dragana Radicic, Effectiveness of public procurement of innovation versus supply-side innovation measures in manufacturing and service sectors, *Science and Public Policy*, Volume 46, Issue 5, October 2019, Pages 732–746, https://doi.org/10.1093/scipol/scz026

Beyond innovation outcomes, recent evidence also highlights broader economic effects of public procurement that are relevant for high-capital-intensity sectors. Budrys (2025) ([403]), using a novel dataset linking US federal procurement data with firm financials, stock market information, analyst forecasts, and credit default swaps, identifies competitive procurement awards as largely unanticipated firm-level demand shocks. The results show that winning a procurement contract leads to persistent increases in sales and profits over several years, with sales rising by around 0.20 dollars per dollar of government obligations on impact and peaking at approximately 0.50 dollars after nine quarters, while profits increase by about 0.10 dollars per dollar of obligations, corresponding to a 4–5 percentage point increase in profitability. Procurement also stimulates investment, with capital expenditure increasing cumulatively by around 0.21 dollars per dollar of obligations over a three-year horizon, indicating medium-term capacity expansion rather than short-term scaling alone. Importantly, procurement contracts generate a risk-mitigation effect, reducing perceived uncertainty and default risk, particularly during periods of tight financial conditions: realised stock-return volatility declines by up to 0.5–1%, analyst forecast dispersion falls by around 4–5%, and credit default swap spreads decline by up to 5% following contract awards. Overall, these findings suggest that public procurement can act not only as a source of demand, but also as a stabilising mechanism that improves firms' resilience and investment incentives, with clear relevance for sectors such as semiconductors characterised by large fixed costs and long investment cycles.

The literature suggests that innovation-oriented public procurement can influence firm behaviour through multiple channels: stimulating product and process innovation, supporting capability upgrading, improving revenue stability, and reducing risk. These mechanisms are highly relevant for the **EU semiconductor ecosystem**, which is characterised by high entry barriers, long qualification cycles, large sunk costs, and strong dependence on reference customers. In this context, public procurement under the EU Chips Act could complement supply-side measures by creating early, credible demand for strategically important technologies, such as trusted chips, advanced packaging solutions, or specialised components for defence, space, health, and critical infrastructure. By acting as a technologically demanding lead customer, the public sector could help European semiconductor firms and suppliers cross innovation and commercialisation thresholds, reinforce the effectiveness of R&D and state aid instruments, and contribute to longer-term resilience and competitiveness of the EU Chips industry.

([403]) Budrys, Z. (2025). *Consumer of last resort: Government procurement, firm-level evidence and the macroeconomy* (Working Paper). Retrieved from https://zymantasbudrys.com/wp-content/uploads/2022/10/ZymantasBudrys_JMP_LastConsumer.pdf

ANNEX 5: COMPETITIVENESS CHECK

1. OVERVIEW OF IMPACTS ON COMPETITIVENESS

Dimensions of Competitiveness	Impact of the initiative (++ / + / 0 / - / -- / n.a.)	References to sub-sections of the main report or annexes
Cost and price competitiveness	+	Discussed in Section 6.2.1 which describes reductions in investment risk, lower capital costs via EU co-funding, faster permitting, improved utilisation, and pricing stability
International competitiveness	++	Discussed in Section 6.2.1 which sets out Strategic Projects, sovereign manufacturing capacity, boutique leading-edge foundry example, cross-border clustering, and resilience gains.
Capacity to innovate	++	Discussed in Section 6.2.16 which describes how Strategic Projects enable industrial deployment of publicly funded research, how innovation procurement and thematic grand challenges stimulate high-risk technological development, and how strengthened design capabilities support long-term innovation.
SME competitiveness	++	Discussed in Section 6.2.1.7 which describes impact of incentives for stronger demand pull, anchor customers via innovation procurement, improved access to manufacturing and design capabilities.

2. SYNTHETIC ASSESSMENT

Policy Option 2 ("Strategic sovereignty") is expected to have strong overall positive impacts on the competitiveness of the European semiconductor ecosystem, building on and surpassing the effects of Policy Option 1. These impacts derive from Strategic Projects, targeted demand-side instruments, enhanced supply chain transparency, and combined horizontal measures (skills, faster permitting procedures, Semiconductor Regions of Excellence). The initiative delivers competitiveness effects across all four dimensions as follows:

Cost and price competitiveness (+) improves moderately, driven by reduced investment risk, lower capital costs through EU co-funding, and more predictable utilisation enabled by innovation procurement. Structural cost disadvantages such as energy and labour costs remain, limiting the scale of improvements.

International competitiveness (++) strengthens substantially. Strategic Projects expand Europe's manufacturing and design capabilities, reduce dependencies on a small number of non-EU suppliers, and support the emergence of advanced semiconductor manufacturing capacity, including for AI chips. The balanced reinforcement approach supported by the European Competitiveness Fund ensures that both leading-edge and upstream segments can be strengthened, positioning the EU more strongly in global markets.

Capacity to innovate (++) is significantly enhanced through measures that support industrial deployment of research, strengthen design capabilities, and stimulate high-risk technological development via innovation procurement and thematic challenges. These mechanisms broaden opportunities for innovation and increase Europe's ability to compete in next-generation semiconductor technologies.

SME competitiveness (++) is expected to improve strongly. Strategic Projects and demand-side measures create new market opportunities for SMEs, particularly fabless design firms and specialised suppliers. Exemptions from mandatory reporting and simplification measures under REFIT reduce administrative burdens and support SME scaling.

3. COMPETITIVE POSITION OF THE MOST AFFECTED SECTORS

Semiconductor manufacturing, advanced packaging and chip design segments of the semiconductor value chain benefit directly. Strategic Projects strengthen Europe's capacity across leading-edge manufacturing, mature-node production, advanced packaging and design capabilities. Enhanced scale, improved investment certainty and stronger value-chain integration increase global competitiveness and reduce vulnerabilities to foreign supply disruptions.

Fabless design firms and semiconductor SMEs also experience substantial gains. Increased demand for specialised inputs, early revenue opportunities through innovation procurement, and access to advanced manufacturing and prototyping facilities improve the market position of SMEs. Exemptions from mandatory reporting obligations and streamlined procedures further support development and scaling.

Upstream suppliers, including equipment manufacturers, materials providers and speciality chemical firms, benefit from increased demand associated with new Strategic Projects and deeper integration across the European value chain. Predictable investment flows reduce uncertainty and encourage further expansion of upstream capacity within the Union.

Downstream user industries such as automotive, industrial equipment, telecommunications, cloud/AI infrastructure and defence gain from improved supply stability and resilience. Reduced exposure to global semiconductor disruptions strengthens the competitiveness of these sectors, which were heavily affected during past shortages. The availability of advanced and sovereign semiconductor capacity supports technological upgrading and adoption of AI-enabled systems.

ANNEX 6: OVERVIEW OF IMPACTS ON SMES

Relevance for SMEs
Based on the SME filter and the ISG discussion, this initiative is relevant/highly relevant for SMEs[404]

(1) IDENTIFICATION OF AFFECTED BUSINESSES AND ASSESSMENT OF RELEVANCE
Are SMEs directly affected?
The semiconductor value chain in Europe is characterised by a high concentration of small and medium-sized enterprises, particularly in design, specialised manufacturing services and upstream supply segments. Policy Option 2 introduces measures such as Strategic Projects, the broadened scope of First-of-a-Kind support, and innovation procurement that directly involve these SMEs as project beneficiaries, suppliers, or suppliers for the increased demand for advanced semiconductor technologies. Directly affected SMEs operate primarily in the following sectors: • Semiconductor design and IP services, including fabless design houses, which in Europe consist almost entirely of SMEs and are explicitly targeted through Strategic Projects and innovation procurement. • Specialised semiconductor supply-chain segments, such as equipment suppliers, advanced materials and chemicals producers, and niche tool manufacturers, which provide critical inputs to potential Strategic Projects and benefit from value-chain strengthening measures. • Advanced packaging, testing and related specialised manufacturing services, where many actors are SMEs supplying low-volume or high-reliability solutions that are with scope of Strategic Projects. • Semiconductor R&D service providers and pilot-line operators, including SMEs offering prototyping, design enablement and verification services linked to the deployment of Chips Act pilot lines. SMEs in these segments are therefore directly within scope of the preferred option, either as beneficiaries of new market opportunities or as participants in supported projects.
Estimated number of directly affected SMEs
Based on the quantitative mapping of firms across the European semiconductor value chain, the initiative is expected to directly affect a substantial share of the 1,481 companies identified in the ecosystem. As shown in the sector distribution (Chemicals and gases; materials; equipment; wafers; EDA; fabless; IDM; manufacturing; OSAT; PCB; services;

([404]) https://ec.europa.eu/docsroom/documents/63274

end users), SMEs constitute approximately 69% of all firms active in the European semiconductor value-chain ([405]).

This corresponds to around 1,020 directly affected SMEs across the Union.

Estimated number of employees in directly affected SMEs

Using the mapping of 1,481 companies across semiconductor-relevant value-chain segments, of which approximately 1,020 are SMEs (69%), it is possible to estimate the number of employees in SMEs directly affected by the preferred option (Policy Option 2).

While official, segment-specific SME employment statistics are not available at EU level, we assume that the average numbers of employees working in European SMEs are the following:

- 15–30 employees in specialised materials SMEs**;**
- 30–80 employees in fabless design and EDA SMEs;
- 50–120 employees in equipment-supplier SMEs;
- 40–100 employees in packaging, testing, prototyping and manufacturing-service SMEs;
- 25–50 employees in semiconductor-related service and support SMEs.

Applying these conservative ranges to the SME distribution across segments results in an estimated 45,000–65,000 employees working in SMEs directly and indirectly affected by the preferred option.

(2) CONSULTATION OF SME STAKEHOLDERS

How has the input from the SME community been taken into consideration?

Inputs were gathered through multiple channels, including an Open Public Consultation (OPC) (103 responses, of which 21% were small enterprises and 22% medium enterprises). A Call for Evidence (209 responses, including 16% small and 14% micro enterprises), targeted surveys (64 respondents), expert interviews (14 stakeholders), and 17 thematic workshops including a dedicated SMEs and start-ups workshop.

The consultation strategy achieved robust representation from the SME ecosystem. Smaller entities accounted for **43% of respondents to the Open Public Consultation**, **48% of the Call for Evidence**, and **60% of private sector respondents** in the targeted surveys. These quantitative inputs were complemented by qualitative insights gathered through interviews with investors and industry associations, as well as a dedicated workshop for SMEs and start-ups.

The design of Policy Option 2 was significantly shaped by this feedback. The input specifically addressed operational barriers, the scope of support, and the mitigation of administrative burdens.

([405]) Survey data collected by DG CNECT from Member States in the context of the Chips Act Pillar III mapping and elaborated by the JRC.

First, regarding **operational barriers**, the consultation revealed that the mechanisms to access support were not fully understood. Although targeted survey results showed that 70% of respondents indicated clarity on the overall goals of the initiative, **none of the industry users surveyed reported clarity on the specific application procedures**. In the OPC, fabless companies identified limited access to venture capital as their most critical obstacle (78%), followed by the high cost of Electronic Design Automation (EDA) tools (67%). Interview and workshop participants described pilot line access as unclear and costly for early-stage innovators. This evidence justified the inclusion of measures in Policy Option 2 to streamline application procedures and accelerate the operationalisation of the Design Platform and competence centres.

Second, regarding the **scope of support**, stakeholders from the PCB, equipment, and chip design sectors argued that the original "First-of-a-Kind" (FOAK) criteria favoured large integrated manufacturers. Submissions to the Call for Evidence from business associations specifically called for broader eligibility to include advanced packaging and design. In direct response to this input, Policy Option 2 includes an expanded FOAK definition that explicitly covers advanced packaging and design. These are segments where European SMEs hold significant potential yet face scaling challenges.

Third, the proposal addresses SME concerns regarding **administrative burden**. In the targeted surveys, support for the monitoring coordination mechanisms was notably lower among supply chain stakeholders (62%) compared to national authorities (88%). Interviewees emphasised that complex procedures made it challenging for smaller firms to benefit without external consultancy support. Consequently, the revised monitoring mechanism maintains a strict exemption for SMEs from mandatory information requests.

Are SMEs' views different from those of large businesses?

The consultation data reveals distinct divergences between SMEs and large enterprises when it comes to investment priorities, sensitivity to administrative burden, and the preferred scope of support.

The primary divergence concerns **investment priorities**. For SMEs, particularly fabless companies, survival depends on access to finance and shared infrastructure. **OPC** data shows that **78%** of these firms cited limited access to risk capital as a critical barrier. Conversely, large foundry and integrated device manufacturers (IDMs) responding to the **OPC** rated the existing FoaK framework as satisfactory or neutral (44%), focusing their feedback primarily on approval timelines rather than funding availability. **Interview** stakeholders confirmed this, noting that while the EIC's Chips Fund was effective for deep-tech start-ups, large manufacturers focused on broader framework conditions.

A second major difference concerns **sensitivity to governance and burden**. SMEs and research organisations (RTOs) expressed significantly higher scepticism regarding the effectiveness of governance mechanisms compared to large firms. In a targeted survey, RTOs reported the lowest levels of positive effects from the intervention (35-41%) and rated administrative efficiency as "very ineffective" (18-29%), nearly double the rate of national authorities. This contrasts with the views of large incumbents, who typically possess dedicated compliance departments to navigate complex requirements.

Finally, views differed on the **targeted scope of EU intervention**. In the OPC, large end-user industries and IDMs overwhelmingly supported subsidies for building large-scale manufacturing facilities (**89% support**). In contrast, input from the Call for Evidence and workshops shows that SMEs and stakeholders in the equipment and design sectors argued that the architecture was misaligned with their needs.

(3) ASSESSMENT OF IMPACTS ON SMES ([406])

What are the estimated direct costs for SMEs of the preferred policy option?

Qualitative assessment

Direct costs for SMEs under Policy Option 2 are **limited and proportionate**, for several reasons:

1. .
2. **Participation in Strategic Projects and innovation procurement is voluntary** and does not impose reporting obligations on SMEs.
   SMEs incur administrative costs only if they choose to participate, and these costs are standard for R&I or public-procurement participation (proposal preparation, reporting, contractual obligations).
3. **No regulatory costs are introduced that require SMEs to adapt processes, meet new standards, or undertake mandatory investments.**
4. **No changes to State aid conditions impose compliance duties on SMEs**, because Strategic Projects are designed as co-funded investment instruments, not regulatory obligations.

To sum up, **the preferred option does not introduce new operational costs for SMEs**.

Quantitative assessment

Since SMEs are exempt from mandatory data-reporting obligations:

- **Direct compliance burden = €0** (no recurring reporting or data-submission duties).
- For SMEs participating voluntarily in Strategic Projects or innovation procurement, administrative costs are limited to:
  - Proposal preparation costs
  - Project reporting obligations

These costs are **standard and voluntary**, not imposed by legislation, and therefore **not counted as regulatory burden** under Better Regulation guidelines.

What are the estimated direct benefits/cost savings for SMEs of the preferred policy option ([407])?

Qualitative assessment

([406]) The costs and benefits data in this annex are consistent with the data in annex 3. The preferred option includes the mitigating measures listed in section 4.
([407]) The direct benefits for SMEs can also be cost savings.

SMEs will likely benefit significantly from the preferred option, through:

1. **Increased demand and market opportunities**, especially for fabless design SMEs, manufacturing equipment SMEs, specialist materials suppliers, OSAT SMEs, and R&D service providers. Strategic Projects create stable, long-term demand for specialised SME inputs.
2. **Innovation procurement**, which provides:
    - early revenue streams,
    - anchor customers,
    - reduced commercialisation risk,
    - enhanced technology validation.
3. **Improved access to advanced design, prototyping and packaging facilities**, which reduces SMEs' reliance on non-EU infrastructure and lowers development costs.
4. **Reduced uncertainty and disruption-related costs** due to improved supply chain resilience and earlier visibility of risks (via the Business-to-Business Semiconductor Supply Chain Platform). SMEs were disproportionately harmed by recent shortages since 2020; improved monitoring reduces production interruptions and lost revenue.

Quantitative assessment

The Impact Assessment presents **no quantified SME-specific benefits**, and therefore no numerical estimates are included. Benefits remain **qualitative in nature**, based on the structural improvements described in the report.

What are the indirect impacts of this initiative on SMEs?

Indirect impacts on SMEs in downstream sectors (automotive suppliers, industrial automation, ICT hardware, telecoms, robotics, medical devices) are expected to be **positive**, due to:

- greater semiconductor availability,
- reduced exposure to global supply chain shocks,
- improved foresight,
- increased access to advanced chips including for AI and edge computing.

These sectors contain large numbers of SMEs that previously experienced significant disruption during semiconductor shortages, suggesting substantial indirect competitiveness gains.

(4) MINIMISING NEGATIVE IMPACTS ON SMES

Are SMEs disproportionately affected compared to large companies?

SMEs are **not disproportionately affected** under the preferred option.

Have mitigating measures been included in the preferred option/proposal?

No mitigation measures are required since SMEs are not disproportionately affected by the preferred option . Instead, the initiative includes several features that proactively promote

SME participation and ensure that the regulatory framework remains proportionate for smaller firms. These features include the possibility of participation in Strategic Projects and innovation procurement. The preferred option also enhances SMEs' access to advanced design facilities, prototyping and potentially small-lot manufacturing capacities, and strengthens supply -chain resilience, which particularly benefits SMEs given their higher vulnerability to disruptions.

CONTRIBUTION TO THE 35% BURDEN REDUCTION TARGET FOR SMES
Are there any administrative cost savings relevant for the 35% burden reduction target for SMEs?
The preferred option introduces several simplification measures that generate administrative cost savings for SMEs and contribute to the EU's 35% burden-reduction target. The establishment of more streamlined and predictable procedures under the revised Chips Act, including clearer pathways for participation in Strategic Projects and innovation procurement, reduces administrative complexity for SMEs.